Universidade Federal de Santa Catarina
Centro de Blumenau
Departamento de Engenharia de
Controle e Automação e Computação

André Luiz de Sousa Marcondes Reuter

Application of the embedded component technology in highly compact inverters

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2018

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Final paper submitted in partial fulfillment of the requirements for the degree of BEng. in Automation and Control Engineering of the Universidade Federal de Santa Catarina.
Advisor: Prof. Dr. Tiago Davi Curi Busarello

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Dedico este trabalho a minha família, meus amigos
e todos meus professores e mestres.

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"It is not despair, for despair is only for those who see the end beyond all doubt."

(J.R.R. Tolkien)

Resumo

O setor de energia renovável testemunha um crescimento contínuo desde o começo do século, especialmente o ramo fotovoltaico (PV). Paralelamente ao crescimento em capacidade instalada, há também os avanços em pesquisa e desenvolvimento na área. A questão mais preocupante com os módulos PV é sua baixa eficiência, apenas entre 14% e 18%. Logo, deve haver desenvolvimento de novas tecnologias para elevar a eficiência dos sistemas. Um dos componentes chave em instalações fotovoltaicas são os sistemas de eletrônica de potência (conversores CC-CC e CC-CA), portanto, a eficiência de tais equipamentos deve ser a maior possível. Nesse sentido o microinversor *HiGaN* foi desenvolvido no Fraunhofer ISE. Esse protótipo atingiu alta eficiência com uma alta compacidade e avaliou o uso de transistores GaN nessa aplicação. Entretanto, de modo a ser ainda mais competitivo, o volume e o peso podem ser reduzidos. Uma estratégia compatível para atingir redução de tamanho é o uso da tecnologia de componentes embarcados (TCE), que é uma técnica de fabricação de placas de circuito impresso (PCI) em que os componentes são integrados dentro do substrato. Esse trabalho traz uma revisão e a formação de uma base de dados sobre a TCE e sua aplicação em uma tentativa de reduzir o tamanho da placa mãe do microinversor *HiGaN*. Uma metodologia de *design* é desenvolvida e aplicada e cinco novas versões da placa mãe são projetadas, além de cinco diferentes sub módulos. Os projetos são comparados com suas versões originais e uma análise econômica é feita em torno de ofertas enviadas por fabricantes. Simulações térmicas de transistores GaN embarcados foram conduzidas para avaliar outras capacidades da TCE e fornecer um ponto de vista mais amplo sobre a tecnologia. Os resultados indicam que foi possível atingir uma redução em área de no máximo 27.1% em uma das versões da placa mãe. Um dos sub módulos projetados atingiu uma redução em área de 65% confirmando que a TCE permite reduções mais substanciais em placas de baixa potência. Os resultados das simulações térmicas demostraram que a TCE pode ser uma ferramenta útil para melhorar o comportamento térmico de componentes ativos de potência. O trabalho mostra que o desenvolvimento da tecnologia deve ser continuado e devem existir mais aplicações em eletrônica de potência usando substratos orgânicos, de modo a explorar todas as facetas da tecnologia.

Palavras-Chave: 1. Tecnologia de Componentes Embarcados. 2. Microinversor. 3.

HiGaN. 4. PCI.

Abstract

The renewable energy sector witness continuous growth since the start of the century, specially the photovoltaic (PV) branch. Parallel to the growth in installed capacity there is also advances in research and development in this area. The most significant issue with PV modules is the low efficiency, only between 14% and 18%. Therefore, there must be development of new technologies to increase the systems' efficiency. One of the key components in the PV systems is the power electronic systems (DC-DC and DC-AC converters) therefore the efficiency of such devices must be the highest possible. In this sense the *HiGaN* microinverter was developed at the Fraunhofer ISE. This prototype achieved very high efficiency with a compact form factor and evaluated the use of GaN transistors in this application. However, in order to be even more competitive the volume and weight can be further reduced. A suitable strategy to achieve size reduction is using the embedded component technology (ECT), which is a printed circuit board (PCB) manufacturing technique where the components are integrated inside the substrate. This work brings an overview and a database formation on the ECT and the application of the technology in an attempt to reduce the *HiGaN* microinverter motherboard size. A design methodology is developed and applied and five new versions of the motherboard are designed alongside five new submodules. The designs are compared with their original versions and an economic analysis is made around offers provided by manufacturers. Although none of the designs are realized, thermal simulations of embedded GaN transistors are performed to evaluate other capabilities of the ECT and provide a wider look into the technology. The results indicate that it was possible to achieve a maximum size reduction of 27.1% on one of the motherboard designs. One of the microcontroller modules designed achieved 65% of area reduction confirming that the ECT allows for more substantial size reduction when applied in low power boards. The thermal simulations demonstrated that the ECT can be a useful tool to improve thermal behavior of power active components. This work shows that the technology development must be continued and there must be more applications of the ECT in power electronics using organic substrates in order to explore all the facets of the technology.

Keywords: 1. ECT. 2. Microinverter. 3. HiGaN. 4. PCB.

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1 Introduction

1.1 Motivation and context

The renewable energy sector grows each year both in generation installed capacity and research and development of new technologies, especially the photovoltaic (PV) power generation branch. The total installed capacity raised 4300% in 2017 compared to 2007 and it is now 404.5 GW globally [1]. This remarkable expansion is leaded mostly by the Chinese market which in 2017 reached 32.3% of the total global share and the global forecast is very optimistic [1]. Figure 1 presents the evolution of the global total installed capacity since the beginning of the century. In Figure 1 *APAC* stands for Asia-Pacific excluding China; *MEA* stands for Middle East-Africa and *RoW* stands for rest of the world.

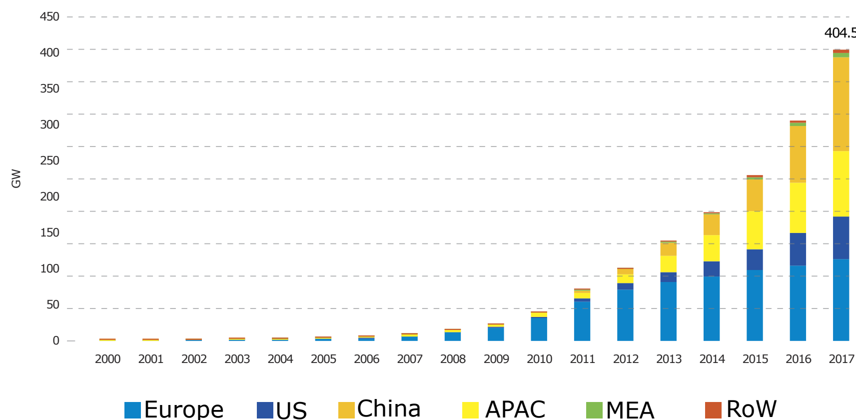


Figure 1 – Global total installed capacity 2000-20017 [1].

Besides the strong dominance of China and the Asia-Pacific region as a whole, the markets are expanding globally. In 2017 the EU market saw a 30% increase in yearly installed capacity compared to 2016, installing 9.2 GW and finally recovering from a five-year downturn. The EU bloc is still the second largest market. The US market, besides a slight decrease in yearly installed capacity still holds the third position and should be a strong market in the next years due to new legislation [1]. The Latin America market stood out in 2017 with Brazil installing for the first time over 1 GW in one year, although solar energy represents just 0.01% of the country's energy production [1][12]. Figure 2 presents the evolution of the global annual installed capacity. The acronyms are the same as in Figure 1.

Beyond the increasing installed capacity there is also the advance in research and development of the PV systems. The most significant issue with PV modules is the low efficiency, only between 14% and 18% though there are new technologies being developed

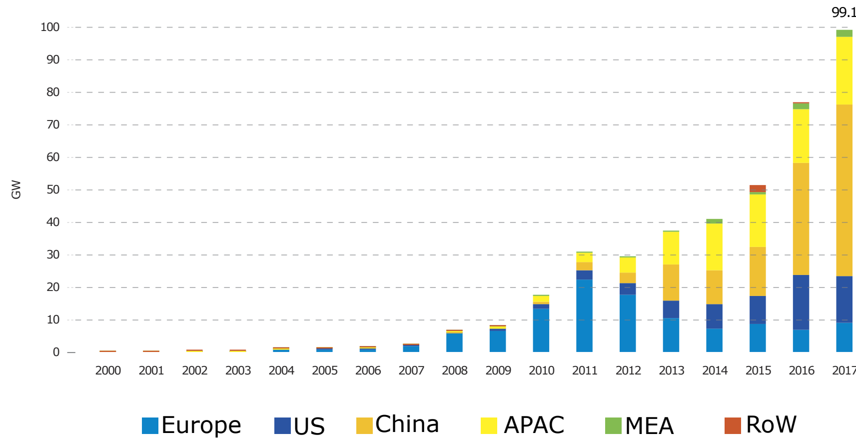


Figure 2 – Global annual installed capacity 2000-20017 [1].

in academic research [13][14][15] capable of reaching efficiencies of over 40% and even 50%. Despite the advances in the academia, the commercial available high efficiency modules aren't competitive enough yet, being more expensive and not providing expressive gains in efficiency [16]. It must be observed that the global efficiency of a PV system does not rely exclusively on the panel efficiency itself. One of the key components in a PV system are the power electronics systems (DC-DC and DC-AC converters) therefore the efficiency of such systems must be as high as possible.

In the inverters area (DC-AC converters), the microinverters, also referred as MLPE (Module Level Power Electronics) are rapidly gaining market share [17]. It is expected that the worldwide energy production by microinverters reach 2 GW in 2018 and the market value is projected to worth US$ 990.3 million by 2022 [18][19].

Solar microinverters are power electronic devices that convert DC power from a low power source, such as a PV module to AC power and are commonly constituted of two stages: 1) a DC-DC boost converter to step up the input voltage and guarantee operation at a maximum power point and, in some cases, provide galvanic isolation, and 2) a DC-AC converter to finally deliver the AC power with acceptable index of energy quality to an appliance or directly to the grid [20]. These devices are commonly rated to handle the power of a single PV module and in a system using microinverters each PV module has its own converter [17].

There are many intrinsic advantages of using microinverters such as the reduction of mismatch losses and partial shading losses, more modularity and flexibility on system level, the possibility of module disconnection since they are isolated [21] and the possibility of having multiple panel types and different orientations in the same system [17]. Furthermore, moving from centralized inverters to microinverters is proven to result in higher harvested energy and longer lifetimes [22]. More importantly, in specific configurations, using microinverters could lead to overall system efficiency improvement and lower installation costs [23].

Microinverters are technically challenging systems due to high specific costs (€/W) because of the low power processed (typically 250-400W); size and weight are critical because the installation is done beside or underneath the PV modules, thus requiring high power density PCBs (Printed Circuit Board) and the device have to be capable of operating in harsh environmental conditions (rain, dust, high and low temperature, etc.) [21]. Furthermore, the commercially available options still present high failure rates compared to centralized inverters [17].

Considering the challenges cited above the *HiGaN* microinverter, a prototype of a microinverter was developed at the Fraunhofer ISE (Institute for Solar Energy systems), as part of an industrial project. The main objectives of the prototype are reduction in weight and volume compared to commercial available solutions as well as high efficiency, while evaluating the use of GaN (gallium nitride) transistors for this application. The particularity of this prototype is that it is capable of processing reactive power and it is galvanically isolated, which means that the DC link can be completely disconnected in case of e.g. fires or power outages. A galvanic isolation is particularly required in order for the device to be in compliance with new grid codes that are, for example, currently used in USA and Austria [21].

The inverter has two stages: an isolated DC-DC converter that uses a fullbridge push-pull topology with a fullbridge rectifier and a DC-AC converter based on a H4 bridge topology with a LCL output filter. The DC link between the two stages is only capacitive (refer to Section 1.3 and Figure 4 and Figure 5). The general specifications of the final prototype are presented in Table 1.

Paramenter	**Value**
Input voltage	15-60 V_{DC}
Output voltage	230 V_{AC}
DC-Link voltage	350-400 V_{DC}
Max. output Power	350W
Max. efficiency whole system	92.4%
Switching frequency DC-DC	150 kHz
Switching frequency DC-AC	50 kHz
Dimensions	150 x 150 x 30 mm
Weight	488 g

Table 1 – Final specifications of the *HiGaN* prototype

The *HiGaN* prototype is modular meaning that the power circuits (DC-DC and DC-AC converters) as well as the microcontroller circuit are built in separate PCBs and connected to the motherboard using header connectors.

As seeing in Table 1, the global efficiency of the inverter (considering the two stages and the auxiliary power supply) is 92.4% and is reached when the output power is approximately 150 W, without MPPT (Maximum Power Point Tracking). In order to achieve

this efficiency some design and hardware choices are worth to be noted. The key component used in both power stages are the high efficiency and very low gate on resistance GaN (gallium nitride) transistors. Also, the rectifier is built using SiC (silicon carbide) diodes, which are also very efficient. The modulation technique used is bipolar PWM and the switching frequencies used are 150 kHz for the DC-DC converter and 50 kHz for the DC-AC converter. A higher switching frequency is used in the DC-DC converter in order to reduce the size of the transformer.

The current version of the prototype fulfilled the requirements of the project and showed good results in the conducted tests. Nonetheless, the prototype could be improved in some aspects. There were some issues with the thermal performance, especially with the power transistors reaching high temperatures. The efficiency could be improved as well. But the most important improvement to be made is size reduction. As mentioned the production cost of microinverters are high (especially if GaN transistors are used), therefore the cost per volume and cost per weight has to be as small as possible in order for the device to be more commercially attractive.

Size reduction in PCBs can be achieved by various different ways, mainly by layout optimization, of course, by combining different functions and components or using smaller component packages. Another way to reduce the PCB size is to use different fabrication technologies. One option suited for this purpose is the ECT (Embedded Component Technology) which is a type of PCB manufacturing technology known and used through more than thirty years. In this technology the passive and/or active components are embedded in the PCB substrate, meaning that the components are buried inside the core material of the PCB.

Nowadays there are a variety of methods to embed components and, independently of the method used, the ECT can deliver very desirable features. Some electronics manufacturers such as Motorola and Nortel have reported size reductions of 40% up to 50% respectively and some even reported costs reductions of 14% (Motorola) up to 40% (Inboard) [24]. Besides size reduction, there are other benefits in using ECT, such as reliability improvement since the components are inside the PCB substrate, therefore more protected from the environment and the mechanical stresses; faster signal speed due to component proximity; signal integrity is raised and interferences reduced; design is also improved as the components are integrated to the PCB, parasitic losses can be minimized mainly in high frequency applications [24].

It must be noted that the ECT has been successfully applied in many fields of the electronic industry, mainly in consumer electronics [2], as well as in more critical application like military and aerospace [25][26]. However, the use of this technology in power electronics has yet to be fully investigated and therefore the effects, advantages and disadvantages can be different compared with other field of applications.

1.2 Objectives

Considering the motivation and context exposed the objectives of this thesis are:

1. Review the current state of the art of the ECT as well as comparing different methods and techniques.
2. Develop a design process for PCBs with ECT.
3. Develop and design a more compact version on the *HiGaN* prototype using the ECT.
4. Investigate the use of the ECT specifically for power electronics.
5. Deepen the knowledge in advanced PCB manufacturing technologies and high efficient microinverters and components.

1.3 Presentation of the current prototype

The *HiGaN* prototype, current version 2.2, which is the starting point of this project, is a galvanically isolated two stage single phase microinverter rated for maximum power output of 350 W. The two stages consists of a) a DC-DC converter stage to boost up to the required DC link voltage and galvanically isolate the inverter and b) an inverter stage that feed the energy to the public grid. One of the advantages of this concept is that the MPP (Maximum Power Point) tracking can be realized independently from the control loop of the grid [21]. A picture of the version 2.2 of the prototype with a description of the modules can be seen in Figure 3.

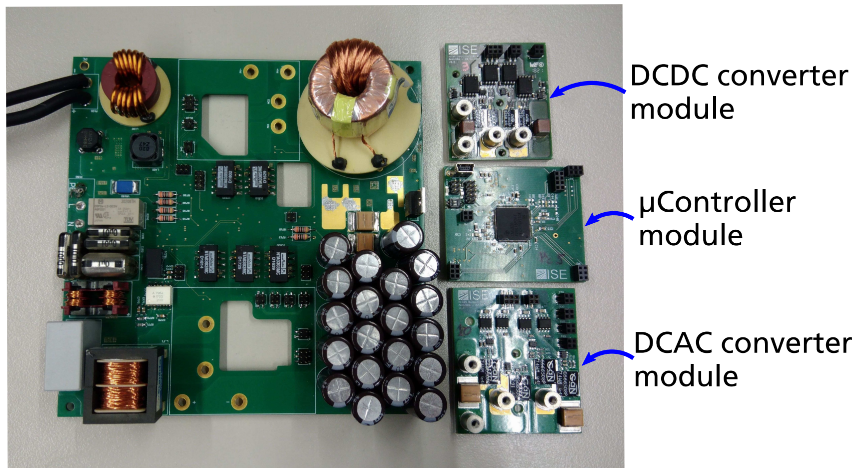


Figure 3 – *HiGaN* v2.2 microinverter.

The DC-DC converter stage circuit schematic can be seen in Figure 4 and can be separated in two parts the primary and the secondary. The primary side (input side,

V_{PV}) is a fullbridge push-pull converter. Using this topology the transformer is simpler, the transistor blocking voltage is lower and the overall efficiency is higher compared to other boost converter topologies. GaN transistors are used in the converter, which present very low switching losses (compared to Si devices), therefore a higher switching frequency can be used and thus the size of the transformer is reduced. It is advantageous to use WBG (Wide Bandgap) devices such as GaN or SiC instead of Si switches due to their better switching characteristics which leads to less losses and overall increased efficiency[27].

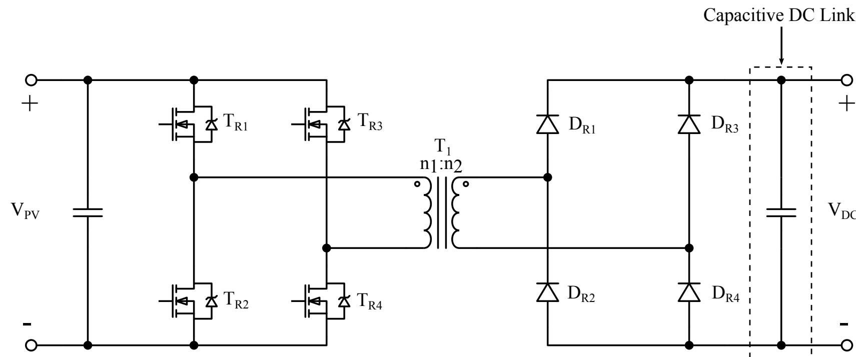


Figure 4 – DC-DC Stage of the *HiGaN* microinverter.

In the secondary part there is a fullbridge rectifier using SiC diodes that are also more efficient than the Si counterparts and the topology grants a more simpler transformer, a lower diode blocking voltage and a lower diode current consumption hence a higher overall efficiency. The DC link is capacitive and acts as an energy buffer and a 100 Hz ripple filter.

The DC-AC or inverter stage circuit schematic can be seen in Figure 5. The topology used is a H4 bridge with a LCL output filter and in this stage the GaN transistors are also used. This topology is classical and it is one of the most commonly used in commercial inverters. The switching strategy used is bipolar PWM for both the DC-DC and DC-AC stages due to the parasitic capacitance of the PV module [21].

To have a global overview on the functioning of the prototype a simplified block diagram is seen in Figure 6.

The overall specifications are seen in Table 1. The LCL output filter is further hybridized with the EMC output filter which reduces the size of the filter inductors used. The output of the *HiGaN* also contains a grid disconnection system with an electromechanical relay, as seen in Figure 6, therefore the microinverter can be fully isolated from the grid.

As seen in Table 1 the maximum output efficiency is high. The DC-DC stage maximum efficiency was 97.7% and the DC-AC stage maximum output efficiency was 98.5%. Although the efficiency could be increased by improving the auxiliary power supply circuit and the microcontroller power consumption should be reduced. Unipolar switching

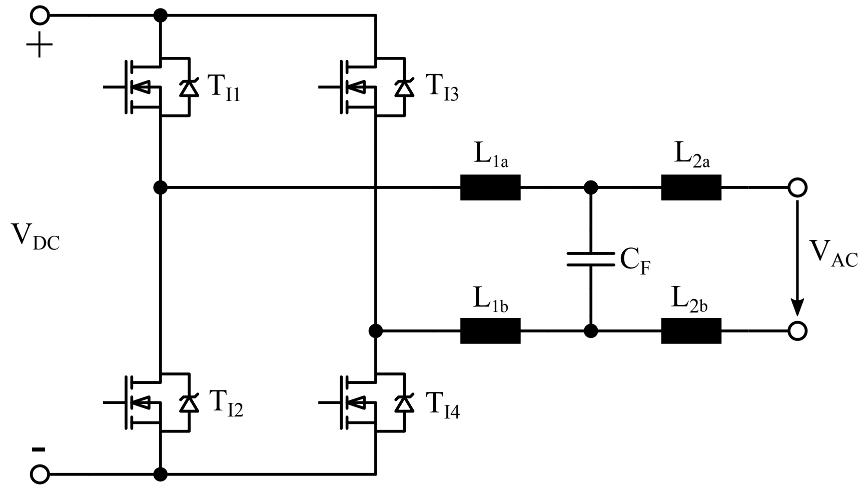


Figure 5 – DC-AC Stage of the *HiGaN* microinverter.

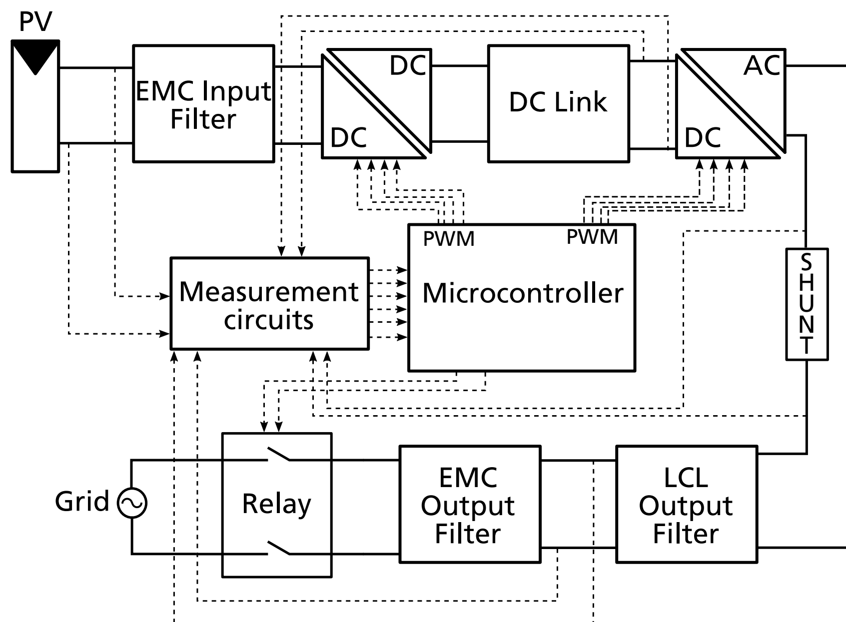


Figure 6 – Simplified block diagram of the *HiGaN* microinverter.

strategy and bootstrapping circuit could also be implemented in order to achieve higher efficiency in the DC-AC stage.

One of the issues with the final demonstrator built is thermal management, mainly in the DC-DC module. Measurements using infrared thermography conducted during test phases showed that, for a power output of 250 W, the junction temperature of the transistors in the DC-DC module was approximately 85 °C and for a power output of 350 W the temperature was 110 °C, being already close to the maximum junction temperature of the GaN transistors used (150 °C). This operation temperatures can significantly reduce the lifetime and affect the efficiency of the device. One of the reasons why the thermal performance is not optimal is because the board is passive cooled to reduce the volume of the final product, therefore the cooling strategy could be improved.

The final external dimensions and weight are 185 x 185 x 35 mm and 0.7 kg respectively

(PCB plus the case developed for the demonstrator). If compared to commercial available microinverters, the *HiGaN* project can be considered a competitive solution in terms of power to weight ratio (W/kg) (Figure 7) although outperformed by other microinverters in terms of power to volume ratio (W/m^3) (Figure 7). Nevertheless the prototype is galvanically isolated and can process reactive power, capabilities that aren't commonly available. It is also worth to note that some of the microinverters in the comparison process power in the range of kW.

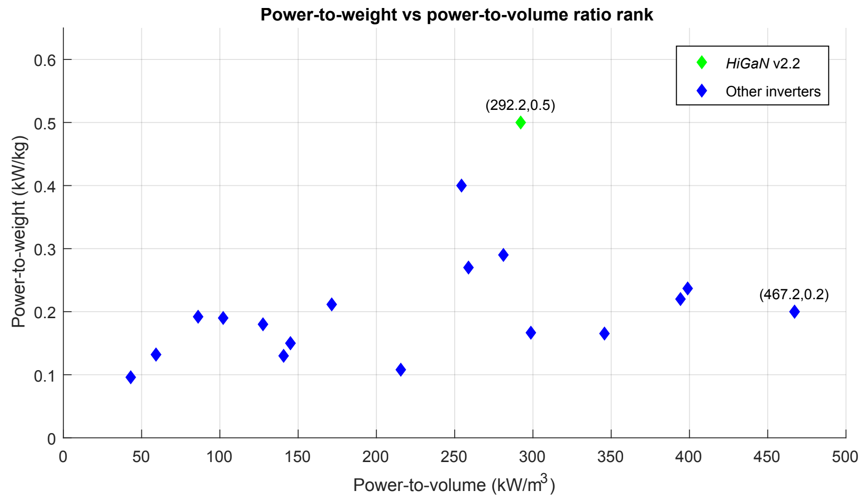


Figure 7 – Power-to-weight and power-to-volume ratio microinverters rank.

From Figure 7 it is clear that reducing the size of the inverter would substantially increase the commercial competitiveness since using WBG (Wide Band-gap) devices such as the GaN transistors is still very expensive, but if the device developed compensates for the extra cost being extremely compact and efficient it could be more easily accepted in the market. This means, essentially, that a displacement in the X-axis is already enough.

2 Literature review

2.1 Overview

The embedded components technology (ECT) is an advanced printed circuit board (PCB) manufacturing technology applied and used by the industry through more than thirty years [24]. The development of this technology was initiated with the goal to have smaller and lighter products with the same or lower costs and to add functionality and value to the PCBs. As the consumer electronics industry refined the process of embedding components throughout the years and the products realized started to be more reliable and with increased quality, sectors with critical and specific applications such as automotive, aerospace, communications and military begun to use this technology [26].

The usage of this technology started in in the late '70s by hybrid PCBs (PCBs composed by both organic and inorganic materials) manufacturers. Initially only passive components were embedded to the PCB substrate. Passive components being components that do not cause a gain neither in voltage nor current in the circuit [28]. In the '90s the AML technology patented by Hoffman Leiterplaten GmbH and the SIMOV by Siemens AG enabled the embedding of active components and semiconductors packages in organic substrates [25]. The Japanese market was one of the first to witness large scale productions of devices using ECT with Murata Manufacturing in 1997 shipping antenna switching modules using the technology [24]. In parallel, the advances in packaging technologies that, combined with the ECT, started to increase the range of solutions for designers and electronics manufacturers [5]. The production of devices with embedded passives rapidly increased due to the series of advantages provided by such manufacturing process, but the technology usage stagnated in the last ten years mostly due to the lack of incentive coming from the manufacturers.

Despite the constant decrease in consumption of passive devices in the past seven years mainly in the consumer market (namely the largest market) [29] and the global trend towards the so called SiP (system in package) market, the amount of passive components in PCBs is still huge and certainly much greater than when the ECT was being first explored. This is one of the factors that kept the ECT as an economical attractive technology during the recent evolutions of electronics devices. Generally speaking, the demand for passive components usually increases proportionally with the power installed on the boards. Therefore, as a high component count demands more space on the PCBs, embedding passives is very attractive to the manufacturers in order to keep devices with a small form factor. This is particularly important in the mobile segment, one of the markets that witness constant growth [29], but also in industrial and specialty segments

like renewable energy, medical, aerospace and military applications.

Embedding passive components seems to be attractive due to the passive/active components ratio in PCBs, however this ratio is decreasing gradually over the years and although more expensive, more and more in-chip solutions are developed. It is important to note the constant global decline of the PCB industry in the last 20 years and in the opposite side the constant growth of the semiconductors industry with the yearly revenue of this branch being over four times the PCB branch [25]. This is one of the reasons why the ECT may not be as attractive to large scale consumer electronics since this segment is looking for the desired embedded solutions directly in package or SiP technologies. On the other hand, specialty segments (military, aerospace, medical, etc.) have a fair smaller demand of PCBs and generally needs that are not attractive for semiconductors manufacturers to fulfill since the start-up costs are too high for small to medium scale production and generally the solutions required are much more complex, thus this segments can take advantage of the ECT.

The ECT could drive the evolution of PCB manufacturing towards the next level of miniaturization with the board being faced as one large component and thus leading to solutions where the final product is capable of handling all sorts of conditions while having the desired features. The industry is taking advantage of the ECT not only for miniaturization but also for delivering new capabilities on the products with the same or small form factors [30]. Therefore, the limits and constraints of the technology as well as how it can be used to fulfill the requirements of the design in the most optimized way must be investigated and documented.

The IPC standard IPC-7092 - Design and Assembly Process Implementation for Embedded Components offers guidance for designers and manufacturers describing the different techniques and challenges of the technology. However, it doesn't standardize a unique methodology nor design rules enabling the existence of multiple methods of manufacturing and consequently different requirements and particularities requiring designers to deeply understand about PCB manufacturing.

The ECT can be divided in embedded formed components and embedded discrete components. Each method is distinct in the manufacturing process and the final properties of the PCB and it is up to the designer to choose which method to use depending on manufacturers capabilities and desired features or requirements of the project.

2.2 Examples and fields of application of the ECT

As a manufacturing technique, theoretically, the ECT could be applied in any PCB. As described earlier, this technology started its evolution in the area of consumer electronics. In fact nowadays it is most predominantly used in the smartphone industry where the companies have developed their own methods of fabrication and the use of ECT is well

justified since the PCBs used in such application have high component density and must accommodate a great amount of functionality in a small form factor. The company Samsung, currently the worldwide smartphone sales leader [31], uses very advanced embedded components solutions and since 2015 is selling memory modules using PoP (Package on Package) technology [2]. In a single package a 3 GB DDR3 RAM memory, 32 GB eMMC (embedded multimedia card) and a controller are integrated with the external dimensions being only 15 x 15 mm and the estimated area savings compared to standard solutions are up 40% [2]. Figure 8 presents the KMR210008A memory module which is one of the commercial available modules using ECT.

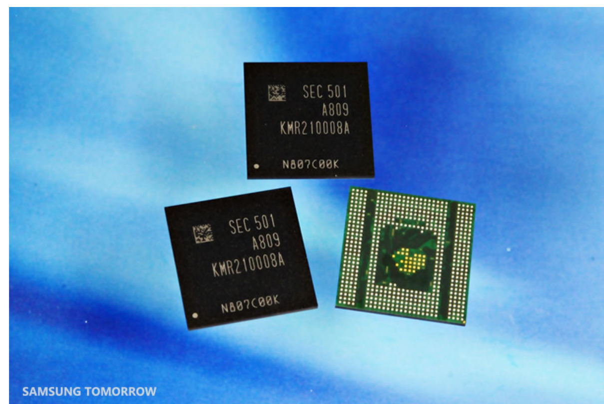


Figure 8 – KMR210008A memory module [2].

The ECT is also applied in very critical applications such as radar modules and military communication equipment [32] [33]. Another area where high reliability is required is in powering transistors gate drivers and a good example is provided by the company Murata with the MGJ1 Series which is a highly compact isolated DC-DC converter and has embedded, among other components, the isolation transformer. The module is seen in Figure 9, the dimensions are 20 x 15 mm which makes for one of the smallest modules with the same parameters in the market.

Figure 9 – MGJ1 5.7kVDC isolated 1 W gate drive DC-DC converter [3].

In the power electronics field however there aren't many applications examples of standalone ECT. Instead, in this field, the integration is generally tied with the use of different substrates such as in the case of the SiPLIT technology for example [9] or as presented by Charboneau et al. where power MOSFETS are integrated in a ceramic substrate to evaluate properties of different liquid cooling methods [34]. One good example is described by Biela, et al. where a higher power density is achieved in a EMI filter but there is also use of ferritic layers [35] . The integration of power devices is also described by Schindler, et al., again to evaluate liquid cooling solutions [36].

One industry that started to take advantage of embedding power devices is the automotive with the increasing need of miniaturization and the rise of electric vehicles. Ostmann, et al. describes a new embedding process as well as its application on high power inverter applicable in a hybrid vehicle [37]. Also, Al et al. shows the development of a embedded die packaging technology specifically for power devices applied directly to the automotive industry [38].

2.3 Embedded formed components

The ECT can be separated into two main methods: embedded formed components and embedded placed components. Embedding formed components means that the components are formed during the fabrication of the board, in other words, the components are manufactured together with the PCB. This method is well established and there are a great number of different techniques to achieve it. Formed components are attractive due to mass production cost reduction compared to standard PCB manufacturing and this method offers the least level of risk, although the tolerances and components value range are limited and stability over time is a concerning point. Another point to be noted in the manufacturing level is that manufacturers of standard multilayer PCBs are capable of using this technique without greater further investments.

Forming components is the oldest ECT method and its first use was in hybrid PCBs as mentioned previously. This method literally prints the component inside the PCB substrate using a variety of techniques. It is used only for embedding passive components since forming semiconductors is too expensive and complex and does not provide good results. The fabricator manufactures the component in the primary interconnect substrate and the formed components are made from raw materials at same time as the board [28].

For both resistors and capacitors, different materials can be used like ink formulations, copper foil based materials, dielectric composites as well as various deposition and curing processes namely screen printing, sputtering, ink jet printing, electroless copper deposition, among others [39][24].

The process of forming can be subtractive or additive. In the subtractive process a layer of the material that composes the component to be formed is deposited over the

whole surface of the board, then a chemical etching or mechanical removing method is used to shape the components in their precise locations, this method of forming components is also known as thin film technology.

One good example of subtractive process is the OhmegaPly formed resistors developed in 1970. In this technology a 0.1 to 0.4 μm layer of NiP (nickel-phosphorous) is electroplated over a standard thickness copper foil, this results in a composite called RCM (Resistive Conductive Material). Then the RCM is laminated upside down on the polymer base, usually FR-4, this results in the OhmegaPly Laminate. Finally, the resistor is realized through subtractive means and if done by etching, both the copper and the resistive material can be etched depending on the chemical used in the process [24][40]. Figure 10 presents the Ohmega Ply process flow.

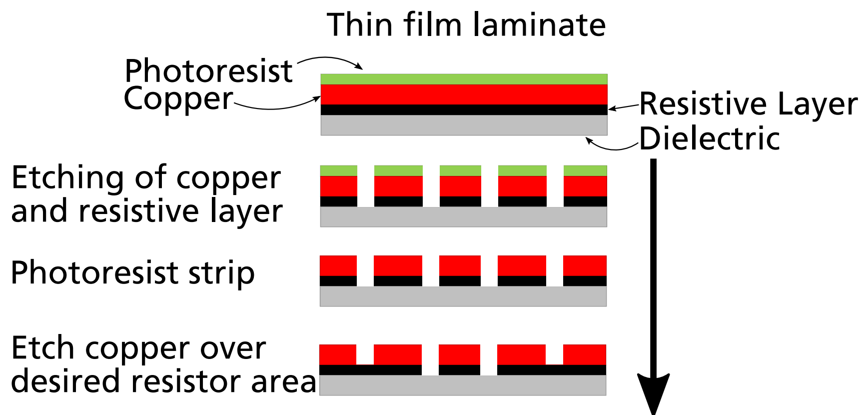


Figure 10 – Graphical representation of the PCB production process flow using the Ohmega Ply technology.

The process is composed of two standard print and three etch cycles. The first step is to apply a photoresist to the OhmegaPly laminate. The second step is the first print and consists of developing the composite image. The third step is the first etching process and this removes the unwanted copper. The fourth step is the second etch and removes the unwanted resistive areas. One can use an etching chemical to remove both resistive material and copper in a single step. The fifth step is to strip the photoresist leading to the sixth step that is applying a new photoresist to print the conductor protective image, being the second print. The seventh step is the third and final etch and consists of selectively removing the copper over the designed area of the resistor. The eighth and final step is to strip away the photoresist [41].

The maximum resistance reliably achievable with the OhmegaPly method is 250 Ω/in^2. There are other thin film technologies that uses the same process flow but with minor differences like other plating methods such as electroless selective plating (M-Pass) or other resistive materials like doped platinum or NiCr [24].

To form capacitors the process is essentially the same changing only the material and the thickness. Essentially what is being produced is a parallel plate capacitor as in

Figure 11, and the capacitance of such capacitor is given by Equation 2.1.

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot L \cdot W}{d} \tag{2.1}$$

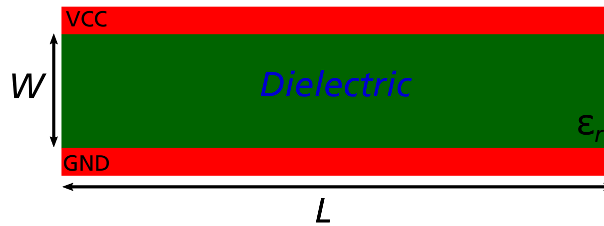


Figure 11 – Parallel plate capacitor.

This way the capacitance value C is inversely proportional to d that is the distance between plates or in this case the thickness of the dielectric material layer, and directly proportional to the permittivity of the material (ϵ_0, ϵ_r) and the length and width (L, W) of the printed capacitor.

There are a variety of materials to laminate capacitors ranging from barium-titanite to epoxy matrix based materials. Basically, to achieve higher capacitance, thinner layers or higher permittivities are desired since increasing the overall dimensions has no point if the purpose of embedding components is to reduce space.

The additive technology performs the opposite of the subtractive technology, the material is precisely added directly on the required position. To form components the material can be made of organic or inorganic pastes and it is deposited as a thick layer ($> 1\mu$m) thus this method is also known as thick film technology. The pastes are added to the substrate and then thermally treated or cured (usually in a conveyor belt furnace at a temperature of 850 °C). The most common method of depositing the pastes is screen printing [24] [42].

Usually thick film components are used with ceramic substrates. For resistors to be printed in copper foils usually the material used is lanthanum-boride and for capacitors the pastes are based on $BaTiO_3$. The manufacturing process uses prefabricated copper foils with the attached components and laminates this foils with prepregs, like the standard procedure for manufacturing multilayer boards [24].

One critical step in the manufacturing of thick film components is the adhesion of the paste to the copper foil. Usually to increase the reliability of the adhesion the copper foils are coated with a copper/glass thermally cured ink [24]. This ink cures at a much lower temperature but this pre-thermal treatment/cure provides a better surface for depositing the pastes and avoids high shrinkage of the copper during the cure of the pastes thus increasing the component adhesion.

This method provides a maximum resistance of 10 kΩ$/in^2$ and usually in the range of 100 pF/mm^2 for capacitors.

In general terms the embedded formed components method is cheaper compared to other methods and its usage is widely accepted in the industry of PCB manufacturing mainly because of its main strong point that is the reliability. Industrial reports states formed components being used in highly critical application without failure [24] and tests in extreme conditions with resistance changes of only 1% [40]. Another interesting advantage is the possibility to make components in custom shapes to achieve different objectives such as better thermal performance or EMI reduction. From a manufacturer point of view this method demands considerably low investments since the process of embedding does not require different types of machinery other than those used in the standard manufacturing procedures, in other words, the components are fabricated alongside the board.

One of the weaknesses of this method is the components tolerances, generally being between 15% and 30% which for the majority of modern applications is not suitable. This happens because the values of the components relies almost exclusively in the final dimensions. Therefore, minimal errors in the manufacturing process results in a large inaccuracy in the components values. Tighter tolerances are achievable using laser trimming but this incurs in higher production costs and times.

Formed components are mainly applied in high frequency circuits and products that doesn't require tight tolerances but work in harsh environmental conditions.

2.4 Embedded Placed Components

Embedding placed components is a newer technique compared to embedded formed components, however the first attempts of integrating bare dies in the substrate date back to the mid '80s [8]. This methodology uses discrete components which can be understood as components in standard SMT/SMD packages, including active components as well and bare dies. The technology is also known as 3D packaging and the development began from the need of more functionality in the same or less space therefore the main focus was in embedding semiconductors [25][6].

This method requires manufacturers to change their production workflow since manufacturing and assembly are done together. As discrete standard components are being embedded the tolerances and stability are not a concern but the manufacturing process could subject components to conditions that may result in physical damage [39]. Although SMD packages are becoming smaller each year, embedding certain components like larger values capacitors could lead to thicker PCBs [43].

Throughout the years many were the methods developed for embedding placed components. Following, an overview of some patented methods available in the market is presented.

2.4.1 AML Technology

Developed by the company Hofmann Leiterplatten, is the first patent of embedded placed components, filled in 1996 and granted to the company in 2004. The process is named AML (Advance Multi Layer) and was the base for other methods.

The patent DE 19627543 describes the basic process flow. The substrate of the board includes multiple surface insulation layers connected with at least one of the inner insulation layers as a distance frame with a window (cavity) where the component is placed and both sides of the window are closed by further layers whose thickness equals at least the height of the component. The contact faces/conductive tracks (copper layers) are on at least one substrate face side and between the insulation layers. It is also described that the prepreg has special cavities that are used as a separator (the spacer prepregs) between the layers of the PCB enabling the manufacturers to use standard technologies without damaging sensitive components during lamination and pressing [33]. In the fabrication, the components are placed on an inner layer and the connection between the components and the layer is made using different methods according to the designer needs or manufacturing capabilities.

The process is very much like standard multilayer PCB manufacturing with the difference of the added windows in the prepregs and isolation layers. Basically the groundbreaking invention or method is how to fill this window or cavity correctly. This specific window technology is used in order to have a stress free embedding of different components/packages in one single press operation. The resin flow as well as the correct resin composition along with the correct opening in the spacer prepreg will fully and safely embed the components [33].

Some attempts of standardization of embedded components techniques entered in conflict with the AML patent, like the attempt of the Japanese JPCA-EB01 that describes a similar process flow and therefore could not be accepted neither by the IEC nor ISO. The standard IPC-7092 is in accordance with the patent regulations and there are specific instructions to negotiate licenses with the company in order not to have patent infringement issues [33].

2.4.2 HERMES Project

In 2008 an EU funded industry and academia consortia, the HERMES project (High density integration by Embedding chips for Reduced size Modules and Electronic Systems) was started. This consortia consisted of eleven partners from PCB design and fabrication industries and applied research and academic institutions and was the successor of the HIDING Dies project that was responsible for developing the technology used by the HERMES project. The main objective was to industrialize a new method of embedding active and passive devices. The company that coordinated the project was AT&S and the

project lasted until 2012. The main result of the project was a method of embedding that has both the acceptance of the industry and academia because of improved properties, cost effectiveness and added value [44].

The technology developed is named ECP (Embedded Components Packaging, patent of the company AT&S) being essentially a laminate-based chip embedding technology that uses core principles of PCB manufacturing. It is a fusion of HDI (High Density Integration/Interconnections) technology, ultra-fine line technology based on a semi-additive technology and a component assembly technology adapted for discrete passive and modified active components [4].

In regular PCB manufacturing the process flow is usually called chip last, meaning that the components placement and assembly is accomplished after the board is completed. The ECP technology is a chip first method in which the chip/component is embedded first in a PCB creating an embedded core that can be built in a multilayer board [4].

The first step of the process is to laser cut registration marks in the ultra-thin copper foil that will be used as guides in the component placement step. The second step is to print conductive adhesive material in the copper foil and then the discrete components are placed face down in the adhesive. The adhesive is cured for a solid bond between the component and the copper foil in order for the components not to move in the following steps [39][5][4].

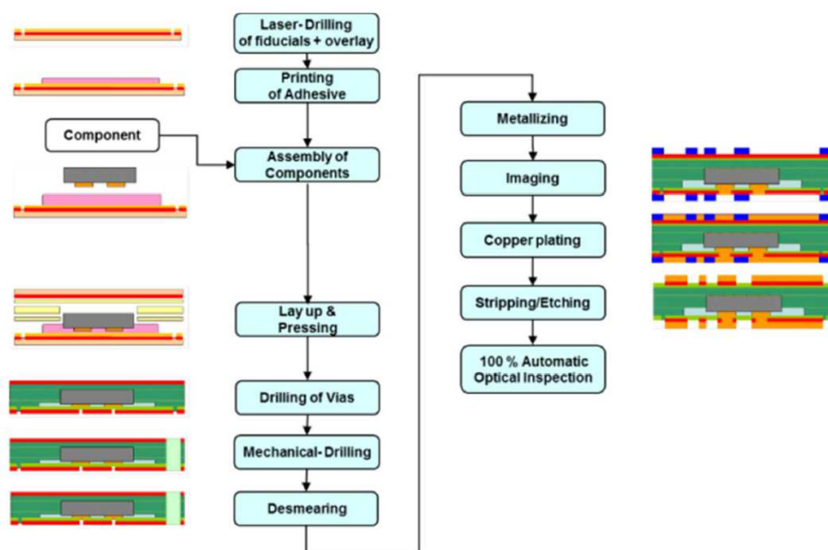


Figure 12 – EPC process flow [4].

The third step is the lamination process. The copper foil with the components firmly bounded by the cured adhesive, the FR-4 prepregs with openings corresponding to the components areas, a regular prepreg without openings serving as a distance frame and a further copper foil are laminated together in a single press cycle. This creates the embedded core. Then via holes are laser drilled and cleaned followed by electroless copper

plating. After that a photoresist is applied using the modified semi-additive process followed by the imaging of the copper pattern. The process is called semi-additive because the exposed copper areas by the photoresist are built by galvanic plating and after the photoresist stripping the remaining copper is removed by flash etching [39][4]. The process steps are seeing in Figure 12.

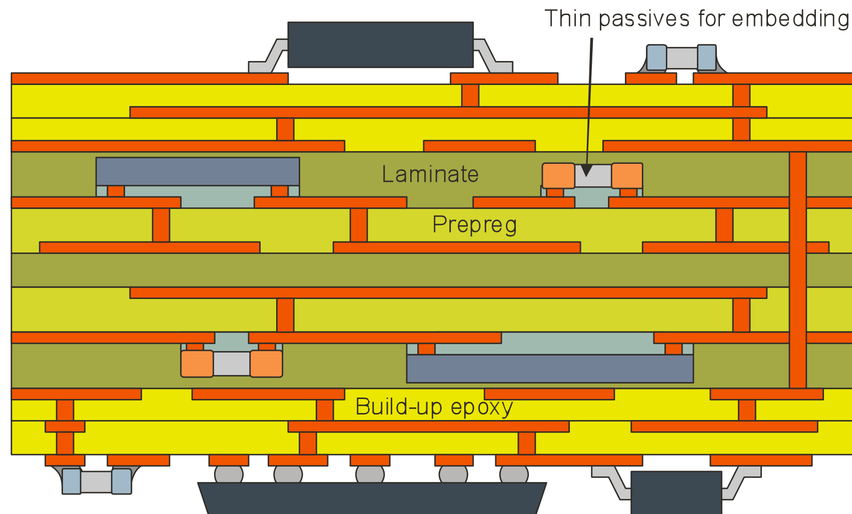


Figure 13 – Graphical representation of a PCB with two EPC cores and components assembled on the outer layers [5].

After all the steps the core pass through an automated optical inspection. It is possible to manufacture a PCB with multiple ECP cores due to the fact that the core can now be viewed as a layer in a multilayer PCB. The restriction is the interconnection between cores that must be made using micro vias and galvanic via plating which can be quite challenging requiring new plating concepts and equipment [4]. Figure 13 presents an example of PCB with more than one EPC core.

The components can also be placed facing up and this creates a distinct way of interconnecting the embedded components with the outer layers and therefore different characteristics from the face-down method described. The face-up approach offers good thermal properties being suited for power components embedding. In the other hand, since components have different thickness, the dielectric thickness will not be constant as well, and this could make the subsequent via drilling and plating process more complex [5].

2.4.3 Multi-Mix

Patented by Crane Aerospace and Electronics, this process is for fusing microwave multilayer integrated circuits and what the company calls micro-multifunctional modules. The technology is based on fluoropolymer composite substrates, which are bonded together into a multilayer structure using a fusion bonding process allowing the integration

of active and passive functions into self-contained modules [32]. This yields to embedded EMI shielding and the PCB itself is a package unit, in most cases even dispensing the usage of an enclosure.

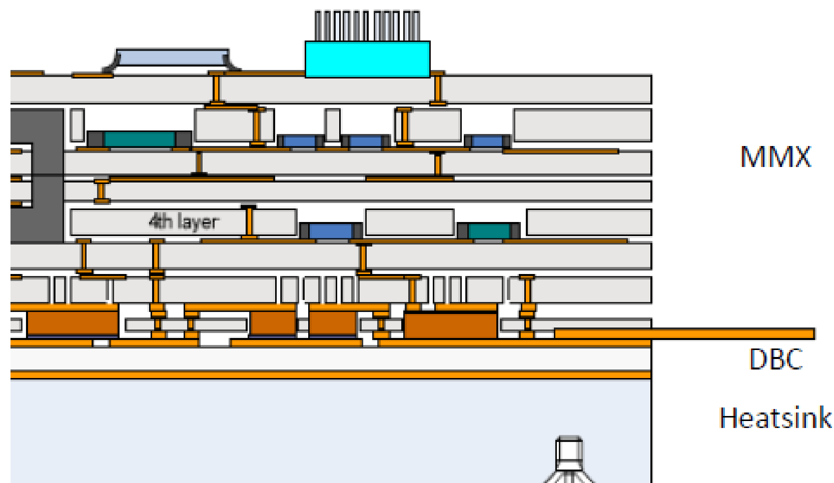


Figure 14 – Graphical representation of the cross section of a PCB using the Multi-Mix technology [6].

The bonding process embeds not only the active components but the passives as well and it even can be used in configurations with formed components. The main advantage of this process is the elimination of the prepregs as can be seeing in Figure 14[6]. The result is a low profile and light weight PCB and the process itself allows for a low cost approach and reduced engineering cycles. This technology is manly suited for highly critical applications such as radars and satellites due to the high reliability and performance [32].

2.4.4 IMB Technology

The Integrated Module Board (IMB) patented by Imbera Electronics is an laminated embedding technology feasible for low- to mid-range I/O count components. The process started development in 1997 at the Helsinki University of Technology [7]. The process itself is very similar to the EPC process described earlier, as is possible to see in Figure 15. The main difference is that the EPC uses ultra-thin copper foil. The IMB process is more focused in the integration of whole systems in the PCB the so called SiB (Systems in Board) and SiP (System in Package) and also BGA (Ball Grid Arrays) packages, and is applicable in many areas.

2.4.5 Embedded Passives and Dies by Amkor

Amkor Technology is also in the embedding market. The company offers embedding in FO-WLP (Fan-Out Wafer Level Packaging) or die-first process. The first step is to

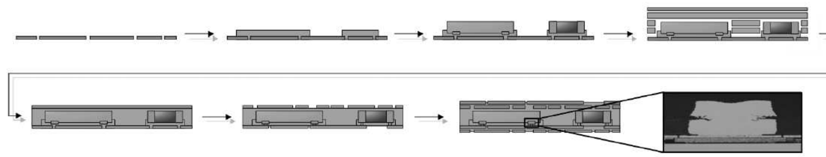


Figure 15 – IMB manufacturing process flow [7].

place a singulated die on a wafer carrier. After that the package infrastructure is built around the die to create a reconstitute molded wafer thus eliminating the need for die attach reflow [8].

Other process are offered such as die embedded in laminate (EPC-like process, or die-first/mid [8]) and the modular embedding, or die-last. In this process flow the top and bottom substrates are prefabricated so the die can be embedded as one of the final process steps. It is also described a process called PoP (Package on Package) where the process flows described can be used to stack packages to create high density I/O [8]. Figure 16 shows samples of each process.

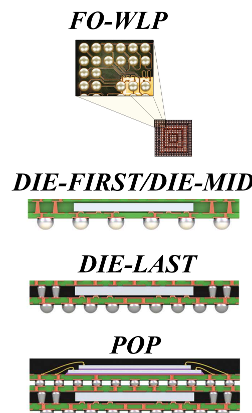


Figure 16 – Examples of manufacturing process flows offered by Amkor Technology [8].

2.4.6 SiPLIT

The SiPLIT (Siemens Planar Interconnect Technology) patented by Siemens is another embedding in laminate process. This technology was developed mainly focusing in power modules systems integration specifically trying to create a better solution than the thick aluminum wire bonds commonly used in power modules packages [9].

The process can use solder, silver sintering or conductive adhesives to attach the dies in the substrate that can be either organic or inorganic (DCB (Direct Copper Bonding) with ceramic substrates). The entire structure (substrate with the dies attached) is covered by a soft epoxy-based insulation film and laminated using vacuum press. After that the contact areas are ablated in the surface of the chip and the substrate using high power pulsed laser, similarly with the ECP process. A sputtered seed layer (photoresist) is then

used as a metallization base for the subsequent photo-structuring process. In this step the interconnects are defined according with the layout. Then, like in the EPC process, copper is deposited galvanically and in the final step the seed layer is stripped by chemical etching [9]. The described process flow can be seeing in Figure 17.

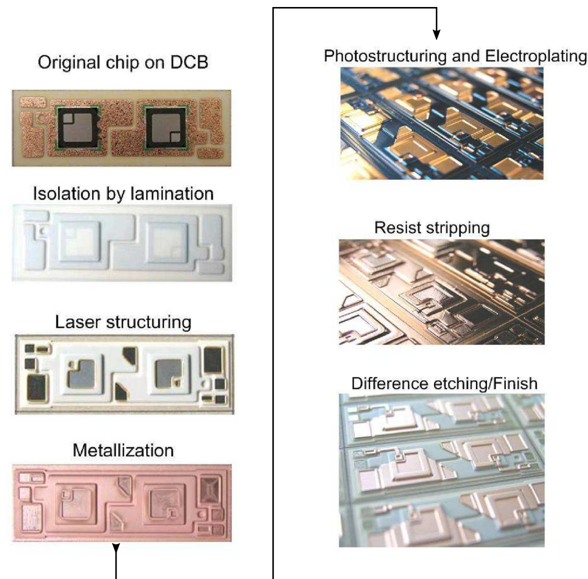


Figure 17 – Process flow of the SiPLIT process applied in a thyristor module [9].

With this process it is possible to use chips with thickness up to 700μm. Since the DCBs have larger cross sections and better heat conductivity as well as smaller heat expansion coefficients it is possible to integrate high power demand circuits such as rectifiers and inverters.

2.4.7 Schweizer's Technologies

Schweizer AG offers some interesting patented embedding technologies. The i^2Board (Integrated Interposer Board) is the company's solution for logic components embedding. Essentially the connections with the semiconductor are made directly to the interposer and it is basically a flip-chip method. This technology allows embedding of both passive and active components and is suitable for logic circuits typically with high I/O counts, although it can be used in a variety of applications since a power dissipation of up to 10W is possible [10]. Figure 18 shows one of the steps of fabrication where the chip is already mounted to the interposer.

The p^2Pack is the company's solution for power electronics. It can be understood more like a packaging technology. Basically power semiconductors (e.g. MOSFET and IGBT) are laminated to a substrate using cavities in the same way as in the ECP technology. Then vias are drilled and galvanically filled with copper to make the connection with the outer layers. The technology offers a symmetric solution meaning that are copper layers both in the top and the bottom of the integrated package, allowing for better thermal

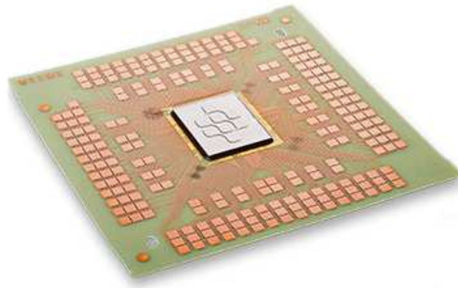


Figure 18 – Chip mounted to the interposer in one of the steps of manufacturing using the i^2Board technology [10].

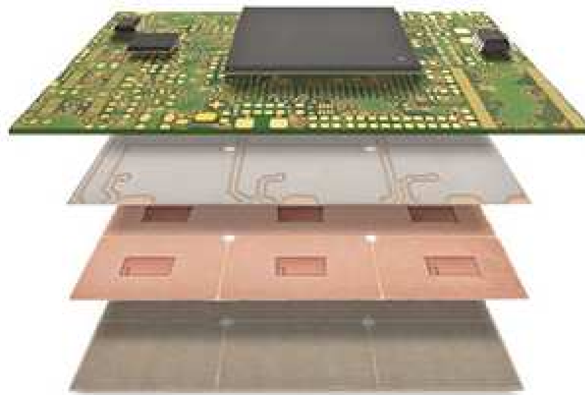


Figure 19 – Illustration of the p^2Board technology process flow [10].

management. Since the final package is flat it can be further embedded in a logic board eliminating the need of other means of connection. This technology is mainly suited for power converters (AC-DC, DC-DC, 3-phase drivers) [10]. Figure 19 illustrates the process flow of the technology.

The μ^2Pack is suited for micro thin, micro pitch applications and is meant to be use in a modular way, that is, different functionalities are built onto a base PCB. The technology can be understood as a PoP method and allows the construction of very thin modules [10].

2.5 Advantages of the ECT

The ECT brings some very desirable characteristics to the PCBs. Alongside size reduction, there are some intrinsic advantages in integrating the components in the inner layers of the board. Following, the main advantages are presented and described. The advantages presented here corresponds to both embedded placed components and embedded formed components.

2.5.1 Size reduction

Size reduction is one of the main subjects in research in electronics in the past decades and one of the most common reasons why the ECT is chosen by the designers. Generally in standard PCBs, size reduction is achieved using components with smaller packages.

One of the smallest packages available in the market is the 0201 (metric package 0603, 0.6 x 0.3 mm). This package usually replaces the 0402 (metric package 1005, 1.0 x 0.5 mm) yielding in a size reduction of 36% in unit area. Although, when considering design rules and pad spacing the reduction is much smaller and the fabrication issues usually are more relevant (handling, assembling equipment, testing) generating reliability issues. Now if embedding the component is possible to achieve 100% of unit surface are savings. It is estimated that the savings in area achieved by reducing the components packages to 0201 is equivalent to embedding the 0402 devices [43].

There are multiple ways of using the ECT to achieve size reduction. If embedding only passive components it is possible to make layouts where the embedded components are directly underneath the active components thus freeing outer layers surface area [30]. If also embedding the active components more functionality can be added with the same space, meaning higher density in the PCB. A smaller surface area also means less material thus material cost reduction. In the case of power electronics size reduction is important because of power density (W/mm^3) [6].

Still, size reduction is highly dependent on the application, the method used and the overall design requirements. For example, Motorola claims that a RF module redesigned using formed embedded components had a space reduction of 44% and the company Nortel, also using formed components reported space savings up to 50% in an emulator product [24].

Another great example is an active hybrid 300W EMI filter designed using embedded discrete components, planar inductors and embedded ferrite core to achieve an approximate 40% size reduction [35]. Crane Aerospace and Electronics claims that their technology Multi-Mix reduces overall weight and volume up to a factor of 10 in filtering applications [32].

2.5.2 Improved Signal integrity

Signal integrity is closely tied with aspects related to transmission lines effects found in the PCB traces. The important aspects are signal speed and propagation time, impedance, reflections, terminations, cross talk, differential signals, return current and loop areas. This aspects are usually critical in logic circuits such as Random Access Memories (RAMs), clock circuits, high frequency switching pattern generators and so forth. In that type of circuits timing is crucial [45].

In power electronics the high frequency signals are usually the switching patterns and are generally within the 500 kHz range. In order to avoid signal reflections preserving the logic circuits and the switches gates, it is needed that the traces have proper terminations and the lowest impedance changes as possible. As well as avoiding parallel traces to overcome the cross talk issue [45].

The key point is protecting the traces against noise and interference and most importantly ensuring that the traces itself aren't causing the issues. The rule of thumb is keeping the traces lengths as small as possible. Sometimes is also critical to maintain some traces lengths equal to each other to avoid problems with differential signals and timing issues. Another important feature to pay attention is power and ground planes, those are essential in high frequency applications to avoid interference. The overall component proximity and decoupling capacitors are important aspects to be noted as well [45][46].

Using ECT the designer is able to significantly reduce the traces lengths and increase component proximity. Another advantage is that the traces and the component itself are surrounded by a single dielectric making it simpler to calculate propagation delays and avoid this issue, as well as increasing the overall signal speed and reducing the noise acquirement from the ambient [30][45]. Still, the connection between the components and power and ground planes could be done more efficiently and it is possible to avoid impedance variations in the traces more easily [30].

An intrinsic advantage of small traces is the reduction of parasitic losses due to smaller trace inductance and capacitance. This parasitic effects are more evident in high frequency switching applications thus using the ECT might be a suitable solution to minimize this problem.

2.5.3 Improved EMI and EMC aspects

In electronic devices, as the frequency of operation increases, the devices start to act as generators of radio frequency signals. The radio energy produced interferes with the neighbour devices and such interference is called electromagnetic interference (EMI). This effect can be really harmful to components in the same circuit and in other equipment. This must be avoided and prevented and the capability of a device of operating without being susceptible to EMI and do not cause EMI is called electromagnetic compatibility (EMC). The device's EMC must be in compliance with the CISPR (International Special Committee on Radio Interference) regulations [28][45].

EMC covers the whole electromagnetic frequency spectrum from DC (0 Hz) to 20 GHz and encompasses the control and reduction of the already mentioned EMI and also electromagnetic fields (EMF) and radio frequency interference (RFI) [28]. Generally designers are more concerned with a specific type of EMI noise, the conductive EMI.

To ensure that the device is not susceptible to and isn't a source of conductive EMI,

input and output filters are applied. These filters are designed to attenuate the two modes of conducted EMI noise: common mode noise (CMN) and differential mode noise (DMN). CMN is the line to ground noise and the noise current flows in the same direction of the signal, returning through the ground. It can be suppressed using inductors in series in each power line and capacitors that are placed in parallel with each power line and ground [47]. DMN is the line-to-line noise where the noise current flows through one line conductor and returns through another without flowing to ground. It is suppressed using capacitors in parallel with the line conductors [47]. An example of input EMI filter is seen in Figure 20, a similar arrange is used as the input EMI filter on the *HiGaN* version 2.2.

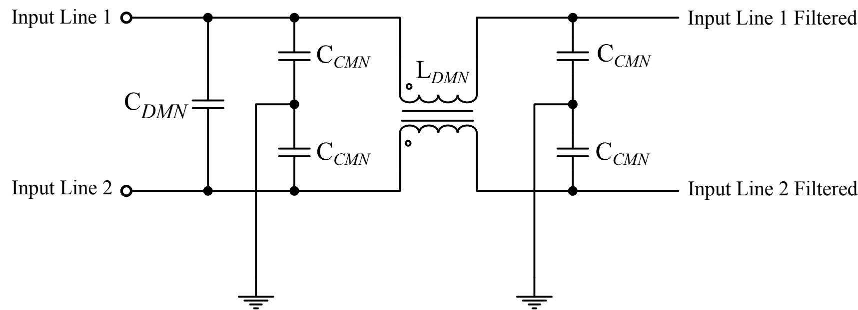


Figure 20 – Example of input EMI filter.

If the input and output filters are realized correctly the EMI noise should be attenuated with a gain below the required by the standards through all the specified spectrum, which is generally between 150 kHz to 30 MHz [47]. However, even though the device is in compliance with the regulations, meaning that the conducted emissions are bellow a certain level, there could still be self deterioration within the device's circuits.

Concerning power electronics, the main source of conductive EMI noise is the switching characteristics of the converters circuits. The EMI noise is usually related to high voltage and high current peaks during switching. The fast variation of voltage over time, or high dv/dt, due to the switching of a transistor, generates high current peaks and create high leakage current in magnetic elements [48]. High di/dt on the other hand, creates voltage peaks due to the stray inductance of current loops [48]. To reduce these effects the dv/dt and di/dt must be reduced, this means reducing the switching frequency and thus increasing losses.

Another consequence from switching is a voltage and current oscillation around the desired level, also known as ringing that happens due to sudden change from both high to low or low to high levels. This transient oscillation has a high frequency and a fast high amplitude peak (also known as overshoot) generating EMI noise. To reduce the ringing effect a damping circuit is generally used, for example a RL or RC snubber circuit in series with the switch. Often the capacitors ESR are also used to attenuate the oscillations [49]. However this also brings losses to the system and a compromise must be made between efficiency and EMI reduction.

An alternative to reduce EMI emissions that affect other circuits within the same board is in the layout level. The key points are reducing the loop stray inductance by shortening signal and power paths, layout optimization for geometric design strategy, use of coupling and filter capacitors [49], use of solid ground planes, isolate signal from power paths and shielding. Those are all good design practices that basically mitigate parasitic effects and thus reduce the EMI emissions. With a good layout and low EMI emissions is sometimes possible to reduce the output EMI filter.

The use of ECT can bring those desired layout improvements. The main effect of embedded components is in reducing trace's lengths due to the type of interconnection which is microvia that has a very small resistance and inductance [50]. Another point is that the components are protected from the environment by the PCB substrate and it is possible to create Faraday cages using the internal copper planes and vias [30]. The proximity with the ground planes also makes decoupling and filtering more effective, for instance, the decoupling capacitors of an IC can be directly beneath the package and directly connected to the ground plane shortening the path and reducing the current loop.

As seen in [50] the use of microvias with embedded ICs resulted in nearly no attenuation on the signal compared with standard technology for the same spectrum, most importantly, very small phase distortion was measured which is even more important in analog measurement circuits, for example. It is also shown that a Faraday cage made simply with through hole vias around the embedded IC is very effective with isolation better than -50 dB against close proximity noise excitation.

Planar capacitors are also interesting for reducing EMI mainly in high density boards as in logic boards with high quantity of high I/O count ICs. Generally at least one decoupling capacitor is needed for each I/O port and thus using a capacitive layer, that is considered a type of embedded formed capacitor, can help no only reduce the component count but also make decoupling more effective since the interconnection inductance is reduced and therefore less conductive EMI noise.

Embedding ferritic layers and magnetic components entirely has also been done. Usually embedding isolation transformers makes possible to reduce leakage inductance and inter-winding capacitance as shown in [51] and thus reducing EMI emissions.

2.5.4 Protection against radiation

Electronic equipment can be submitted to hazardous amount of radiation. Typically, fields that concern about the resistance of electronic equipment against radiation are aerospace, nuclear energy, medical imaging and special segments such as ultra precise measurement and instrumentation. The application defines the radiation environment and thus type and level of protection required.

On the Earth's surface, the primary radiation source are atmospheric neutrons due to galactic cosmic rays (GCR) [52][53], but usually are in harmless levels to electronics. In low to high orbits the radiation levels are much higher and have different configurations. Basically protons, electrons and heavy ions are trapped in the Earth's magnetic field and the effects of solar particle events (coronal mass ejections and solar flares) are much more evident [53]. In deep space missions the effects of GCR is higher because there are no protection from the Earth's magnetic field.

The radiation levels in orbit missions are variable as well. In low orbit at high latitudes the levels and type of radiation mimics the same levels seen by deep space missions [52]. The asymmetry in the Earth's dipole makes that a region of the Earth is closer to the Van Allen proton belt, an effect known as the South Atlantic Anomaly (SAA) and the levels of radiation in this region are higher [52][53].

Depending on the environment the effects are different. There are basically three main types of radiation induced effects (RIE): total ionizing dose (TID), single event effect (SEE) and displacement damage (DD) [54]. The RIE are a concern mainly in semiconductor devices.

In the case of TID, which is a long term, cumulative effect, and degrades the device's performance due to direct and indirect ionization of semiconductor material. When a charged particle passes through the material it interacts with the semiconductor and charges emerge and are trapped in the oxides [54]. This causes a number of issues such as decrease (N-MOS devices) or increase (P-MOS devices) in switch-on voltage, shifting of thresholds, increase in leakage currents and ultimate fail since the device will be permanently activated (N-MOS) or deactivated (P-MOS) [54][53].

SEE on the other hand, is caused by a single charged particle and can have the same effect of the TID [53]. The effects are different depending on the type of particle, but generally a SEE causes a current pulse due to the generated electrons by the passing charged particle [54]. The electrons rapidly migrate to the reversed biased junction causing the current pulse and this causes the soft errors or failures creating transients effects on signal paths (SET - Single Event Transient) or changing the state of a stored bit (SEU - Single Event Upset) [54][53].

DD effects are not particularly seen in oxide devices since this is a non-ionizing damage caused by protons, electrons and neutrons and occurs when these particles interact with the silicon lattice [54][53]. This is also a cumulative effect since the displacement of atoms in the silicon structure is proportional to the flux of particle through the silicon over time [54][53].

There are two types of radiation protected components/devices, the Radiation Hardened components, also known as *rad-hard* and the Radiation Tolerant components, or *rad-tol*. *Rad-hard* components are completely immune to all of the radiation effects cited. The device can be radiation hardened by process when there is, for example, special coat-

ing materials or use of different alloys in the construction; or it can be *rad-hard* by design when some technique is used to cancel the radiation effect, generally done in software [54].

The *rad-tol* components on the other hand are not fully immune to radiation but can be used in radioactive environments as the device will mitigate the radiation effects although still being susceptible to and will be considered as a calculated liability/risk [54].

With the growing aerospace market with more and more satellites being lunch per year and the orbit altitudes being reduced, since the *rad-hard* components are very expensive, there is a trend on the market on using commercial off-the-shelf (COTS) components and try to make them at least *rad-tol* and compromise mission times in order to have better cost effectiveness [55][56].

The easiest way of making a device *rad-tol* is by shielding. So the problem gets to find a material that offers a good trade between radiation protection, stability in harsh conditions, mechanical strength and weight. One of the best materials known for this purpose is polyethylene, because this polymer is highly hydrogenated and this prevents nuclear fragmentation process [52]. Currently, this material is used as a benchmark to test other material for radiation shields [52].

This polymer is widely used in all sorts of applications, is cheap, easy machinable, there are multiple variations of it and can be found as fabric, being ideal to be used as a shield and be incorporated with other polymers as a composite. Polyethylene is also used as a substrate material for flexible PCBs.

In this sense it would be possible to use polyethylene as the substrate material of a PCB using ECT. This way the components embedded on the board would be naturally shielded. Probably the thickness of material wouldn't be enough to make the device *rad-tol* but it could contribute to reduce the overall shielding of the device and therefore reduce overall weight. Or it could be used as an extra measure to protection. In some cases, however, when the radiation levels are lower like in communication applications, for example, this could be used as the final shield.

2.5.5 Improved Thermal management

Thermal management is directly related with the design process being dependent on layout, PCB substrate material selection, component selection, etc. In the package level, when a device operates outside its temperature range it significantly reduces its life cycle, compromises overall system efficiency increasing losses, alters the frequency behaviour and ultimately can fail [28]. As the components footprints are becoming smaller the component density in the PCBs are increasing thus thermal management in the PCB level and how efficiently the components heat can be transferred to a heat sink is a main issue [57].

In power electronics applications like power converters and heat intensive components

like power LEDs, thermal management is an even more important concern. Commonly used design techniques to extract heat from SMT power devices include the use of thermal vias array to transfer the heat from the component to a heat sink [58], use of metal-core PCBs [57], thick copper PCBs for high current applications, water cooled PCBs [36], among others.

When using ECT, since the components are embedded in the substrate it's possible to use the substrate itself as a heat dissipator or heat spreader as well as adding copper planes directly in contact with the components. This feature is particularly interesting for embedding power transistors, diodes and power supply ICs. This is demonstrated by Kearney et al where the embedded solution presented a 30% to 40% smaller thermal resistance than the standard technology [59]. Sharma et al. also demonstrated that embedding power components with substrates using thick copper interposer results in better thermal behaviour [60].

Using different materials for dielectric and prepregs with higher thermal conductivity can also be an alternative to copper, to reduce the size of external heat sinks or in some cases eliminate the need of it. The optimization of the vias pattern lead to a better thermal management and since the distance between the thermal pads of the components to the opposite layer where the heat will be dissipated is shorter, the use of thermal vias can be more effective [58].

One direct example of improved thermal conditions using embedded technology without different substrates is the demonstrator presented by Hofmann which consists in a 54 x 62 mm board with four transistors processing 6 W. In the standard board (without ECT) the outside temperature distribution is uneven and the hot spots reach 185 °C while in the board with embedded components (using the company's patented method, AML) the maximum temperature is 85 °C and it is evenly distributed [33].

2.5.6 Improved reliability

In standard PCBs, components are susceptible to dust and moisture from the ambient when not properly enclosed in a protective case. Accumulated dust reduces the PCB capability of dissipating heat, and in some cases can cause electrical breakdown (arcs) between components [61]. Moisture is responsible for a number of failure mechanisms such as insulation resistance deterioration and galvanic corrosion which can lead to premature failure of the whole device [28]. In case of very sensitive circuits such as analog measurement circuits, this ambient factors might have a greater impact not only reducing the life cycle of the device but interfering in its function during operation [28].

Using ECT the components are automatically protected against dust and moisture, as well as corrosive substances that might be in the air depending on the application. Another advantage is that the components are less susceptible to mechanical stress since

they are surrounded by resin (placed components) or make part of the laminated (formed components) being protected against the main mechanical failure mechanisms, shock and vibration [28]. According to Osmolovskyi, boards with embedded components are also more reliable concerning thermal cycles [62]. The loaded testability is also improved [26].

These characteristics are particularly good for applications with harsh environments such as military and aerospace and heavy industries like mining and foundry. It can also be advantageous for applications such as pharmaceutical and medical that require clean environments.

2.6 Disadvantages

Even bringing various benefits, the ECT has some limitations and disadvantages. Following there are some of the main disadvantages corresponding to both presented methods, embedded formed components and placed components.

A. Although it is a well known technology and it's present in the market for more than thirty years, manufacturers still list it as a special technology and generally only fabricate under special requests. This is a major drawback in case of prototype fabrication.

B. Since the components are inside the PCB substrate, testing and troubleshooting during operation can be very difficult and rely upon the design itself. The designer should plan the board carefully in order to provide test points to critical embedded components or not embed components which will have to be measured thoroughly. This presents a serious limitation for the technology particularly when dealing with active components, specifically testing during the manufacturing process [39].

C. For the same reason as testing is an issue, maintenance is also a problem because it is impossible to replace a damaged component without destroying the board. Therefore, in prototype to small scale applications, potentially problematic components should not be embedded compromising size reduction capability [26].

D. There is lack of dedicated EDA (Electronic Design Automation) tools. Current EDA tools don't provide support for embedded components as a specific category of design, therefore the designer have to configure the tool of choice accordingly [30].

E. Another issue is with the PCB designing workflow. Designing with embedded components requires even more attention to common high density design practices and guidelines with the additional design rules and manufacturing limitations of the technology itself. Also, the designers should treat the project using embedded components no longer as a two-dimensional thing but as three-dimensional solution

and work intelligently to use the technology effectively [30]. This learning curve and common practices adaptation usually takes time and could increase the design costs.

F. The overall cost in prototype scale is higher than standard manufacturing techniques [30]. This is presented in more details in Section 3.3.

G. Although the IPC - 7092 standard describes the different process of the ECT, there are multiple different methods and still patents conflicting with the current standards [33]. This makes even more difficult for the manufacturers to offer the technology and significantly increases cost to the costumer because in some cases there's the need of paying for licenses to use the process [63].

H. Still in the manufacturing context the ECT requires adaptations in the supply chain and in manufacturing equipment [63] [39]. This usually means investments and changes in manufacturing layout and integration.

It must be stated that the points listed in the Section 2.5 can be achieved using both embedded placed or formed components. However, there are some specific disadvantages of both methods that can be decisive in the selection of what process should be used.

2.6.1 Specific disadvantages of embedded formed components

The following points are disadvantages in using embedded formed components.

- The value of the formed components is limited to the material used in the forming process and overall dimension. In general those values are very limited and this constraints the technology's applications [24][30][26].
- As described in Section 2.3 the final dimensions of the etched area in the resistive material or the dielectric defines the formed component value of resistance or capacitance, thus this values have a high dependency on machinery accuracy. That, together with material instability, leads to components with high tolerances, 15% to 30% in general, requiring a laser trimming operation in order to achieve better results, significantly increasing the costs and production times [24][30].
- The material instability overtime is also an issue [24] and can short the device's lifetime or cause reliability problems during operation.
- There are no commonly known or up-to-date commercial available EDA tools that provide support to work with embedded formed components.

2.6.2 Specific disadvantages of embedded placed components

The following points are disadvantages in using embedded placed components.

- In the process of embedding, the components receive a huge amount of mechanical and thermal stress due to the pressing process. This could partially or completely ruin the components [30].
- In some methodologies special components are required such as in the EPC process, for example (Section 2.4.2), that is only able to embed copper termination components due to the method of component attachment [4]. This limits the use of the technology in some cases.
- The embedding process also affects the components values, up to 3% for resistors and 10% for capacitors due to the mechanical and thermal stress the components are subjected during the vacuum press process [63].

3 Design and development methodology for ECT application

In the previous chapters the motivation and objectives for the current project along with a detailed description of the ECT were provided. This chapter is devoted to describe and report the development of a design methodology for the ECT application. This is done showing the steps and workflow used to design a new version of the *HiGaN* prototype aiming size reduction. The requirements and the approach for the design are presented as well as the procedures to use the ECT with the software Altium Designer version 17.1.

3.1 Requirements for the new prototype

Following, the requirements and rules for the new prototype are listed and described.

3.1.1 Use of same components

It is important to understand that, since the *HiGaN* prototype is an already functioning project and its characteristics were well studied and defined, it is not in the scope of this project to modify any functionalities or try to improve characteristics by redesign circuitry. Therefore, the most important requirement is to use the same components values as in the current version of the *HiGaN*. What can be changed are the components footprints and the use of different arrangements of components to reach the same values, for example paralleling capacitors.

This requirement also applies for software and switching frequencies, since the inductive elements used in the current version are specifically made only for this project. Another important observation is that, initially, the power sub modules (DC-DC and DC-AC converters) cannot be modified.

3.1.2 Power path

It is a good practice in PCB designing to well separate the power areas from the signal areas in order to maintain a good signal integrity. In a two-stage inverter for PV application like the *HiGaN*, at the input there is a relatively high DC current (above 10 A, the whole output current of a PV module) and a small DC voltage (between 20 V to 50 V). The DC-DC boost converter boosts the DC voltage to 350 V with low current and at the output we have grid voltage (230 VAC in this case) and a lower current (maximum 2 A).

This kind of power can severely interfere with the low power signals on board (measurement and switching pattern signals). The solution adopted in the *HiGaN* design was to island the low signal circuitry in the center of the board as seen in Figure 21.

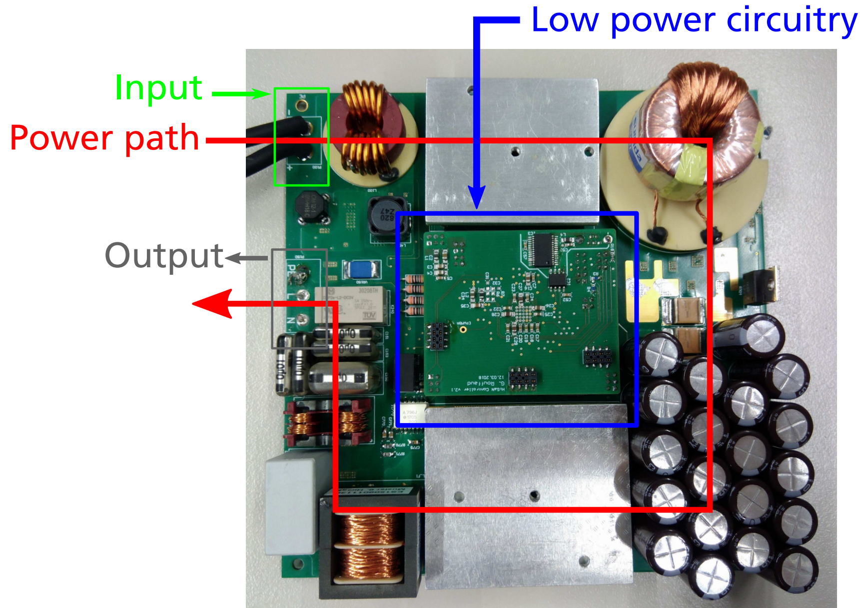


Figure 21 – Power path in the *HiGaN* v2.2.

This power path also permits the input and output to be located in the same side of the board. This feature is important due to how the microinverters are mounted on the PV modules, generally in the back side, hence having the input and output in the same side allows for a better cable management in the system and also for rack mounting.

3.1.3 Dimensions

Regarding the microinverters comparison shown in Figure 7, the aim is to have a better power-to-volume ratio. Since it is much more difficult to reduce the height of the final design due to the large inductors and filtering capacitors, the main reduction has to be made in area. The requirement is to reduce the maximum possible in area and the height of the board's bottom side is set to be equal to the highest component used in the board that is 24 mm.

3.1.4 Embed only passive components

The initial requirement is to embed only passive components since, not considering the sub modules, the passive-to-active ratio in the current prototype is fairly high (around 7:1). Another reason is that to embed certain active devices there might be the need to get the bare dies from the manufacturers and this could be somewhat non-trivial or not cost effective.

Still, as mentioned in Section 2.6 there is no easy way of performing tests and measurements in embedded components unless modifications in the layout are done, being one more reason to not embed the active devices at first. This also the reason to deliberately not embed specific passive components that are critical for the functioning of the inverter, are very sensible, are optional components that might or might not be populated, and some potentially problematic components that will likely have to be replaced at some point.

3.1.5 Embedding method to be used

Regarding the points described in Section 2.4 and Section 2.6.1 the method to be used in this project is required to be embedded placed components. Another reason for that is the software used for the design. The current version of the *HiGaN* was designed using Altium Designer v17.1, therefore the same software is meant to be used and Altium only provides support for embedded placed components.

In terms of comparison between standard technology and the ECT, using embedded placed components allows for a more fair comparison since standard components are used, in fact the same components used in the current version and, since one of the objectives of this project is to provide a comprehensive view of the technology, a good comparison base have to be established.

3.2 Design workflow

There are multiple approaches and ways to achieve size reduction using ECT. Following, the methodology and each step of the new design is described in detail.

3.2.1 Optimization of the current design, without ECT

The *HiGaN* v2.2 has final square board dimensions of 150 x 150 mm which is very compact and surely fulfill one of the objectives of the project that was to design a highly compact microinverter. Although, there are still some points where space saving improvements could be made. Therefore, the first step of the new design was to analyze the current version, looking for those possible improvement points and try to optimize it regarding space either by changing components or footprints.

In Figure 22 some examples of modifications made are highlighted. As can be seen the input EMI filter inductor, the transformer and the DC link capacitor bank are the most bulky components. The plastic plates of the EMI filter inductor and transformer occupy more space than the components themselves, this is due to modifications in the design of those components without modifying the plates. In fact the use of those plates

was reevaluated and there is no need to use them. Therefore the components footprints could be reduced, saving space.

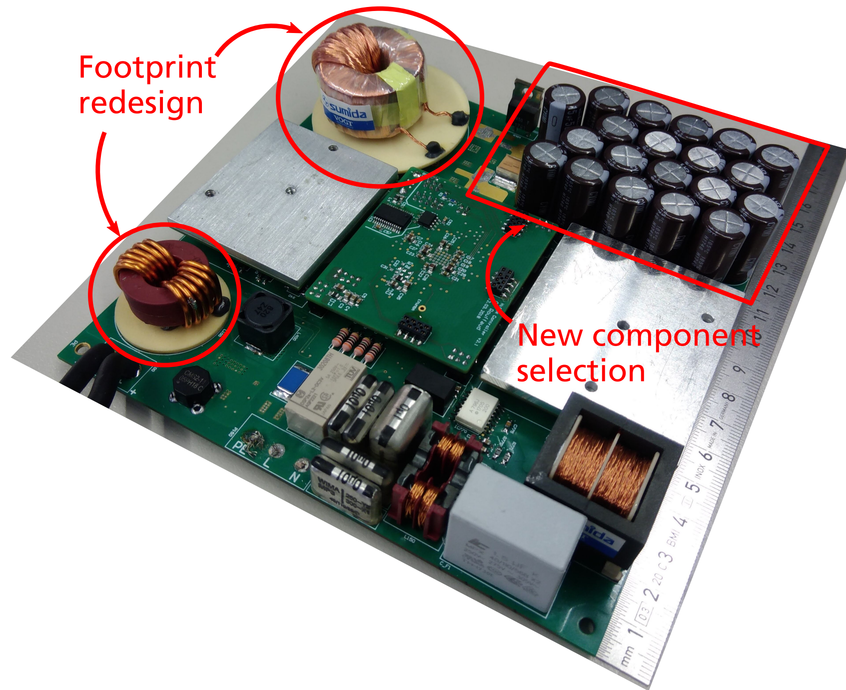


Figure 22 – Examples of modifications in the current design to optimize space.

As mentioned, the DC link capacitors occupy a huge portion of the board's area, in fact around 3542 mm^2 or approximately 16% of the total area. This is a 300 μF capacitor bank and this capacitance is achieved using twenty 15 μF Nichicon UCY2H150MHD capacitors in parallel conferring a very low total ESR (Equivalent Series Resistance). Therefore another options of capacitors combinations were evaluated. The options can be seen in Figure 23.

Parameters	Solution					
Combination	20x 15uF UCY2H150MHD	2x 150uF ESG157M500AQ5AA	2x 150uf 380LX151M500A012	1x 300uF ALA8DA301CF500	1x 300uF ALA8DA301DD500	1x 300uF ALS80A301DA500-ND
Diameter (mm)	12.5	22	35	30	35	36
Length (mm)	25	45	25	50	40	52
Area occupied vertically mounted (mm²)	3542	968	2450	706.9	962.1	1017.9
Area occupied horizontally mounted (mm²)	-	1980	1750	1500	1400	1872
ESR (Ω)	-	-	0.5225	0.6874	0.7802	0.706
Temp. Rating (°C)	105	105	85	105	105	105
Ripple Current (mA)	220	1020	1290	1990	1520-2970	2200 - 5200
Tolerance (%)	20	20	20	20	20	20

Figure 23 – Comparison of possible DC link capacitors combination.

The selection was made based on the requirements presented in Section 3.1. From Figure 23 the capacitors used in the current version have a height/length of 25 mm, exceeding the height requirement. The combination using two KEMET ESG157M500AQ5AA 150

μF capacitors mounted horizontally seems to be the most attractive option and fulfill the requirements. The capacitor selected can be seen in Figure 24. The mounting of the capacitor on the board is discussed in Section 4.1.

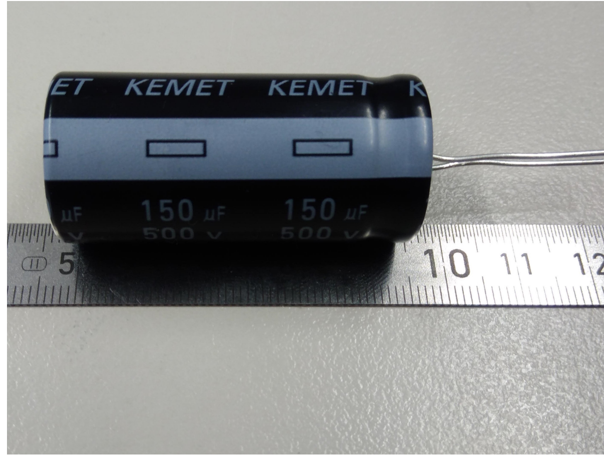


Figure 24 – KEMET ESG157M500AQ5AA 150 μF @500V 22 x 45 mm capacitor.

In the current design the input and output are meant to be connected using screw connectors. Although, in the final assembly, those connectors weren't used and the input and output cables were directly soldered on the board. This makes possible to reduce the footprint required for the input and output connections, saving space. Another component selection modification was the use of an alternative shunt resistor on the current measurement circuit. Currently the SMV-R056-0.5 from Isabellenhütte is used. The new selection, Vishay WSHP2818R0500FEA, has the same characteristics but with a smaller footprint.

3.2.2 Selection of components to be embedded

As discussed in the Section 2.6 the selection of components to be embedded must be done carefully, particularly in the case of prototypes. In the *HiGaN* motherboard there are some critical and also optional passive components, therefore those were selected to be placed in the outer layers of the board.

The components not embedded are the optional filtering capacitors in the measurements circuits, high value resistors at the input of the measurement circuits (those have large footprints), the DC link discharge circuit resistors (again, large values and critical functionality, potentially problematic), NTC sensors, and passives that exceed 2 mm in height in order to constrain the PCB thickness, generally high value ceramic capacitors.

The rest of the SMD passive components were selected to be embedded. In Figure 25 the highlighted areas show where most of the components selected to be embedded are in the current version of the *HiGaN*. As can be seen, the components are basically concen-

trated in the center of the board and compose mostly the measurement circuitry and the logic power supply circuitry.

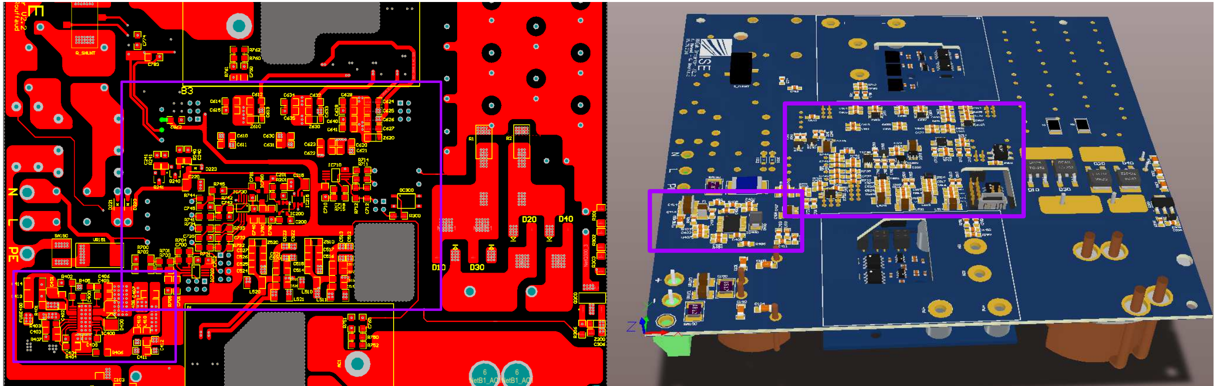


Figure 25 – Areas in the current version of the design containing most of the components selected to be embedded.

3.2.3 Altium Designer configurations

In order to design the board using Altium Designer software there are some modifications and additional configurations to be made compared to a standard PCB design.

The first change is to modify the footprint libraries. In Altium it is possible to place components in any signal layer, therefore if a component is placed on an inner layer this component is embedded. Depending on the component dimensions it is necessary to define a cavity that accommodates the whole component body inside the inner layer with clearance. In fact, most manufacturers recommend to define cavities for all footprints, although for the software, there is no difference whether a cavity is defined or not, only if embedding with open cavity is required.

To design a cavity in the footprint library editor first a region with the outer dimensions enough to fit the component with clearance (the XY cavity clearance is generally a design rule provided by the manufacturer) must be placed. Then this region have to be configured as in Figure 26. The parameter *Kind* must be changed to "Cavity definition" and in the parameter *Layer* a mechanical layer must be assigned. The parameter *Height* must be set to the suitable component height plus clearance.

Since the component will no longer be in the outer layers there is no need for the component's outline and designator to be in the top or bottom silkscreen, or as named in Altium, top and bottom overlay. Nevertheless, the outline and designator still need to be present in the design due to the manufacturing and assembly process. Therefore, the component outline must be relocated in a mechanical layer (generally the same mechanical layer assigned in the cavity definition). In Figure 27 the differences between a standard footprint and the embedded component footprint is presented.

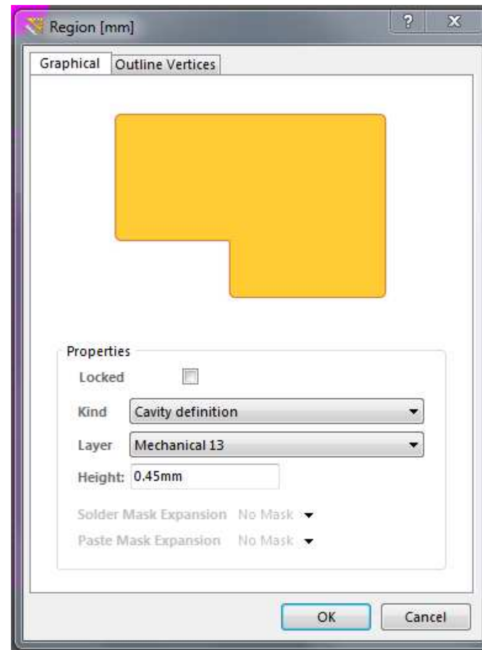


Figure 26 – Parameters to define a cavity in the Altium Region modification dialog.

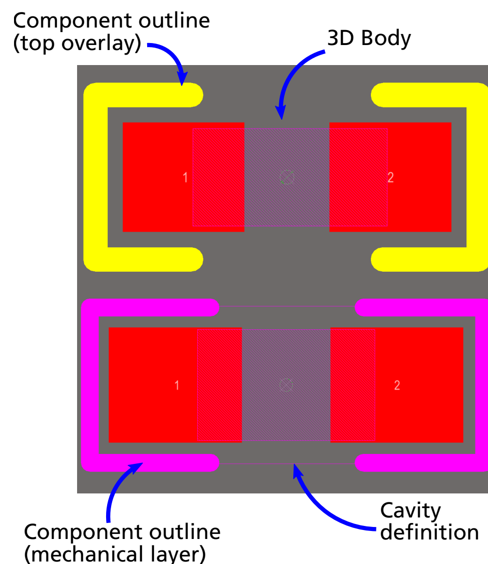


Figure 27 – Differences between standard component footprint and embedded component footprint.

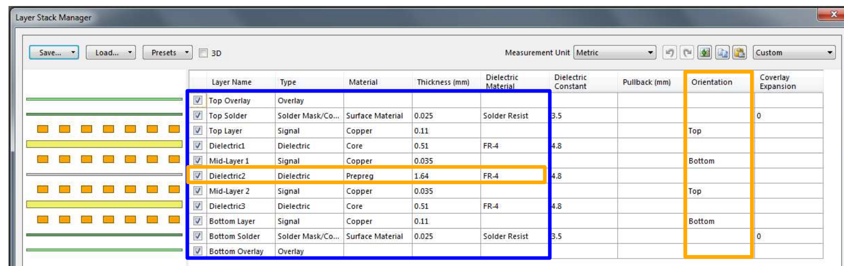
In Altium the overlay layers are special type of layers and the top and bottom overlay layers are linked in a way so that in a standard footprint there is no need to define the overlay art for both top and bottom. When, in a standard design, the component is switched from top to bottom layer (or vice versa), the overlay is reassigned automatically. Although, in the case of embedded components, since the outlines are now in a mechanical layer, if there are different layers with embedded components, the outlines won't be reassigned automatically.

To solve this, a mechanical layer pair must be defined. When the pair is defined, the

software can automatically relocate the outline in the different mechanical layer defined. This is a point to carefully pay attention since it is crucial for the assembly process. If not done correctly, there is a risk of a component to be placed in the wrong position or even in the wrong layer during manufacturing. A mechanical pair is defined in the PCB editor and the first layer of the pair must be the layer chosen to have the outline in the component library.

One important remark is that, up until the latest version of Altium, there is no support to define solder paste and mask regions in inner layers automatically. A workaround is to assign two new mechanical layers with this purpose and specify to the manufacturer. This is only needed if the method of component attachment in the inner layers is done using solder joints. Another point is that the component 3D body placed on the footprint must always be in the top side, otherwise the cavity definition won't fulfill its purpose.

Once the new footprints are defined, the next configuration is the layer stack. There are multiple ways to configure an ECT layer stack and the possibilities rely on manufacturer capabilities. Independently of the layer stack type to be used, there are some common points to be adjusted in the Altium *Layer Stack Manager*. In Figure 28 the highlighted areas show the configurations that must be done.



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.025	Solder Resist	3.5			0
Top Layer	Signal	Copper	0.11				Top	
Dielectric1	Dielectric	Core	0.51	FR-4	4.8			
Mid-Layer 1	Signal	Copper	0.035				Bottom	
Dielectric2	Dielectric	Prepreg	1.64	FR-4	4.8			
Mid-Layer 2	Signal	Copper	0.035				Top	
Dielectric3	Dielectric	Core	0.51	FR-4	4.8			
Bottom Layer	Signal	Copper	0.11				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.025	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Figure 28 – Different alterations in the Altium *Layer Stack Manager*.

As can be seen the thickness of the dielectric material that the components will be surrounded by must be enough to accommodate the height of all components to be embedded in the corresponding layer. Another point that is usually not used in standard designs is the orientation of the components in the inner layers. Those aspects depend on the layer stack being used. For the particular configurations showed, the layer stack is illustrated in Figure 29.

To verify if the component is correctly placed on the board (e.g. if the dielectric layer thickness is enough or the component is in the right orientation) is possible to use Altium *3D Mode*. Generally if the component's 3D body wasn't placed correctly on the footprint, when placed on the board, the component will appear in the wrong orientation and the cavity will not be visible in the right position. Furthermore, the layer stack manager will create a managed layer stack automatically to try to resolve this aspects automatically.

To illustrate this situation Figure 30 presents a simple board with two embedded capacitors in different layers and the difference between the correct and wrong 3D body

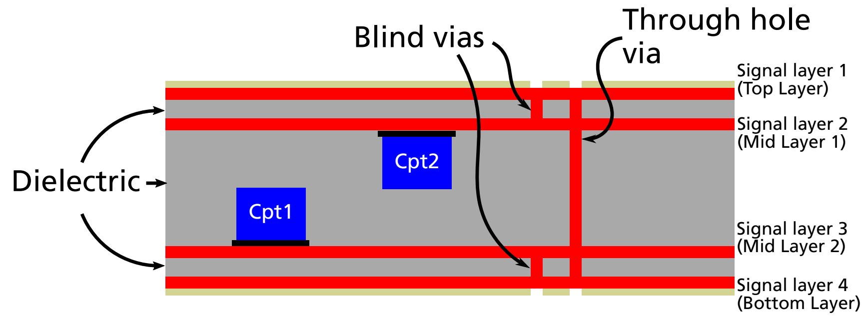


Figure 29 – Example of ECT layer stack.

placement. As is possible to see, if the component body is placed incorrectly the cavities will be in the wrong direction, and in practice will be useless. The layer stacks of each configuration are seen in Figure 31. When the 3D bodies are placed incorrectly regarding the mechanical pairs the software generates an extra managed layer stack (in this particular setup) when in fact there must be only one, with the prepreg removed by the cavity definition.

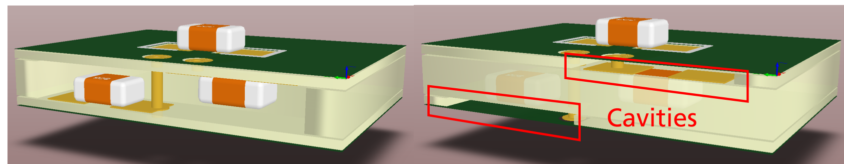


Figure 30 – The effect of the footprint 3D body placement. Correct placement (left) and wrong placement (right).

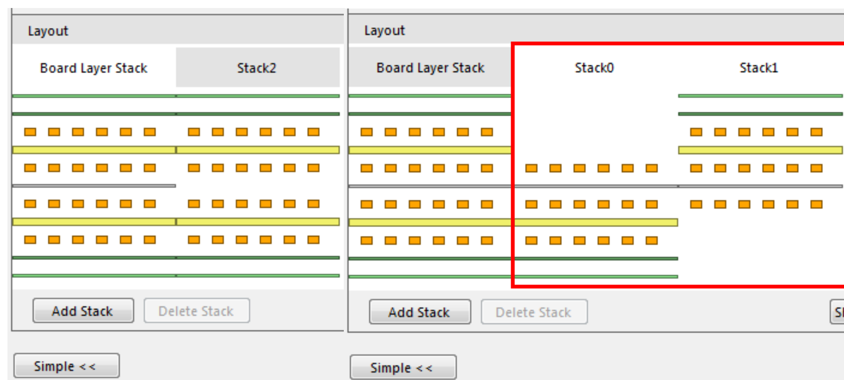


Figure 31 – Generated layer stacks for different 3D body placement. Correct layer stack (left) and incorrect layer stack (right).

If the dielectric thickness between two layers is too small there might be the need of creating an exception in the component placement design rule (if active), because the software evaluate the distance between components in all directions and disregards the fact that the components in different layers are separated by a dielectric layer and have different orientations.

3.2.4 Size reduction approach

After all configurations in Altium and regarding every requirement the new design was started. Analysing the current version of the *HiGaN* motherboard and considering the selection of components to embed as seen in Figure 25 is possible to note that there is more opportunity for size reduction in the vertical axis (Y axis).

That's because the components on the board's left hand side cannot be changed and the layout is already well optimized. It is also difficult to modify the components layout in the right hand side due to the need of large copper tracks since the high current in this part of the board. Another reason is that, with the new DC link capacitors, and the way they will be mounted (horizontally) already saves space in the Y axis. Moreover, the DC-DC converters ICs used to supply the power modules gate drivers can be simply rotated by 90°and space can be saved in this direction. This is illustrated in Figure 32.

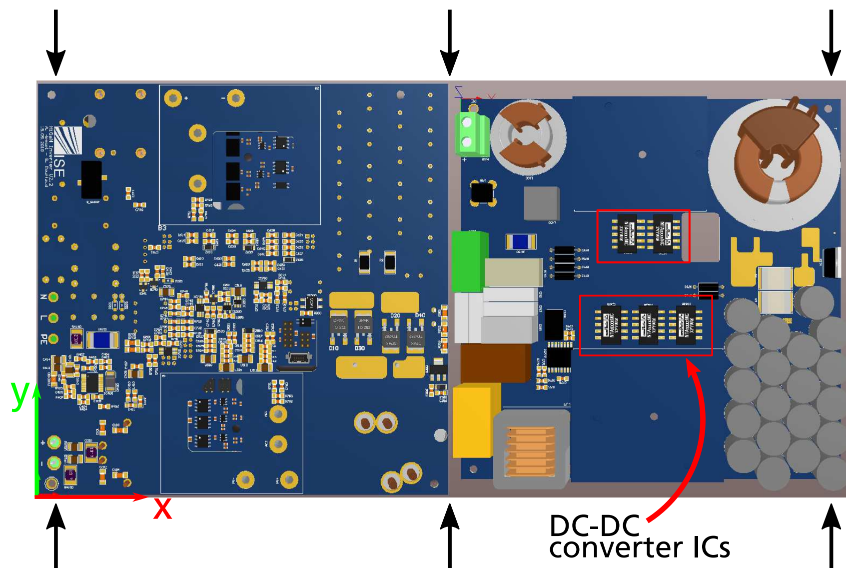


Figure 32 – Size reduction approach used illustration.

The motherboard's central area can be defined as a region where there is only low power signals and can be seen in Figure 33. Currently, this area measures approximately 73 x 54 mm, 3942 mm^2 or about 17.5% of the total area.

As seen in Figure 25 the above mentioned area contains most of the components to be embedded, thus, supposedly, a greater area reduction can be achieved in this area. Furthermore, there is opportunity to increase density and by doing so freeing space needed in other areas to relocate circuits in order to reduce the size in the Y axis.

The central region contains, in the top layer, most part of the measurement circuits, circuitry for the DC-DC converters operation, a relay actuation circuit and part of the DC link discharge circuit. The same area on the bottom side contains the DC-DC converters ICs, part of the measurement circuits and most importantly, the connectors for mounting the microcontroller module.

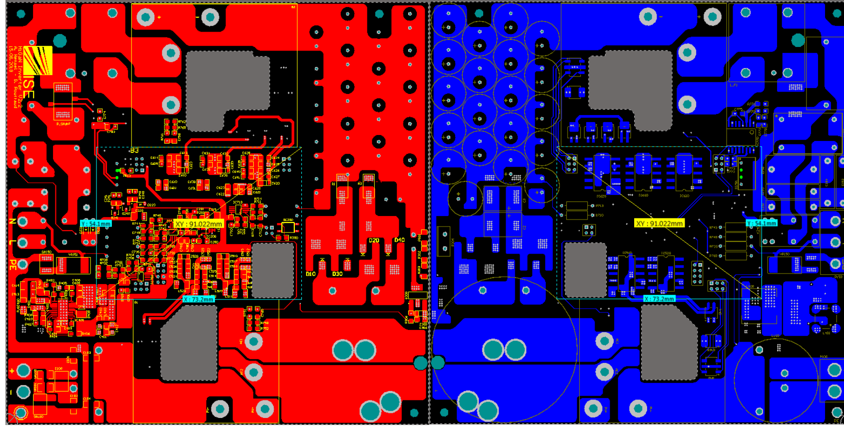


Figure 33 – *HiGaN* motherboard's central area. Left: top layer. Right: bottom layer.

In order to comprehend the particularities of relocating circuits and design a new layout is important to briefly understand the functionality of the circuits mentioned. To better understand the circuits, refer to Figure 6 where a block diagram of the system is presented.

- *Measurement circuits.* There are six circuits responsible for measuring signals of interest. To measure voltage a classical voltage adder operational amplifier circuit is used with the MCP6282 op. amp. The voltages measured are the DC link voltage, the output or mains voltage, the input voltage and the LCL output filter voltage. To measure the output current the sigma-delta (Σ - Δ) optically isolated modulator ACPL-796J is used. This integrated circuit uses sigma-delta modulation to sample analog input, storing the data as a density of ones to transmit across the isolation and then decodes and streams a high speed digital signal [64]. This IC is ideal to be used with low-level analog input provided by shunt resistors, as in the case of the motherboard. There is also two temperature measurement circuits, using NTC (Negative Temperature Control) resistors, but those circuits are used to measure the temperature of the power modules and therefore aren't in the central area of the board.

- *DC-DC converters.* In order to supply very stable and isolated power to the power modules gate drivers ICs the NTA0303MC dual output DC-DC converter is used. In total there are five of those chips and each one has a ripple rejection additional circuitry consisting of coupling and filtering capacitors, inductors and a Zener diode. All circuitry is found on the board's central area.

- *Relay actuation circuit.* The *HiGaN* prototype contains a grid disconnection system in order to isolate the inverter from the grid when not in operation and in case of failure. This system works using the TPS3836 voltage supervisor. The chip monitors the logic supply voltage and has an inverted output or $\overline{RESET}$ output, meaning

that as long as the supply voltage is below the threshold voltage (2.93 V [65]) the output is active-low state. In the *HiGaN* the chip supply voltage is constant and the manual reset ($\overline{MR}$) pin is used. Since the supply voltage applied, 3.3 V (above the trheshold), is fixed, to change the output state it's only a matter of switching states of $\overline{MR}$ pin, and this signal is an output of the microcontroller. Since the chip's output is active-low, the signal passes through an inverter and finally drives the gate of a MOSFET that actuate the relay. The relay used is the DSP2a-L2-DC3V and switches both the inverter's line and neutral connections. The components of this circuit contained in the central area of the board are the ICs mentioned and all the auxiliary passive circuitry, and an energy buffer circuit, that stores enough energy to actuate the relay in case of failure.

- *DC link discharge circuit.* This circuit is used to discharge the DC link capacitor bank. It is a safety measure since the energy stored in the capacitors remains for a long time after the device's shutdown if not properly discharged. The principle of operation is basically using a series of large value resistors (in the range of Mega ohms) to reduce the time of discharge of the capacitor bank. This circuit is activated using MOSFETs with the gate signal being provided directly by the microcontroller. The only part of this circuit on the central area of the board is an optocoupler precisely to provide the gate signal with proper isolation between the high voltage circuit and the low signal part.

The microcontroller module is a PCB with external dimensions of 58 x 49.5 mm and it is mounted on the motherboard using header connectors in a "flat" configuration. Therefore its footprint is the whole area of the board, 2871 mm^2. This module can be altered and, in order to save space in the Y axis, the way the board is mounted have to be modified in such a manner that the largest dimension in the Y axis is the overall thickness of the PCB.

To summarize:

- The reduction will be made in the Y axis.
- The central area of the board, which will have most of the embedded components, will be used to relocate circuitry in order to make the reduction.
- The microcontroller module must be redesigned to occupy less space in the Y axis.

3.3 Comparison and selection of PCB manufacturers

As described in previous sections there are multiple different embedded placed components processes provided by different companies. Therefore each manufacturer has

different capabilities and thus different design rules and guidelines. This can make the task of finding the right manufacturer difficult and time consuming and in the process several modifications in the design might have to made.

With that in mind, before redesigning the whole motherboard there was a need to acquire a good database on the manufacturers availability and capabilities. Therefore a research was made in order to first find manufacturers that provide the embedded placed components technology in their portfolio. In Table 2 a list with the manufacturers found that are probably suited for the eventual fabrication of the prototype and basic information about their PCB manufacturing capabilities is presented. As a disclaimer the information presented in Table 2 is available publicly in the companies' website.

Manufacturer	**Max. # Layers**	**IMS Cores**	**Flex. PCB**	**HDI**	**Thick Copper**	**PCB + Heatsink**	**Prototype**
Andus Electronics	14	✓	✓	✓	✓	✓	✓
AT&S	28	✓	✓	✓	✓	×	✓
ILFA	32	×	✓	×	×	×	✓
Micro Systems Technologies	20	✓	×	×	×	×	✓
Schweizer AG	18	✓	×	✓	✓	×	?
Würth Elektronik	20	✓	✓	✓	✓	✓	✓

Table 2 – List of selected manufacturers and their capabilities

Although there's a fairly big amount of companies that provide the ECT, Table 2 presents only the ones that seamed most interesting for this project regarding capabilities and location. All companies in the list, except for Schweizer AG (Switzerland), are based in Germany.

In order to have a good idea of cost and average production times and to gather technical information about design rules and guidelines the board files have to be provided to the manufacturer. Since this first contact was being made in the very beginning of the project, the new motherboard design still didn't exist, therefore to gather the desired information a microcontroller module with embedded components was designed.

This new microcontroller board was basically a redesign of the current module used in the *HiGaN* v2.2. It must be stated that there is no connection whatsoever between this design and the new microcontroller module to the motherboard final design (see Section 4.1 and Section 4.4). The idea was simply place all the passives in the inner layers of the board. Since this module has much less components than the motherboard and there weren't any special requirements, it wasn't too much time consuming.

The microcontroller used in the module is the Texas Instruments TMS320F28075 is a 32 bit, 120 MHz, 512 kB digital signal processor MCU [66]. In this particular module there are no external clock circuitry. The communication is made using the FTDI FT232RL that is a USB to serial UART interface with data transfer capability of 3 baud to 3 Mbaud [67]. There is a Mini USB type B connector on board that provides both power for programming and communication. The power input is galvanically isolated. Version 2.1 (current) has external dimensions of 58 x 49.5 mm (2871 mm^2). A comparison between the current design and the ECT design can be seen in Figure 34.

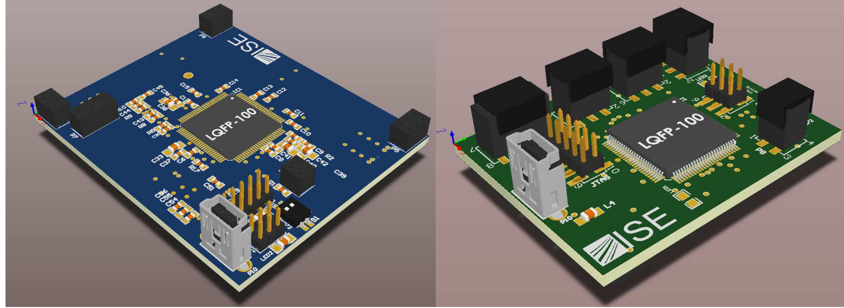


Figure 34 – Controller module v2.1 (left) compared with Controller module v2.1.1 (right).

In the new design the only component change were the header connectors, replaced by their SMD counterparts (in version 2.1 those connectors are THT). The final dimensions of the design using ECT (version 2.1.1) are 36.6 x 46.4 mm (1698.24 mm^2). Therefore a size reduction of approximately 41% was achieved. Of course, it is not fully fair to compare the area of both boards due to the connectors positioning that has a specific configuration to fit the motherboard, even though, it is an interesting result by itself.

Each company have its own embedding process and specific design rules. In general terms, the design rules are the same as for a standard technology with minor modifications in dimensions and clearance requirements. Following there is a summary of the feedback provided by the manufacturers contacted.

- The layout of the embedded components have to be made in small groups of components. This is required by the majority of manufacturers due to resin flow issues as will be discussed in Section 4.2
- If the embedding process uses solderless attachment methods generally only copper termination components can be used due to the conductive adhesives used. This a common requirement in standard lead free PCB manufacturing as well.
- If there is embedded components in different layers, the components cannot be directly above each other, in other words there must be a horizontal distance between the components. This only valid for the inner layers, components in the outer layers can be directly above embedded components. This requirement is due to the pressing process, because the pressure between components during this process can cause permanent damage.
- There is a variety of layer stack capabilities and this is one the most important information that must be acquired before the start of the design. Among other aspects, the layer stack defines the drill pairs possible and therefore it has a huge impact in the way routing is done because of the vias placement and use.
- There must be more clearance between through hole vias and components than usual. This is due to the via drilling process. The drilling of through hole vias is

done after the components are embedded, therefore the components can be destroyed if there is not enough clearance.

- One information that is not usually found in the BOM (Bill of Materials) of standard PCBs is the component's height. This is information is crucial for the manufacturer in order to check if the embedding of certain components and the layer stack desired are feasible.
- As discussed in Section 3.2.3 the components outline and designators must be placed in a mechanical or construction layer and this layer should be plotted only once in the fabrication files. This is required by the manufacturer due to assembly reasons. Some manufacturers also require pick-and-place data.

The information listed above is crucial for the development of a new prototype because the board designed have to be feasible by the manufacturers. Also some of those requirements are directly tied to good design practices in PCB development and provides good results overall.

The costs of the ECT will be discussed in details in Section 4.6. Even though, from this first contact was possible to understand immediately that this technology is expensive in the prototype level and this is the reason that realization of the prototype wasn't possible in this project.

4 Results and Discussion

In this Chapter the realized designs of the new versions for the *HiGaN* motherboard are presented. The design process is presented and the results in terms of size reduction and overall data on the design is shown. A comparison between the boards is also presented. A deeper analysis of the cost of the ECT is provided based on quotations of the boards designed with the manufacturers cited in Section 2.

Several versions of the motherboard design were made in order to have different configurations to be evaluated and analyzed for future projects. This way, the task to choose the best suited option is less time consuming.

4.1 *HiGaN* version 3.0.1

The very start of the design, regarding software procedures, was to copy all files from version 2.2 to a new location, then these files were renamed and the changes were done directly on them. This is easier and less time consuming than start a new board file, for example, because good part of the layout was kept. The configurations described in Section 3.2.3 were made in this stage as well. This same procedures were repeated for all versions designed.

In terms of files, the HiGaN v.2.2 is a ten files PCB project being eight schematics documents and one PCB document. The project is hierarchical, meaning that each schematic respect a sequence from the "father" document, this way the project is better organized and there is no need to redefine nets in different schematics. This project uses five custom component libraries.

In version 2.2, the power components layout and the connections are very well optimized and follow strict design rules, therefore only minimal changes were made in this regard.

The first steps in the design of version 3.0.1 were to make the modifications described in Section 3.2.1. The most significant change is the DC link capacitors and for that a new submodule was designed. This new module or extra board was developed in order to mount the capacitors selected horizontally with a decent mechanical strength. The module is presented in Figure 35 where is possible to see the two connection pads. This kind of mounting/connection is widely used in the so called 3D designs and fits perfectly for the purpose of this project. The PCB itself is standard and have only two layers.

When the modifications without ECT were done the next step was to, change the layers of the components selected for embedding to inner layers and start the new layout considering the approach described in Section 3.2.4. All versions designed uses the layer

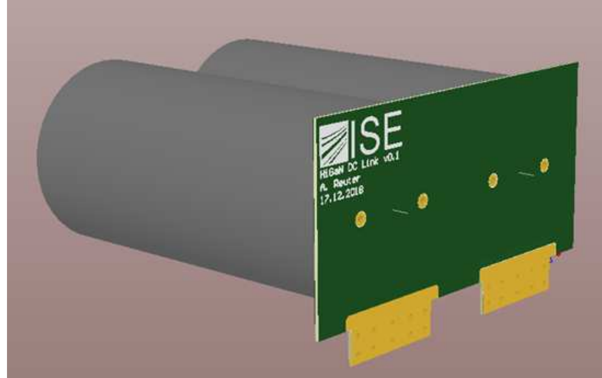


Figure 35 – DC link capacitors submodule.

stack presented in Figure 29.

In order to save space using the embedded components, the layout was made in such a way that the components are placed directly underneath the active components on the surface, this also reduces the trace length. In this version an attempt was made to somewhat divide the embedded components evenly between Mid Layer 1 and Mid Layer 2 but since the drill pairs possible (refer to Figure 29) and because the Top Layer have most of the active components, Mid Layer 1 ended with more components than Mid Layer 2.

Although most of the components selected to be embedded are in the central area of the board as described in Section 32, the logic supply circuit is on the board's left hand side as it is possible to see in Figure 25. This logic supply circuit is based on the Texas Instruments LM5576 switch mode power supply IC which is a buck converter regulator, with an adjustable voltage output and a wide input range (6 V to 75 V). In the *HiGaN* the circuit's input is the main non regulated input voltage (in practical operation the output voltage of a PV module), the output is fixed at 3.3 V and the current the IC provides is 3 A.

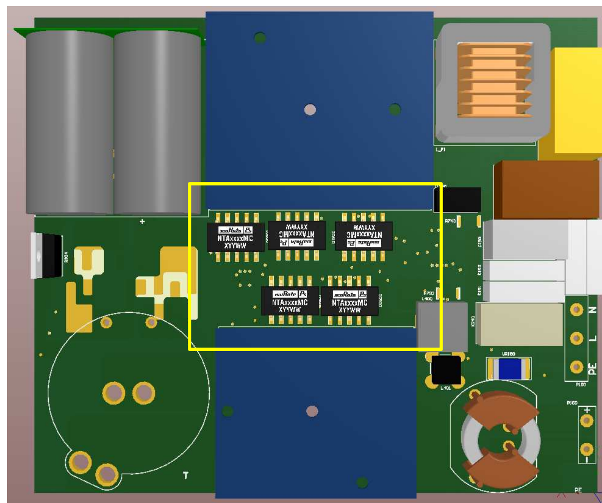


Figure 36 – Space suitable for mounting the new microcontroller module defining the design dimensions requirements.

This circuit supplies all logic circuitry on board including the microcontroller module, therefore it is crucial for the functioning of the board. Another important aspect is that, since it is a switching element, the layout have to be made carefully to avoid EMI issues. The location of this circuit in version 2.2 basically prevents size reduction in the Y axis, therefore all circuitry had be relocated to the center of the board and that was a key change in the design in order to achieve a meaningful size reduction.

The design sequence was made disregarding the microcontroller module, therefore when all the layout on board was done it was possible to understand the design requirements for a new microcontroller module. Figure 36 shows a screenshot of the unfinished design and highlights the area left after the layout which is suitable for the new microcontroller module. The length of the highlighted area is approximately 70 mm. It also has the cutout present in version 2.2 removed, this cutout serve as access to the microcontroller module's interfaces.

With the constraints defined the *HiGaN* Controller v3.0 module was designed. The result is seen in Figure 37. The board is mounted vertically on the board using 90°angled, double row, THT header connectors. There is one connector in the top layer and one in the bottom to fit the space available and give more mechanical stability to the board. The main modification compared to version 2.1 in terms of components was the USB connector, previously being a vertical THT Mini USB type B and now a horizontal SMD Micro USB type B.

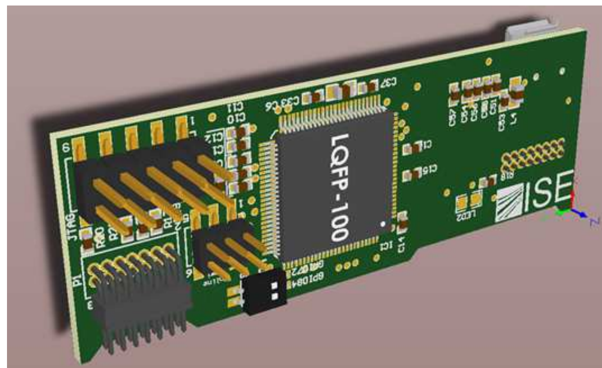


Figure 37 – *HiGaN* Controller v3.0.

The dimensions of this module are 23.1 x 65 mm and an estimated thickness of 11 mm. Thus, hence the way the module is mounted on the board, the footprint has an area of approximately 960 mm^2 (calculating as a box containing the whole board's body), allowing for a somewhat not too complex routing. The module's height when mounted fulfill the height requirement staying below 24 mm. Besides the size reduction, this new module also allows for a better heat dissipation of the DC-DC converter ICs, because now it lets free air flow in the vertical direction.

The final result of the HiGaN v3.0.1 can be seen in Figure 38 and Table 3 presents overall information of the board. To calculate size reduction the formula presented on

Equation 4.1 is used.

$$S_r = 100 \cdot \left(1 - \frac{A_x}{A_{2.2}}\right) \tag{4.1}$$

Where S_r represents the size reduction percentage (%), A_x is the area of the version being compared and $A_{2.2}$ is the area of version 2.2.

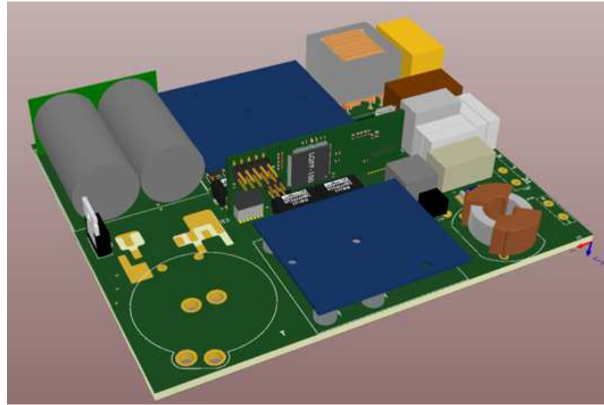


Figure 38 – *HiGaN* v3.0.1.

Parameter	**Value**
Dimensions (mm)	150 x 126.41
Area reduction	15.7%
Total number of components	213
Total number of embedded components	106
Number of embedded components in Mid Layer 1	59
Number of embedded components in Mid Layer 2	47

Table 3 – Information on the components and size reduction of the *HiGaN* v3.0.1.

The area reduction in this version was 15.7% which is already a good result for a highly compact board that is the *HiGaN* v2.2. This size reduction was provided mainly by the use of ECT and the new modules designed. The central area of the board was reduced by approximately 42% and the component density in this area was increased.

In Figure 39 the highlighted areas shows that there are empty spaces on the board indicating that is possible to achieve an even higher reduction. This is basically because it's impossible to even approximate the DC-DC converters ICs in the center area of the board without violating a clearance rule set between those components, furthermore there must be enough clearance between the power modules and the converters in order not to compromise the assembly.

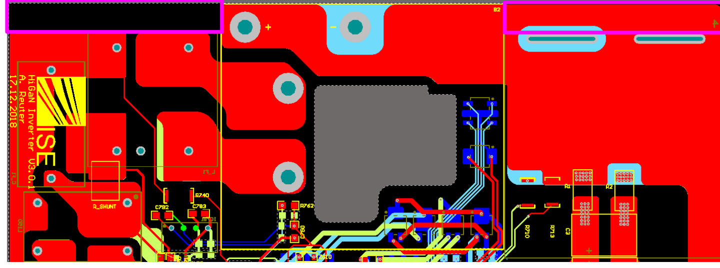


Figure 39 – Empty areas in the *HiGaN* v3.0.1.

4.2 *HiGaN* versions 3.0.2 and 3.0.3

As discussed previously, there was still opportunity for size reduction in version 3.0.1, though it is a solution by itself, therefore another version of the motherboard was designed.

The main bottleneck in size reduction is the central area of the board, specifically the DC-DC converters ICs. Those have a large footprint (15.24 x 11.2 mm), process a considerable amount of power (1 W) to be near signal tracks, are galvanically isolated using a transformer, thus EMI is an issue and the clearance must be kept in order to conserve a reliable power supply for the gate drivers on the power modules.

A new submodule was designed to accommodate the DC-DC converter ICs. This module can be seen in Figure 40. It is mounted the same way as the *HiGaN* Controller v3.0, using angled header connectors. This module contains the ICs and all circuitry used to its operation. It has dimensions of 70 x 24 mm and the its footprint occupies approximately 728 mm^2 on board. The board is a standard four-layer PCB. Two layers are used only for ground and supply voltage planes in order to shield the board as an attempt to reduce the EMI generated by the ICs.

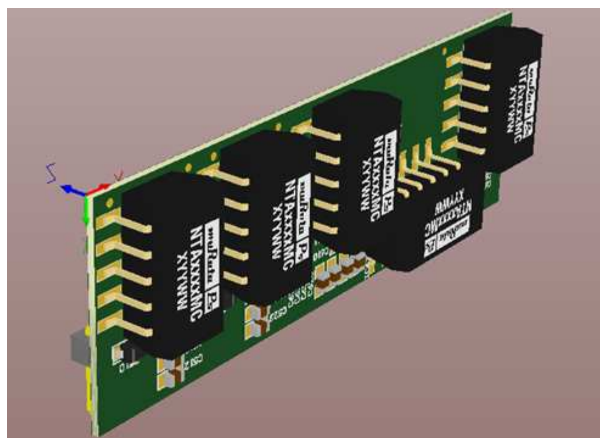


Figure 40 – *HiGaN* DCDC Breakout v0.2.

This module allows to reduce the central area even more and thus save the space left empty in version 3.0.1. Furthermore it also reduces the component count on the motherboard allowing for more functionality in the same area or a cleaner and more optimized layout.

The final result of the *HiGaN* v3.0.2 is depicted in Figure 41 where is possible to see how the new module is mounted as well. Table 4 presents overall information of the board.

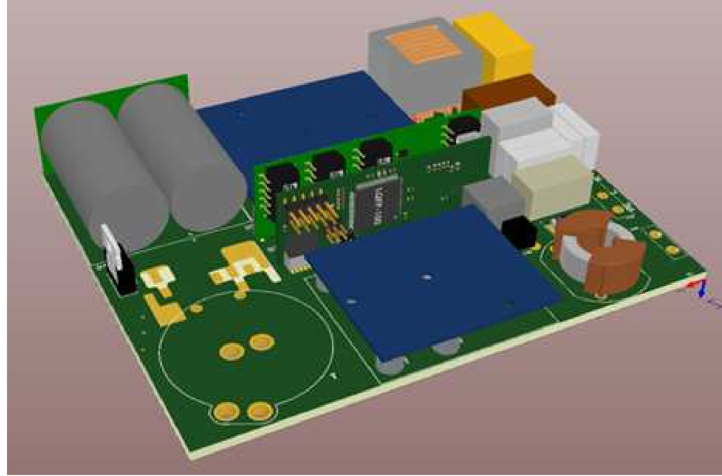


Figure 41 – *HiGaN* v3.0.2.

Parameter	**Value**
Dimensions (mm)	150 x 120.91
Area reduction	19.4%
Total number of components	156
Total number of embedded components	58
Number of embedded components in Mid Layer 1	51
Number of embedded components in Mid Layer 2	7

Table 4 – Information on the components and size reduction of the *HiGaN* v3.0.2.

The area reduction in version 3.0.2 is 19.4%, 3.7% more savings compared to version 3.0.1. The central area was reduced by approximately 54% compared to version 2.2, which is above 10% more reduction than version 3.0.1. Of course, in this version the main size reduction vector was the new submodule designed.

In version 3.0.2 there is more free space in the inner layers as well as in the top layer, so in a hypothetical situation where active components are to be embedded, there is opportunity for that, thus it is possible to add functionality within the same form factor.

In Figure 42 a comparison between the central area of the board in Mid Layer 1 (yellow) and Mid Layer 2 (blue) of versions 3.0.1 and 3.0.2 is presented. The free space is clearly seen, although there is a small area concentrating most of the embedded components in Mid Layer 1. This happens because most of the op. amps. from the measurement circuits are in this area (on the top layer) in order to have shorter tracks coming from the power area.

Depending on the process of embedding the placed components and the manufacturer capability it is not possible to have a large group of components clustered. This is due

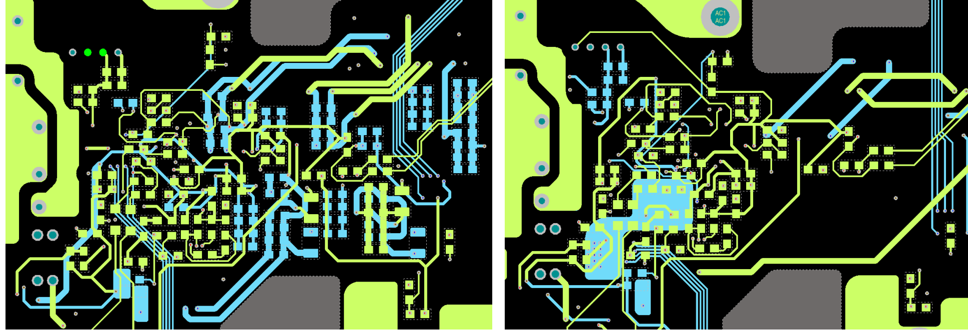


Figure 42 – Comparison between the inner layers of the *HiGaN* versions 3.0.1 (left) and 3.0.2 (right).

to how the cavities in the prepregs are milled. In most cases it is not possible to mill a cavity for one single component, because of a variety of reasons (milling machine limitations, space between components, prepreg material, etc.). Therefore a larger cavity, that accommodate a group of components, is milled.

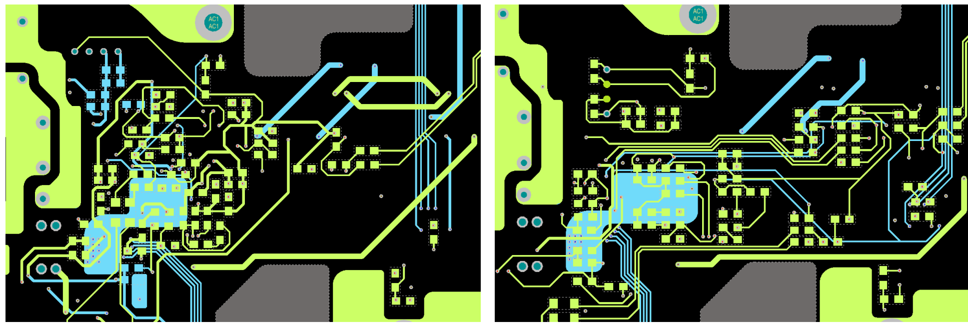


Figure 43 – Comparison between the inner layers of the *HiGaN* versions 3.0.2 (left) and 3.0.3 (right).

The cavity size to component size ratio, in case of one single component, does not affect the embedding process, meaning that the cavity can be completely filled with no voids [62]. However for more than one component in the same cavity the resin flow can be uneven and leave voids or air bubbles and in the further pressing process this could ruin the board completely. Therefore, most manufacturers set as a design rule, that the layout must be done in such a way that the embedded components are organized in small groups with a minimum distance between those groups.

To fix this issue, *HiGaN* version 3.0.3 was designed. It is exactly the same board as version 3.0.2 with no further modifications other than the layout of the embedded components aiming small separated groups. A comparison between the inner layers of version 3.0.2 and 3.0.3 can be seen in Figure 43. A consequence of the new layout is that in version 3.0.3 there is no more components in Mid Layer 2. Routing on this version was much more complex due to component positions, although it results in a much more cleaner and comprehensive layout.

The results regarding area reduction are the same as in version 3.0.2. It is expected that version 3.0.3 should be more accepted by the manufacturers in terms of feasibility. Depending on the manufacturers capabilities, there might not exist issues with the clustering of embedded components and eventually this could make for a good comparison between methods. That's the reason why a separated version was designed.

4.3 *HiGaN* version 3.0.4

Although as mentioned in Section 3.1.1 the power sub modules (DC-DC and DC-AC converter modules) weren't going to be modified, this version of the design was an attempt to integrate the modules to the motherboard and evaluate if this is a good opportunity to size reduction and overall system improvement. Therefore, first, it's important to understand some basic characteristics of the power sub modules.

4.3.1 The *HiGaN* power sub modules

There are two power sub modules used in the *HiGaN*, the input and output modules, as seen in Figure 44.

The DC-DC converter or input sub module, is a 52 x 44 mm six layer PCB with a thickness of only 1.2 mm. The board contains only the four transistors and the gate drivers circuits of the DC-DC converter explained in Section 1.3. The gate driver used are Analog Devices ADuM4121 which is an galvanically isolated gate driver. The switches used are the GaN Systems GS61008P which are gallium nitride transistors rated to 100 V, 80 A. These transistors have a very low drain to source resistance ($R_{DS(ON)}$ of only 7.4 mΩ at 25 °C. GS61008P is the bottom cooled version meaning that the thermal pads for heat dissipation are in the bottom side of the package. This module processes a low voltage (the inverter input, between 20 V to 50 V) but a high current, up to 15 A.

The output sub module or the DC-AC converter is a similar board being 59 x 51 mm with the same amount of layers but only 1 mm thick. In this module the the Silicon Labs Si8610BC-B-IS digital isolator is used to provide galvanic isolation between the signal input and the power part and the Texas Instruments UCC27511A-Q1 is used to drive the gates of the GaN Systems GS66508P 650 V, 30 A, 50 mΩ $R_{DS(ON)}$, bottom cooled gallium nitride transistors. This module processes a higher voltage than the DC-DC module with its input voltage being the DC link voltage, up to 350 V.

Both modules are connected to the motherboard the same way, using header connectors for the digital switching pattern signals and power connectors for their input and output. Those are highly special products due to the number of layers (six) and the very low thickness of the PCBs. The thermal management is done using an aluminum plate glued in the bottom side of the board occupying the whole area to maximize heat dissi-

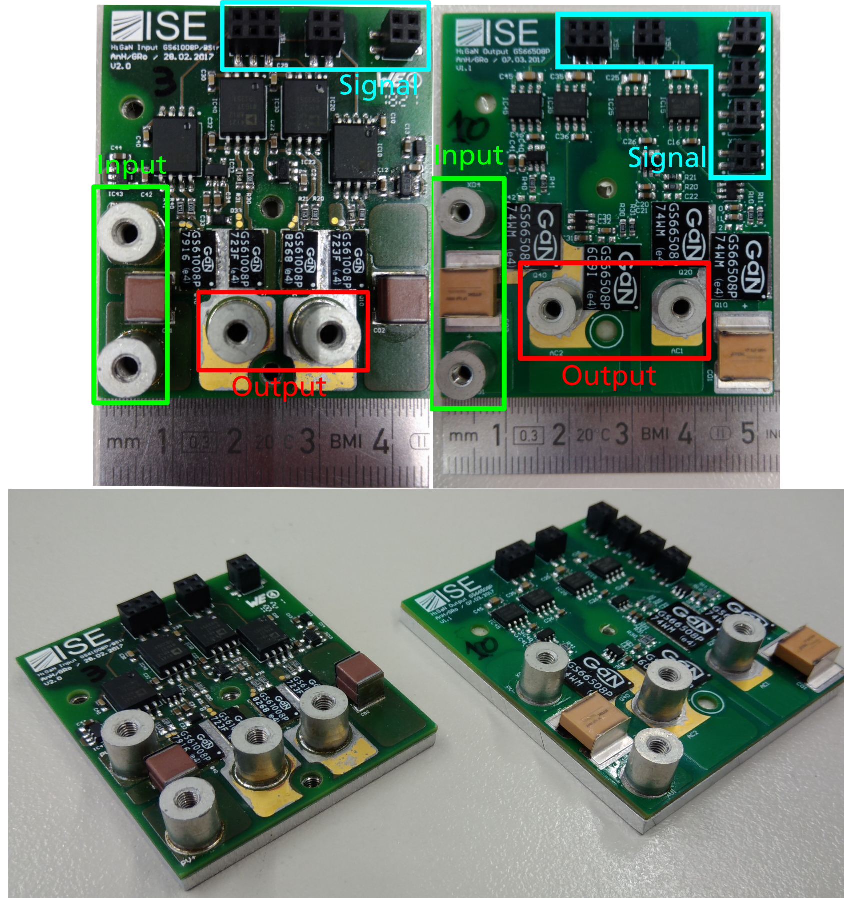


Figure 44 – Power sub modules. Input module (left) and output module (right).

pation. The thermal pads of the transistors are connected to the heat sink using thermal vias arrays.

The components layout on the modules is symmetrical in order to have a better charge balancing. Six layers are used in the modules due to the current processed and the way the components are disposed.

There are some aspects that make the idea of using modules in this project very attractive. The GaN transistors used are very thin devices (0.45 mm for the GS61008P and 0.51 mm for the GS66508P) making the handling quite difficult. In order to use these devices in their maximum performance, very good soldering have to be performed, this, together with the handling difficulty, makes the process of using the devices directly on the motherboard a very hard task.

Besides, since the HiGaN is a prototype, although now already functional and without the need of components modifications, in the process of fine tuning its functionality and configuring the circuits the power devices are more likely to present malfunction or sometimes be completely destroyed in the process, making it necessary to replace the components. But as discussed, this can be a very hard and time consuming process so instead, replacing just a module is more efficient.

It also important to note that the power modules aren't exclusively used in the *HiGaN*

prototype, but instead are a self contained, independent board and it are used by multiple different projects.

4.3.2 The integration of the modules to the motherboard

The footprint of the modules is exactly their area (2288 mm^2 and 3009 mm^2 for the input and output modules respectively) and their positions on board were kept basically the same through all the versions designed. In fact, only the position of the output module in the Y axis was changed. The polygons used to make the power connections were also kept the same, with slight changes in shape, because those were extensively optimized in version 2.2.

To integrate the modules on the motherboard first the components had to be removed from the PCB document. Then the schematics of the modules were added to the project and the PCB document was updated with the new components. The only change in the schematics were the removal of the header and power connectors, the rename of certain nets in order to be compatible with the whole project and the rename of the components so that there wasn't any conflicts between documents since the project is hierarchical. To follow the design requirements described in Section 3.1, only the passive components were embedded.

One of the main technical difficulties of integrating the sub modules on the motherboard is that the board has only four layers but the modules have six. This requires a different layout and the design of thicker tracks. Another issue is that there must be free space in the bottom layer to accommodate a sufficient heat sink, ideally the same as used in the modules. In order to do the integration, the cutouts present in version 2.2 at the modules area, used to reduce the board's weight and improve isolation, were removed.

As there is less components and more flexibility to layout particularly the low power circuits form the modules it was possible to make relocation of some components on the motherboard and hence achieve size reduction. It was possible to free space in the lower part of the board due the use of the embedded components in the gate driver circuits because they got more compact and thus it was possible to move the circuits towards the center of the board. This enable to take more advantage of the smaller footprints designed for the transformer and EMI filter inductor, moving those components by a small factor also towards the board's center.

The final result was a motherboard 4% smaller than version 3.0.3 and with two less modules. The design of the *HiGaN* version 3.0.4 can be seen in Figure 45 and basic information about the design are presented in Table 5. As seen in Figure 45 one of the corners of the board is chamfered, this was possible due to the new transformer position and saves approximately 3.4% of surface area.

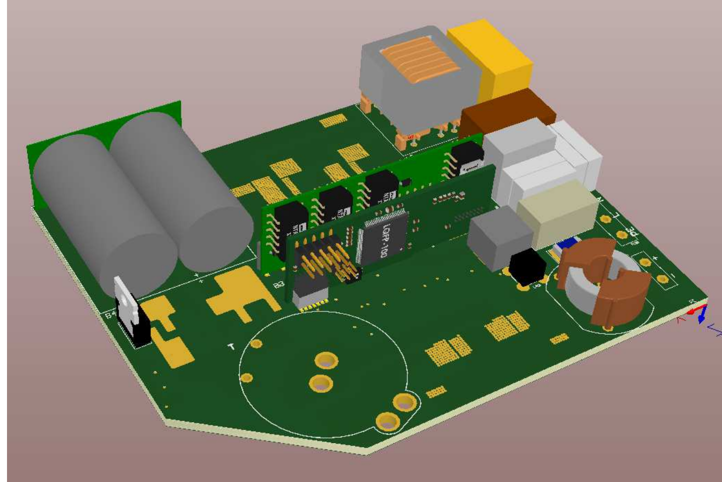


Figure 45 – *HiGaN* version 3.0.4.

Parameter	**Value**
Dimensions (mm)	150 x 118.9
Area reduction (not considering chamfer)	20.7%
Total number of components	236
Total number of embedded components	93
Number of embedded components in Mid Layer 1	93
Number of embedded components in Mid Layer 2	0

Table 5 – Information on the components and size reduction of the *HiGaN* v3.0.4.

4.4 *HiGaN* version 3.0.5

As exposed in Chapter 2 the ECT has been used mostly in low power applications, where there's use of a high quantity of active components with large footprints but with small volume and, overall, the passive components are much smaller (much less bulkier) than those used in power electronics applications. Since in this project the use of extra module showed to be a very interesting solution to size reduction, it's worth to investigate the application of the ECT to the modules.

In Figure 45 it is possible to see that the microcontroller module and the DC-DC converter breakout board occupy all space available in the X axis on the central area of the board, therefore reducing the size of the modules would result in a substantial reduction on the motherboard. Another point is that it would be a more direct way to compare the application of the ECT in low signal and power electronics PCBs.

In this sense a new design of the microcontroller module and the DC-DC converter breakout board using the ECT was made. The objective is to achieve at least 3.5% of size reduction compared with version 3.0.4, which is the surface area the chamfer applied in version 3.0.4 saves. The chamfer is a good solution to save surface area on the PCB but when a case for the board is fabricated, is technically more difficult to build the chamfer and could be also more expensive, therefore the case would most likely be fabricated

without it, losing the whole purpose. That's why the objective is to achieve at least the same surface area savings but with a rectangular form factor.

Also, the integration of the power sub-modules in version 3.0.4 increased the space in the central area on the bottom side of the board, allowing for the modules to have a higher width and consequently a new layout can be realized.

The aim in the modules new design is to reduce the size occupied in the X axis, or in other words, reduce the modules length. In version 3.0.4 the reduction in the Y axis reached a feasible limit from the point view of designing in such a way that more reduction could compromise signal integrity and isolation properties and the routing of the connections would be very difficult or impossible.

The new design of the microcontroller module is seen in Figure 46. The main modifications in version 3.1, besides the use of ECT, were the relocation of the USB connector, now facing the side edge of the board and RS232 to USB converter IC is now on the opposite layer of the digital isolator, making the whole interface circuitry more compact, but still preserving galvanic isolation. Another significant change is the use of smaller header connectors because in version 3.0, connectors with unused extra pins were applied to enforce the mechanical stability of the board, but since version 3.1 is smaller this became a less critical issue.

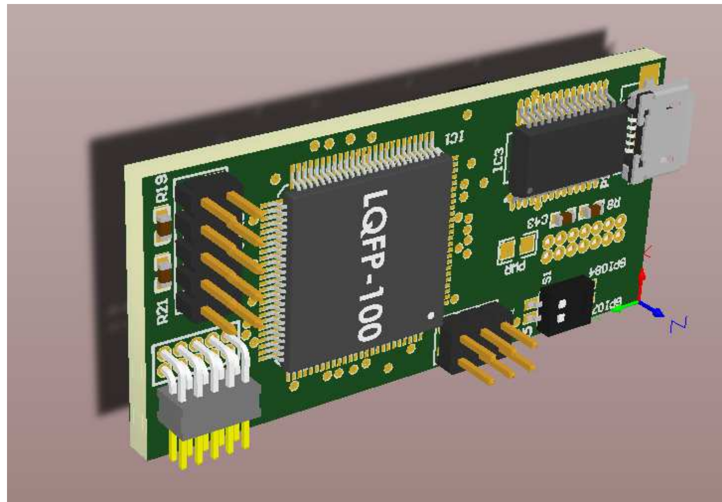


Figure 46 – *HiGaN* Controller v3.1

Version 3.1 has final dimensions of 21.6 x 46.52 mm or 1004.8 mm^2 meaning a size reduction of 65% related to the microcontroller module used in the *HiGaN* v2.2 and 33% compared to version 3.0. A more detailed comparison is presented in Section 4.5.

The new design of the DC-DC Breakout module is seen in Figure 47. Compared to version 0.2 the only changes are the connectors, now using THT header connectors that are directly soldered to the motherboard in order to keep the module's height under 24 mm and the position of the DC-DC converter ICs, which in the previous version were all

in the bottom layer, thus increasing the width of the module, but this is acceptable due to the reason explained earlier.

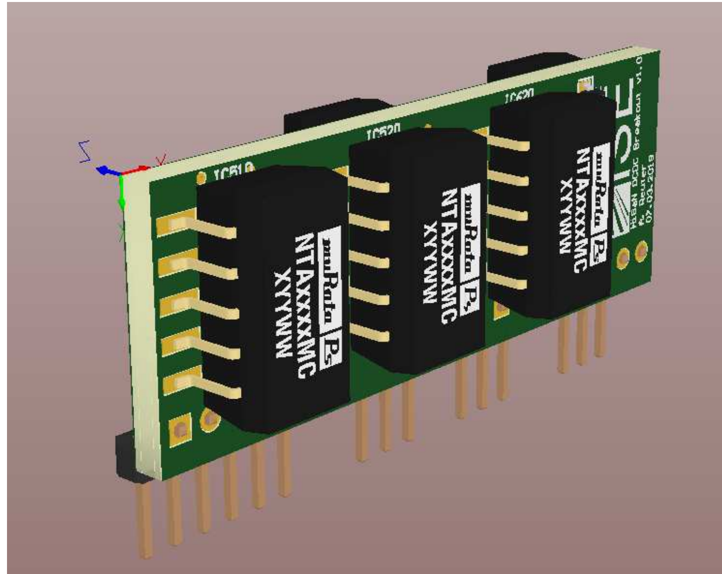


Figure 47 – *HiGaN* DCDC Breakout v1.0

Version 1.0 has final dimensions of 53 x 19.2 mm or 1017.6 mm^2 meaning a size reduction of 39.4% compared to version 0.2.

Applying the new modules to the motherboard, it was possible to realize new layouts for certain circuits in order to reduce the size. The most significant change was the new positions for the input and output inductors of the logic power supply circuits as is possible to see in Figure 48. This actually improves the circuit as the inductors are closer to the IC, reducing the current loop and thus minimizing the generation of conductive EMI. This also allowed the input and output capacitors to be properly separated, improving the isolation.

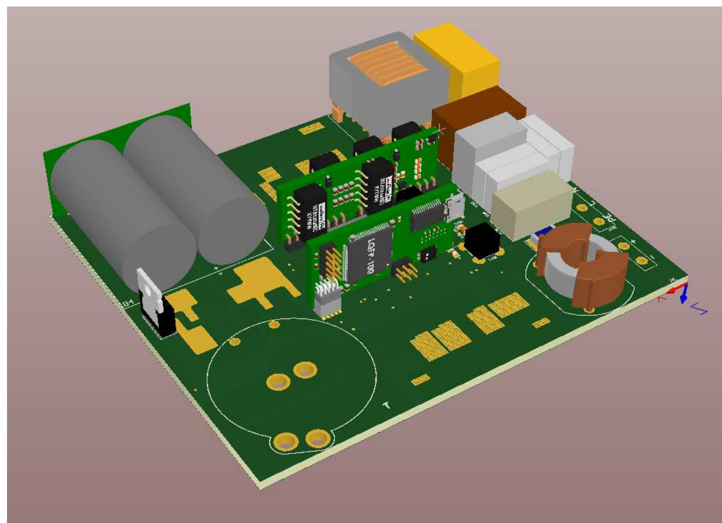


Figure 48 – *HiGaN* version 3.0.5.

The disadvantage of the new version is that the galvanic isolation of the gate drivers from the power converters is not as effective as in version 3.0.4 due to the new position of the DC-DC Breakout board. This could bring undesirable effects to the switching patterns of the power transistors. Nevertheless, since the galvanic isolation wasn't critically compromised, this version could be an interesting alternative and overall a good comparison base.

The final dimensions of version 3.0.5 are 137.9 x 118.9 or 16396.3 mm^2, meaning 27.1% of size reduction compared to version 2.2 and 8% compared to version 3.0.4, over two times more reduction than the primary objective. The reduction was achieved only in the X axis, as expected.

4.5 Comparison of all the designs realized

In previous sections a detailed description of new designs of the *HiGaN* inverter was presented. In this section a comparison between all the designs realized is discussed. Not only the motherboards designed are included in this comparison but all the other boards and modules developed. It is valid to compare boards with different functionalities and requirements in order to evaluate where the ECT can be most effectively used.

The comparison is shown in Table 6 which contains the data about the motherboard designs and Table 7 containing the data for the submodules designed. Here, since only passive components were embedded, the total number of passive components is shown.

Board	**Dimensions**	**#Passive Components**	**Component density (cpt./mm^2)**	**#Embedded Components**	**Embedded to Passive components ratio**	**Area reduction**	**Volume Reduction**
HiGaN v2.2[1]	150 x 150 x 30.8 mm 22500 mm^2 693000 mm^3	190	0.0103	0	0	-	-
HiGaN v2.3[2]	150 x 150 x 30.8 mm 22500 mm^2 693000 mm^3	124	0.0069	0	0	0	0
HiGaN v3.0.1	150 x 126.41 x 30.6 mm 18961.5 mm^2 580221.9 mm^3	172	0.0112	106	61.6%	15.7%	16.3%
HiGaN v3.0.3	150 x 120.91 x 30.9 mm 18136.5 mm^2 560417.9 mm^3	124	0.0086	61	49.2%	19.4%	19.1%
HiGaN v3.0.4	150 x 118.9 x 31.9 mm 17835 mm^2 568936.5 mm^3	178	0.0132	93	52.2%	20.7%	20.5%
HiGaN v3.0.5	137.9 x 118.9 x 31.9 mm 16396.3 mm^2 523042.3 mm^3	178	0.0144	92	51.7%	27.1%	24.5%

Table 6 – Comparison of all boards designed and the original versions (motherboards).

[1] Current version of the motherboard, not designed in this project
[2] Refer to Section 4.6

Board	Dimensions	#Passive Components	Component density (cpt./mm^2)	#Embedded Components	Embedded to Passive components ratio	Area reduction	Volume Reduction
HiGaN Controller v2.1[3]	58 x 49.5 x 14 mm 2871 mm^2 40194 mm^3	70	0.0303	0	0	-	-
HiGaN Controller v3.0	23.1 x 65 x 15.3 mm 1501.5 mm^2 22972.9 mm^3	70	0.0539	0	0	47.7%	42.8%
HiGaN Controller v3.1	21.6 x 46.52 x 12.5 mm 1004.8 mm^2 12560 mm^3	70	0.0806	55	78.6%	65%	68.8%
HiGaN DCDC Breakout v0.2	70 x 24 x 11.3 mm 1680 mm^2 18984 mm^3	48	0.0375	0	0	-	-
HiGaN DCDC Breakout v1.0	53 x 19.2 x 15.2 mm 1017.6 mm^2 15467.5 mm^3	48	0.0619	48	100%	39.4%	18.5%

Table 7 – Comparison of all boards designed and the original versions (modules).

The height of the boards designed, as well as the volume, is an approximation using the 3D model provided by Altium and only serves as demonstration purposes, real dimensions may vary.

On the motherboards design, the reduction in volume is affected by the change of layers of certain components. For example, changing the ceramic capacitors of the DC link from the bottom layer to the top layer, increases the overall height of the design and thus less reduction in volume. In the *HiGaN* v3.0.4 and v3.0.5 the ceramic capacitors from the output power sub module are integrated on the top layer as well, hence those are the tallest versions. Another aspect is the increased thickness of the PCB due to the embedded components.

The *HiGaN* version 3.0.1 has the highest component density and embedded components count, it also does not make use of the DC-DC breakout board, therefore the main size reduction vector is indeed the ECT. It is also worth stating that this version uses the *HiGaN* controller v3.0, which is a standard board, making this version the closest to the original *HiGaN* v2.2.

Version 3.0.3 has the smallest component density of all, although having achieved a considerable area reduction, hence in this version, the vector of reduction is clearly the use of the DCDC brakout module. Nevertheless, the use of the ECT in this case allowed a cleaner layout and routing and most importantly, is possible to increase functionality in the same space, due the free areas in the outer layers. Version 3.0.4 has the power sub-modules integrated but it is essentially the same board as version 3.0.3. The low component density of version 3.0.3 and the integration of the power modules allowed a new layout and modifications in the power path resulting in more size reduction. As discussed in Section 4.3 the integration of the sub-modules could bring potential functional issues and one noted during the design is that the galvanic isolation of the gate drivers is

[3]Current version of the microcontroller module used, not designed in this project

not as effective as in the other versions due to the layout and component proximity.

Version 3.0.5 uses the sub-modules with embedded components. In this version the size reduction vector is a fusion between the use of extra modules and the ECT, because the modules now have been reduced due to the use of embedded components and this is reflected on how much size reduction was achieved on the motherboard. As a result this version is the smallest and it has the highest component density of all motherboards designed. The issues mentioned for version 3.0.4 are also present in version 3.0.5.

If the objective is only and exclusively size reduction, version 3.0.5 would be the right option to realize. However, considering the issues mentioned, version 3.0.3 seems to be more attractive. Even though as will be seen in the next section, version 3.0.1 would be the least expensive option in prototype level since it only needs one extra module.

It would be reasonable to expect that the quantity of embedded components is directly proportional to the size reduction achieved. However from Figure 49 is possible to see that there is no clear proportional relation between the size reduction and embedded components. In the case of the motherboard designs, the opposite happens, version 3.0.1 has the most embedded components but the least size reduction. This is obviously due to the use of the sub-modules.

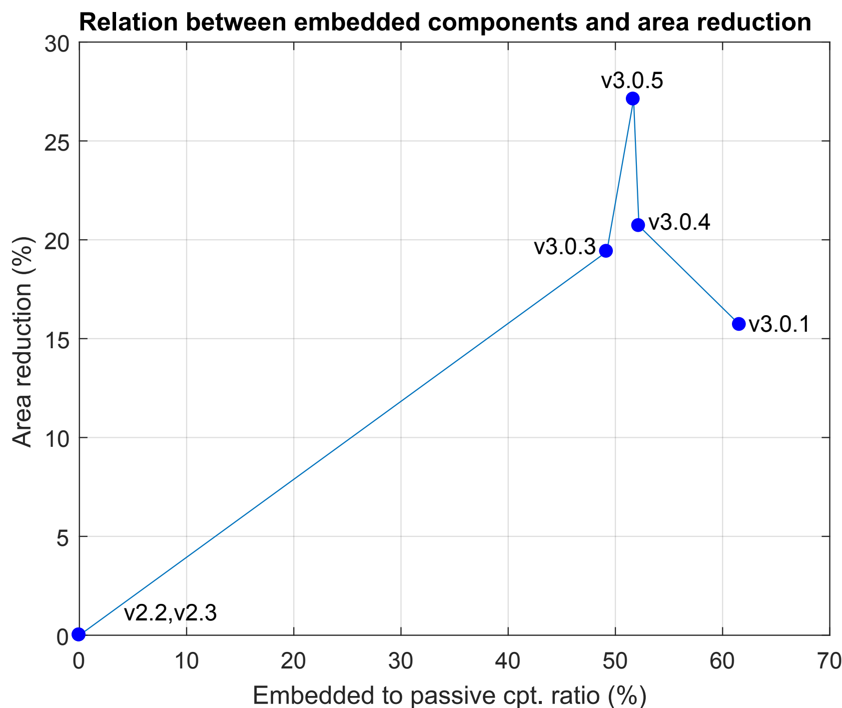


Figure 49 – Area reduction versus embedded components for all motherboard versions.

Figure 49 not only shows that a direct comparison between the motherboard versions is difficult due to the different configurations but also that using embedded passive components to achieve size reduction is more suited for low power processing PCBs. From Table 7, the size reduction achieved on the microcontroller and the DC-DC breakout

modules is substantially higher compared to the motherboard designs and it is almost completely due to the use of the ECT. This was already expected and it's in congruence with the exposed in Chapter 2.

Although there are multiple variables, this can be explained due to the type of components and requirements of each type of board. In boards like the modules, the overall volume of all components is small, and when considering only passive components (which were embedded), the volume is even smaller, because almost every passive component used is SMD and processes very low power. The isolation requirements are more easily fulfilled as well, because only low voltages and low currents are being carried on the traces hence the level of interference is lower. Therefore, more passive components can be embedded, consequently the component proximity increases yielding more size reduction.

On the other hand, on higher power processing boards, as the inverter motherboard designs, there is a considerable amount of bulky components, such as inductors, transformers, large capacitors, etc. Besides, the voltages and currents processed are higher requiring good isolation between inputs and outputs and between power lines and signal lines. Another point is that the active and electromechanical components count is higher than in boards like the microcontroller module, therefore as only passive components were embedded, there is less opportunity to take advantage of the ECT in this sense.

The graph presented in Figure 49 allows to clearly see that the use of sub modules are a good solution for size reduction for the *HiGaN* prototype and when the ECT is also applied to those modules, as in version 3.0.5 (Section 4.4), the size reduction achievable is fairly substantial. This result also shows that in order to further reduce the size of the *HiGaN* microinverter using ECT it would be necessary to embed also the suitable active components.

4.6 Costs of the technology

Regarding the aspects discussed in the previous section, version 3.0.3 was chosen to be quoted with the manufacturers listed in Section 3.3. At first, only one unit of the motherboard was quoted without the additional modules needed. From all manufacturers contacted only two accepted to make an offer for the prototype. This happened due to various reasons, usually availability, but also the design complexity, for example.

Table 8 presents the offers by the manufacturers that replied. This information is sensible and is only available under request, therefore the name of the manufacturers that replied is preserved.

It is possible to see that there is a considerable difference between the manufacturers. This is due to a number of factors, from the methods used, through equipment and supply chain to size of the companies.

Manufacturer	Initial costs (€)	Unit cost (€)	Total cost (€)	Delivery time (days)
A	1140.00	195.00	1335.00	42 - 46
B	1320.00	1068.82	2388.82	No time specified

Table 8 – Costs of the *HiGaN* motherboard version 3.0.3 by different manufacturers.

Although very different prices, both companies have similar manufacturing methods (basically a variation of the ECP process), which uses solder joint attachment, although manufacturer B provides other methods as well. Inclusively, the design rules and guidelines provided are similar, but manufacturer A is more flexible, having less constrained rules, more layer stack options and able to manufacture thicker PCBs. Nevertheless, manufacturer B is in the market of embedded components for a longer time and has more experience, guaranteeing the final PCB while manufacturer A disclaims and warns that the final product could be outside the client's specifications.

As described in Section 3.3 there are different requirements from each manufacturer. One of these requirements is that embedded components in different inner layers cannot be placed directly above each other. This really limits the layout possibilities and seems a major drawback. However, this is only true for certain layer stacks, most notably for 4 layer boards, which is the case for all the motherboard designs. This is rather interesting and makes possible to better understand the manufacturing process.

The reason why the components components in different inner layers cannot be placed directly above each other, according to manufacturers is that the pressure during the lamination process would cause excessive mechanical stress in the components and eventually cause them to completely break or present cracks in the body and/or the solder joint that gradually would ruin the functioning of the PCB.

This makes possible to assume that the whole manufacturing process is symmetrical. For a 4 layer PCB, for example, there would be two pre-laminated cores, which consists of pre-pressed layers of copper foil - prepreg - copper foil, with the inner layer components placed and fixed. Then, those two cores are laminated to form the full PCB. In this step the inner components would be practically in contact with only the cavity Clarence separating them.

Therefore, one can assume that the solution would be separating the inner layers that contains components with more cores. Such layer stack would be as presented in Figure 50. This would be feasible according to manufacturing A, although there is no information about in the design rules. With the design rules provided by manufacturer B is not possible to assume the same.

The layer stack presented would result in a 6 layer PCB and the additional layers could be used as ground (GND) and logic supply voltage (VCC) planes for example. This way three cores would be used. The first (according to Figure 50) would comprehend the top layer and signal layer 1; the second, the two planes and the third, signal layer 2

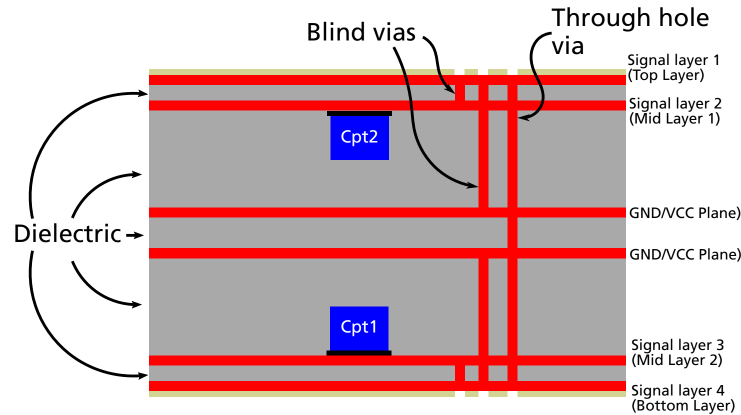


Figure 50 – Minimal layer stack in order to have embedded components above each other.

and bottom layer. The cores could be further laminated all together since the core with only the planes can be thinner and the thickness of the dielectric between the embedded components and the planes can also be smaller.

This would naturally increase the costs since there is more processes of lamination and obviously more layers, but it is a good alternative in really dense designs with severe space limitations.

Assembly is also one important aspect of the process and the methodology varies between the manufacturers. In the offer by A the assembly of the embedded components is made by the client. This is rather interesting to some extent because it allows to use very specific components or make adaptations during assembly. The downside is that it considerably increases production time since the panel has to be sent back to the company to finish the rest of the board. The offer by B, in the other hand, contemplates assembly by a third part company and one of the reasons why the initial costs are higher is that a special SMD stencil is needed to assembly the embedded components. That's also one of the reason why B doesn't specify the delivery times, because it depends on the components availability.

To fully comprehend the costs, a comparison with the standard technology is needed. For that the *HiGaN* v2.3, an adaptation of the *HiGaN* v2.2, was quoted. The only modification on the board was the use of the same sub modules, in order to have a fair comparison. The costs are seen in Table 9. This time a standard PCB manufacturer that provides quotations only based on the board specifications was added to the comparison, and it's called manufacturer C. This offers some kind of base or minimum price for this type of board.

As is possible to see, the prices of the standard technology are much lower, actually 70.6% smaller for manufacturer A and 38.1% for B. This can be explained because both manufacturers offer the ECT as a special technology, consequently it's already expected that the ECT would be a more expensive solution. Additionally, as discussed in Section 2.6.2, the companies have to modify their manufacturing layouts and make invest-

Manufacturer	Initial costs (€)	Unit cost (€)	Total cost (€)	Delivery time (days)
A	345.00	47.17	392.17	31 - 33
B	712.60	764.12	1476.72	No time specified
C	56.08	317.72	373.80	7

Table 9 – Costs of the *HiGaN* motherboard version 2.3 by different manufacturers.

ments in machinery and specialized personnel. Furthermore it is not a very commonly used technology, so the low demand also elevates the costs.

One important point to be noted is that, in both cases, manufacturer B offers the PCB with assembly included. As is evident in Table 9 the final cost of manufacturer B is substantially higher than manufacturer A, and the difference between the standard technology and the ECT is smaller for manufacturer B, indicating that the costs of the assembly process are a good portion of the total offer.

To have a wider economical view of the ECT, a large scale production analysis is also interesting. Therefore a quotation for a high volume (10000 pieces) production was requested. Only manufacturer B was able to provide an offer for the number of units required, manufacturer A stated that the ECT is still in development in their company and therefore only small scale is available. The comparison of the unit price of the standard technology and the ECT versus the quantity is presented in Figure 51.

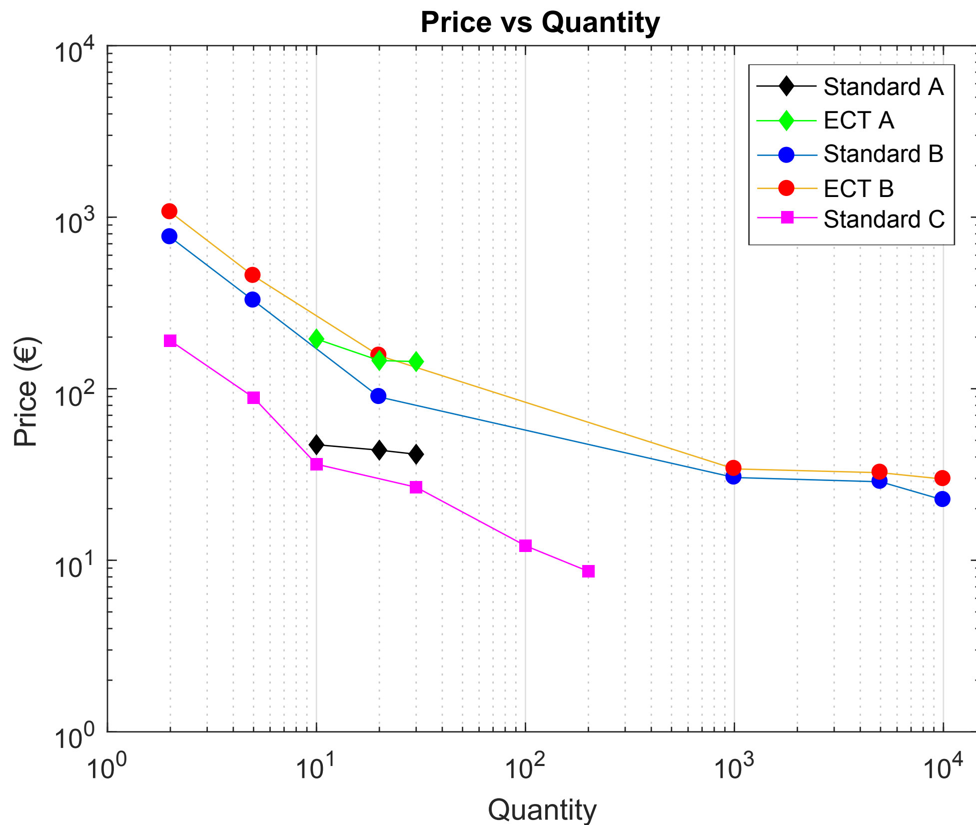


Figure 51 – Price comparison between different technologies and manufacturers.

It is possible to see that the ECT follows the same curve as the standard technology.

Although even for the maximum number of pieces, the standard technology is still over 24% cheaper than the ECT. This is a drawback since even with size reduction and consequently less material, the board using ECT is still more expensive than the standard technology.

By comparing the curves is possible to see that the costs of manufacturer A for both the standard technology and the ECT are much lower than manufacturer B and if compared to C, therefore is clear that there is a huge influence of the assembly costs also in larger scales.

In order to balance the analysis about the cost of the ECT, it is also interesting to keep in mind that the main purpose of the ECT is not particularly cost reduction for the final client. If analysing from the manufacturers point of view, it‘s actually the opposite. The ECT can be considered as a relatively new technology and it brings, among size reduction, multiple desirable features. This is in fact adding value to the product and therefore will naturally cost more to the final consumer.

In the stage of the technology at the moment, where it‘s not widely available and is mostly used by big corporations to manufacture their own products, it would be fair to say that, in economical aspects, the ECT is a very advantageous technology for the manufacturers, because it offers a way to deliver an added value product and still save material in large scale. However, for the consumer, meaning the entities, companies or individuals that need to use this technology and are dependent of the services provided by the manufacturers, the ECT is still not very economically attractive, especially in the case of prototyping.

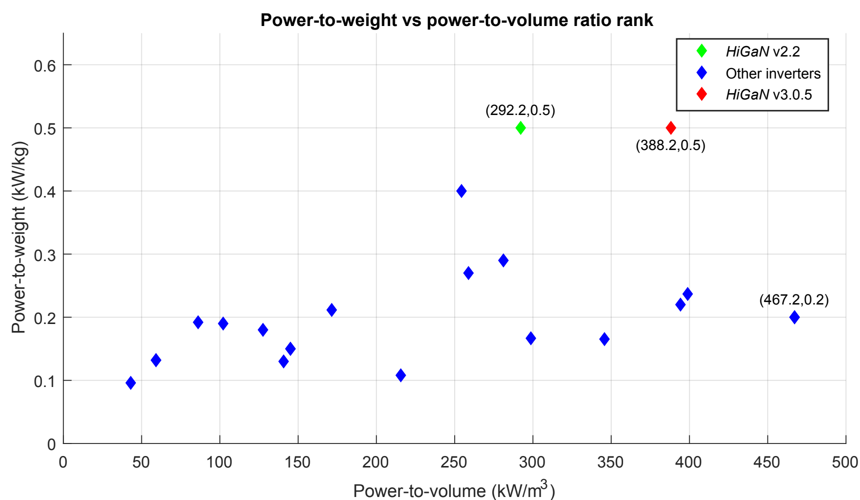


Figure 52 – Updated power-to-weight and power-to-volume ratio microinverters rank.

It’s valid to revisit the microinverters rank presented in Section 1.3 (Figure 7) adding the best result achieved in terms of size reduction, in this case version 3.0.5. The new rank is presented in Figure 52 and it considers a case for the new design with the same proportions of the one designed for version 2.2. The weight is considered to be the same,

since other modules are used, however, in reality, the realized board would be considerably lighter since it is smaller, uses less large electrolytic capacitors and also doesn't use the heavy power submodules. Nevertheless, for illustration purposes and since a displacement only in the X-axis was already enough to make the new version more competitive, the same weight is considered.

From Figure 52 it is clear that an improvement was made and the power-to-volume ratio is now in the range of the 400 kW/m^3. This increases the competitiveness of the prototype and besides the high manufacturing costs, it is definitely an interesting alternative.

5 Thermal behaviour of embedded power transistors

The advances in power electronics systems are increasingly requiring more power density and thus smaller packages that can withstand higher currents and higher voltages, have less thermal resistance and can efficiently switch at higher frequencies. Those are reasons why WBG semiconductors such as GaN and SiC devices are becoming more and more popular in power electronics applications [27] and also the case of study in the *HiGaN* project.

Thermal management in WBG semiconductors is currently a challenge. Although these devices have superior thermal conductivity, can operate under higher temperatures and have less issues with self heating due to higher efficiency, the cost of such transistors are higher and since the main reason to use them is miniaturization, the devices are often operated at their limits[27][68][69]. Therefore, to be able to take advantage of all the device's capability and performance, care must be taken in the design in order to allow for a well suited thermal dissipation system.

In the *HiGaN* project the power conversion steps are made almost completely on the power sub-modules as discussed in Section 4.3.1. As is possible to assume, these modules have to dissipate a lot of heat produced by the power transistors. Some of the design choices on the power sub-modules are almost exclusively an effort to optimize heat dissipation, for example the overall PCB thickness is only 1 mm in order to have a shorter path of which the heat have to be conducted, the board is constructed with a thick aluminum heat spreader which in turn is further attached to a heat sink on the case, the thermal interface material (TIM) is a special type with a very high conductivity but great insulation properties in order to be as thin as possible, among other design features.

This type of design features not only makes more difficult for the designers to come with an optimal layout that preserves the electrical characteristics, but also significantly increases costs which is even more critical in this particular case since the GaN power transistors used are already a very expensive solution. On top of that there are the size constraints meaning that the thermal management have to be made keeping a small form factor.

Both the GS61008P (input module) and the GS66508P (output module, refer to Section 4.3.1) are bottom cooled versions of the E-HEMTs (enhanced mode high electron mobility transistors) provided by GaN Systems and are very low profile packages occupying a small footprint on the board although its power processing capabilities. On the modules, all the components are surface mounted on the top layer of the PCB leaving the bottom layer free to accommodate the heat spreader. Therefore, the method used to

cool the power devices is thermal vias. In the application note GN005 [70] an extensive description and thermal tests describe the optimal via patterns and quantity to dissipate heat and in the design these recommendations are followed the best way possible.

However, although the *HiGaN* microinverter being highly optimized both electrically and thermally, there are still concerns with the thermal management. Thermal measurements indicated that the input module (DC-DC converter) presents the highest temperatures on the board, with the junction temperature (T_j) reaching 85°C for an output power of 70% of the nominal power which is a quite high temperature considering that the maximum operating T_j is 150°C. Therefore, the cooling of the transistors could be improved in order to have a more reliable system for all its output power range and to not degrade the device's lifetime. Another point is that the R_{DSon} increases significantly with temperature as can be seen in Figure 53 on the curves extracted from the GS61008P datasheet. Since the devices are switched at high frequency, this reduces the system efficiency substantially.

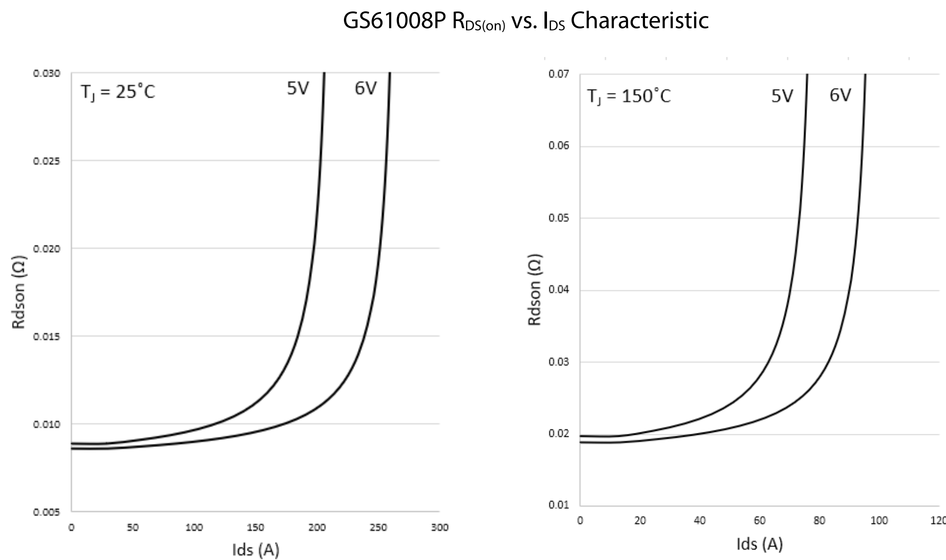


Figure 53 – GS61008P R_{DSon} versus drain-to-source current for different junction temperatures [11].

As discussed in Section 2.5.5 the ECT can improve the thermal management of the PCBs, mainly in the case of power converters as inverters and DC-DC converters, where there is high power processed by semiconductors. Under the optic of size reduction, it is interesting to achieve a better thermal management in order to reduce the size and consequently the weight of heat sinks and heat spreaders, which in aforementioned power converters are a great part of the weight and size occupied by the PCBs when the devices are installed. Besides, with more effective heat conduction from the components to the heat sink it is possible to increase component proximity because the heat produced by the power processing components doesn't affect the surrounding components as much.

Using the placed components ECT the transistor package would be placed in an inner layer of the PCB and therefore surrounded by the cavity filling material, prepreg, dielectric and copper. Hence the heat dissipation problem gets down to how well heat can be transfer from the device to and through these materials, to finally a heat sink/spreader or directly to the environment.

There are already dedicated process aiming better heat dissipation for embedded power electronics, for example the P2P packaging technology, described in Section 2.4.7, that uses thick copper layers to act as heat spreaders inside the board, but there are a range of core PCB materials with enhanced thermal properties that also could be investigated and maybe be a more cost-effective solution since the process of embedding standard packages can be done with different materials.

Regarding the exposed, it is interesting to evaluate how the ECT could improve the thermal management of the power sub-modules by embedding the GaN transistors used. As mentioned, these packages are very low profile and very thin, being ideal to embed since the depth of the cavities can be smaller consequently allowing to keep the PCB thickness small. Furthermore, up until now, this study focused on the embedding of passive components and how this could be used to reduce the size of the *HiGaN* motherboard, not directly involving the power components of the inverter. Therefore is worth to investigate the capabilities offered by the ECT in this regard to have a better understanding of its application in power electronics. This chapter is devoted to present the results of thermal simulation using finite element analysis and CFD (Computed Fluid Dynamics) of different layer stack configurations for embedded GaN transistors.

5.1 Thermal simulation methodology

The first step to conduct any thermal simulation is to create a model of the system in the desired coordinate system or environment. In this case the model must be simulated in a 3-dimensional environment because the temperatures of the bodies in different locations are ought to be known and the heat flow in all axis have to be evaluated.

Ideally a thermal-electrical simulation would be performed using a complete model of a PCB containing the transistor to be evaluated, for example the output power-submodule. However, this would require to know the power losses in each component of the board to account for joule heating effect and the whole model would be very complex. Furthermore, since in this simulation the point of interest is to evaluate how well the heat produced by one single embedded transistor is dissipated by the PCB material, there is no need to simulate a complete model because, despite the complexity, there would be other factors influencing in the heat dissipation.

Considering the exposed, a simplified model was designed. The model is based on the simulation presented in [70] and consists of a 30 x 30 mm PCB with one single GS66508P

transistor. Initially a standard (without embedding the transistor) configuration is used to provide a comparison base. For this initial simulation the parameters such as number of layers, layer thickness, PCB thickness, area of copper planes and number of thermal vias are the same as in [70]. All model parameters for the initial simulation are shown in Table 10.

A boundary condition of constant temperature is applied to the external face of the bottom layer setting it to 25°C. This would emulate the lower face of heat sink directly in contact with the bottom copper plane. This boundary condition is an approximation needed in order for the solution to converge, and could be faced as an ideal heat sink capable of maintaining the temperature constant.

The model is simulated with the bottom layer facing up (regarding the direction of gravity being the negative Z axis). This way is possible to mimic the conditions of how the power submodules are mounted.

The CFD software used to perform the thermal simulations is FloTherm 12.1. This software provides tools to directly import the PCB data from the EDA software (Altium Designer), however it doesn't discretely generates the copper areas of the board. Instead it evaluates the copper data and creates what is called by the software as *patches*, which is, in simplified terms, areas in the model with modified material properties based on the estimation of amount of copper in this particular area.

The more patches are created, the more accurately the representation is, however still an estimation, thus generating a model more suited for a system level simulation than a package level simulation which is the case. Besides, the amount of bodies created in the model is higher, hence the simulation is more complex and requires more time and computational power. Therefore, instead of importing the data directly from Altium, the model was designed in FloTherm using the primitive geometric entities.

The model designed is seen in Figure 54. The transistor model is simplified and consists in the package, the die and the copper pads. The dimensions of the package are provided in the datasheet and the material used is the "Typical Plastic Package" provided in the material library of FloTherm. The copper pads dimensions are also provided in the datasheet. The dimensions of the die are provided in [70] except for the thickness which was provided by GaN Systems after requesting the information. The die is defined as the power source in the simulation.

To further simplify the model, the vias were designed with a square shape and the dimensions were modified from the values in [70] to approximate the surface area of a round via. The properties of the materials used in the model are listed in Table 11.

In order to evaluate the embedded transistor thermal behaviour and compare with the standard configuration, several different cases were simulated modifying the parameters of the model seen in Figure 54. Each case or *run* is presented in Table 12. To reduce the number of factors that influence on the final results, the number of vias, die power

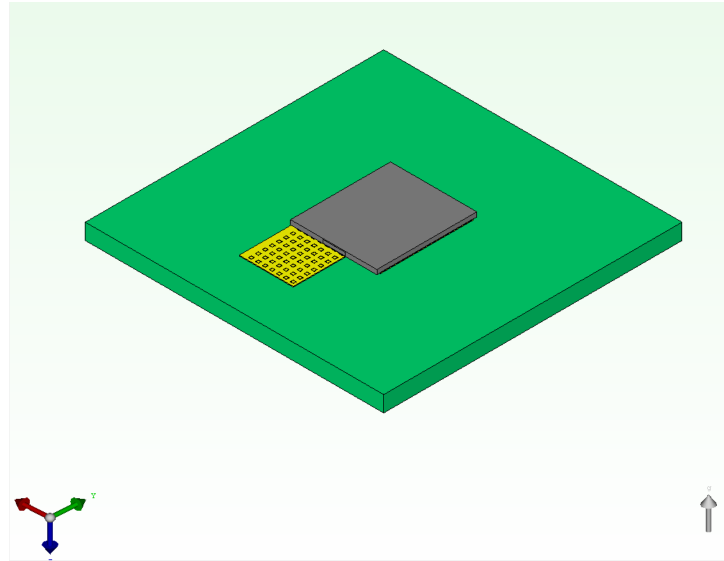


Figure 54 – Isometric view of the model in opposite direction to gravity.

Parameter	**Value**
System (world) dimensions (mm)	35 x 35 x 30
PCB dimensions (mm)	30 x 30 x 1.6
Layers	4
Layer thickness (μm)	70 (evenly spaced)
Copper planes area	70 mm^2
Number of vias	123
Die power	10 W
Ambient conditions	25°C, 1 Pa
Ambient boundaries	Open
Number of grid cells	409812
Grid aspect ratio	218.6

Table 10 – Model parameters for initial calculation.

Material	**Thermal conductivity (k) (W/mK)**	**Density (kg/m^3)**	**Specific heat (J/kgK)**
FR4	0.3	1200	880
Copper	385	8930	385
Plastic Package	5	2000	395

Table 11 – Material properties.

and copper area in each layer were not changed. In the output power submodule, filled and capped vias are used, therefore for each case listed a simulation with regular plated through hole (PTH) vias and filled and capped (FC) vias was performed.

The layer stack configurations used in each run are depicted in Figure 55 and serves as illustration purposes only, not representing the model used on FloTherm nor the actual dimensions applied. To better understand the layer stacks used in the simulation refer to Section 3.2.3.

For run 2 the embedded layer stack is not practically feasible because there is not

Run	Configuration	PCB Thickness (mm)	# Layers	Layer Thickness (μm)	Observation
0	Standard	1.6	4	70	Control simulation with 0 W die power
1	Standard	1.6	4	70	Standard stack with evenly spaced layers
2	Embedded	1.6	4	70	Evenly spaced layers (not feasible by most manufacturers)
3	Embedded	1.6	4	70	Changed distance between layers to simulate a common dielectric thickness for embedded components stack
4	Embedded	2.73	4	105; 35; 35; 105	Same layer stack as used in the *HiGaN* v3.0.4
5	Embedded	2.73	4	105	Same layer stack as in Run #4 but with same layer thickness to all layers
6	Embedded	2.73	6	105; 70	Same layer stack as in Figure 50 with 70 μm copper planes

Table 12 – Parameters of each simulation run.

enough clearance between the component body and the layer above (as explained in Section 3.3) due to the fact that the layers are evenly spaced, hence this run is just for comparison purposes.

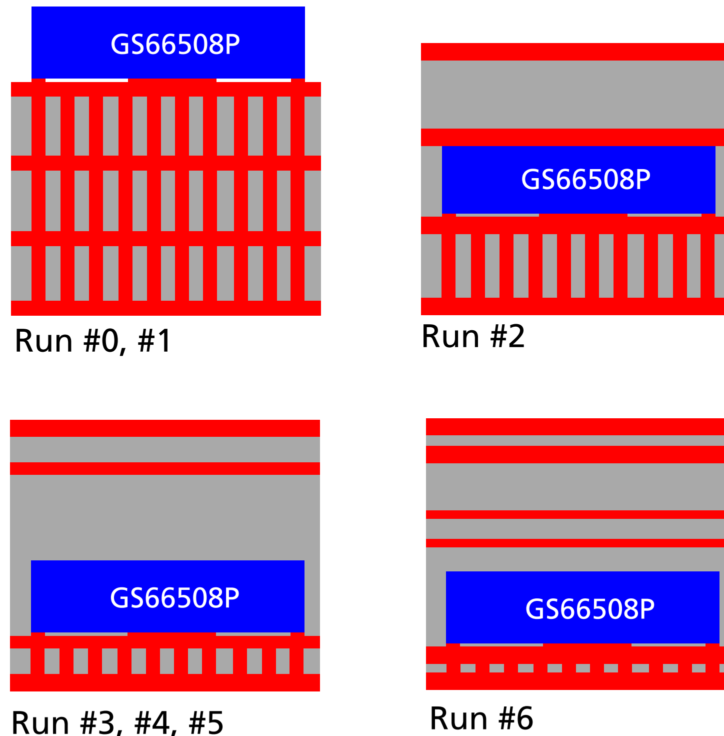


Figure 55 – Layer stack configurations used for each run of the simulation.

Only one monitor point was added to the simulation and is located directly on the center of the lower face of the die, and is named *Die Temperature*. This would translate as close as the junction temperature can be measured in practical experiment. The highest temperature in the cross section exactly in the middle of the board is tracked automatically by FloTherm. To conduct the simulations the default FloTherm solver

settings for a steady state solution were used.

5.1.1 Thermal simulation results

Table 13 presents the two temperatures tracked during each run for the two types of vias modeled and Figure 56 shows a plot of the temperatures for each run. Since run 0 was only performed to serve as control and provide initial data for a future transient analysis, the values were not plotted in Figure 56.

From Table 13 is possible to see a considerable difference between the standard configuration (run 1) and the embedded stacks. In fact, the average temperature difference for the die was 15.5 °C for the configurations with PTH vias and 7 °C for filled and capped vias. Another notable point is that the temperature difference between the maximum temperature detected and the die temperature is lower for the embedded configurations indicating a better heat distribution.

Run	**Via Type**	**Die Temperature (°C)**	**Max. Temperature (°C)**
0	PTH	24.9	25
1	PTH	54.2	58.1
1	FC	38.1	40.6
2	PTH	31.2	39.9
2	FC	27.6	32.3
3	PTH	34.4	36.4
3	FC	29.4	30.9
4	PTH	40.9	43.2
4	FC	32.1	33.7
5	PTH	37.7	40.1
5	FC	30.1	32.5
6	PTH	34	36.5
6	FC	29.1	31

Table 13 – Results for each run.

Is possible to see that run 2 presents the lowest die temperature for both PTH and filled and capped vias, but not the lowest maximum temperature. This indicates and makes possible to assume that besides not being feasible, layer stacks with incorrect dielectric thickness also brings worse heat distribution. Another conclusion from the data is that, as expected, the copper thickness of the layer where the transistor is attached is one of the most important aspects to achieve lower temperatures as is possible to see from the difference between run 4 and 5.

It is important to understand how the heat is distributed through the board and for that a surface temperature plot is suited. The point of interest is the cross section of the

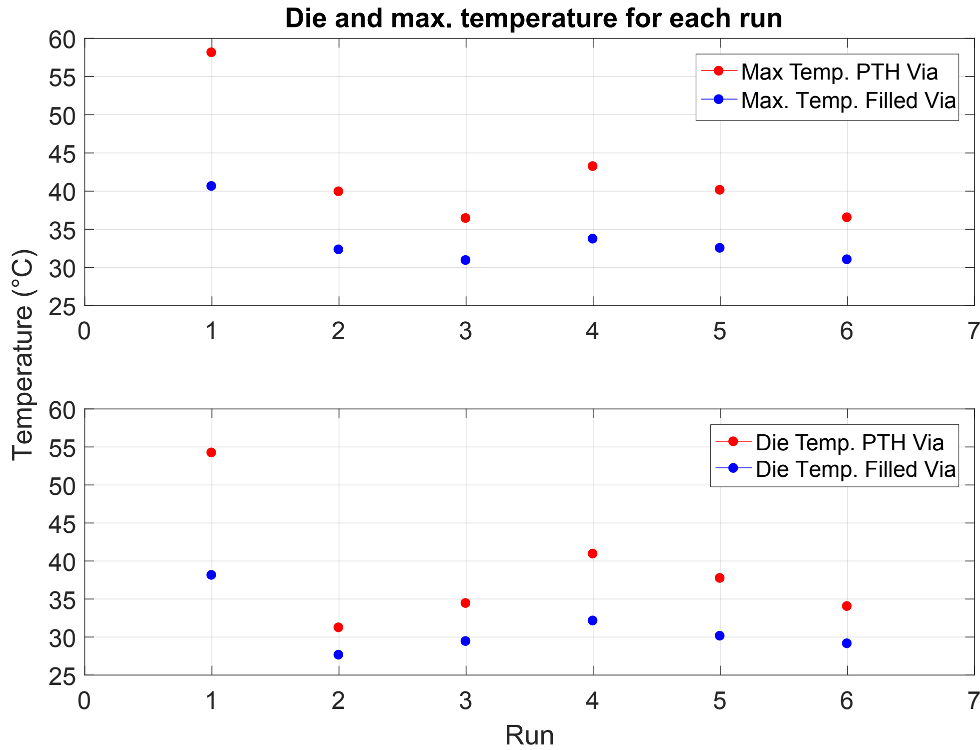


Figure 56 – Thermal simulation results plot.

board as is possible to detect the highest temperatures and verify if the stacks simulated provide a good way of dissipating the heat produced by the transistor. To generate the surface plots, since the actual power submodule is realized using filled and capped vias, only these results are evaluated.

In Figure 57 through Figure 59 the surface temperature plot for run 1, 4 and 6, respectively is shown. Run 4 and 6 are compared to the standard configuration (run 1) because they represent the two most probable layer stacks that would be used in case if new power sub modules were fabricated. Additionally, the stack applied in run 4 is identical to the layer stack of the *HiGaN* version 3.0.4 (see Section 4.3), providing a way to test a theoretical case where the transistors are embedded in a board with other embedded components and therefore higher dielectric thickness. Besides these two layer stacks are known to be feasible by the manufacturers contacted.

From the surface temperature plots is possible to see that when copper planes are added to the stack (run 6) the heat distribution is much more even, as it would be expected. This reduces the temperature of the hot spot and depending on the materials and parameters used (overall dimensions and number of layers) could even eliminate the hot spots completely as is also shown by Hofmann in a demonstration of the AML technology [33].

It is also possible to understand why the location where the monitor point was positioned wasn't the point of maximum temperature. For all cases the heat is concentrated in the region closer to the die but where there is no direct contact with the thermal vias.

Since inside the board almost all the heat transfer occurs by conduction, the points with good contact with the copper parts will naturally be able to transfer the stored heat more efficiently since the laminate thermal conductivity is very low, therefore, as the bottom surface of the die is in direct contact with the thermal pad, the temperatures are lower.

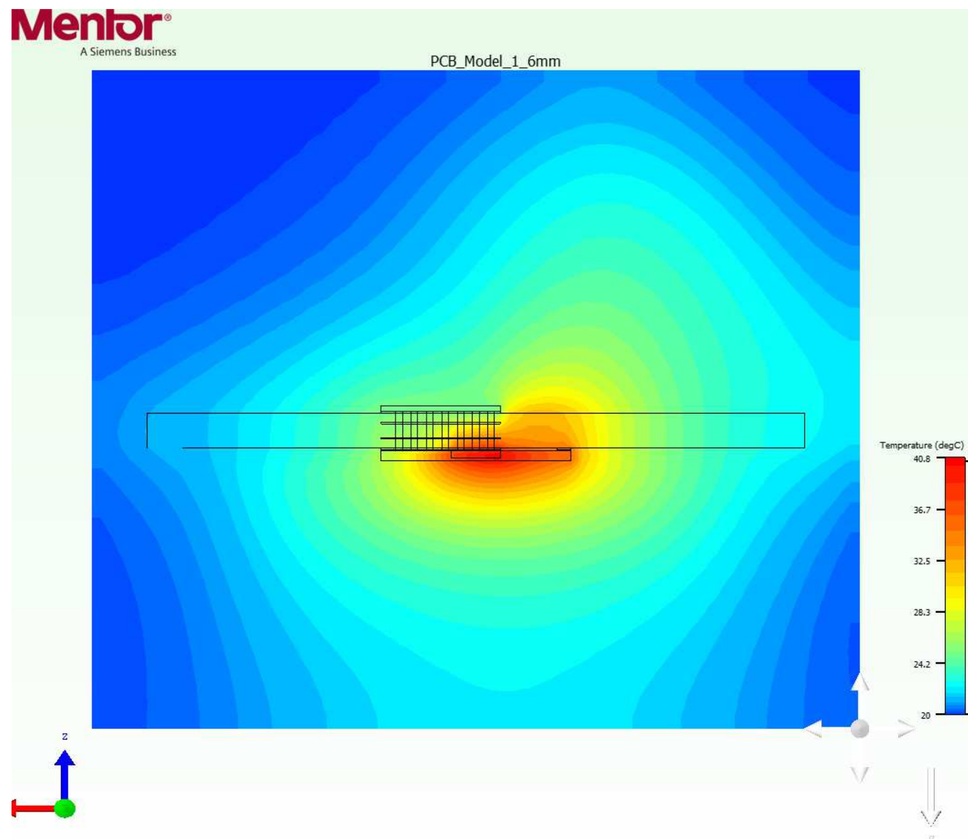


Figure 57 – Surface temperature plot in cross section for run 1.

One interesting point to be noted is that even with higher PCB thickness, run 4 and 6 still outperform the standard configuration. Another point is that normally there are vias connecting the two upper signal layers as shown in Figure 29 and Figure 50, thus there is possibility for an even better thermal performance since the heat transfer would be more effective.

Although there are multiple configurations for a possible layer stack, using different materials and construction parameters, and further aspects to be analyzed, these initial results confirm the exposed in Section 2.5.5 and show that is possible to achieve a better thermal management for a device like the GS66508P. The results presented in this section make part of a broader investigation that is currently ongoing. Nevertheless is safe to conclude that the ECT can be a suitable alternative to improve the thermal management of power converters using WBG devices and this opens other possibilities to the use of this technology.

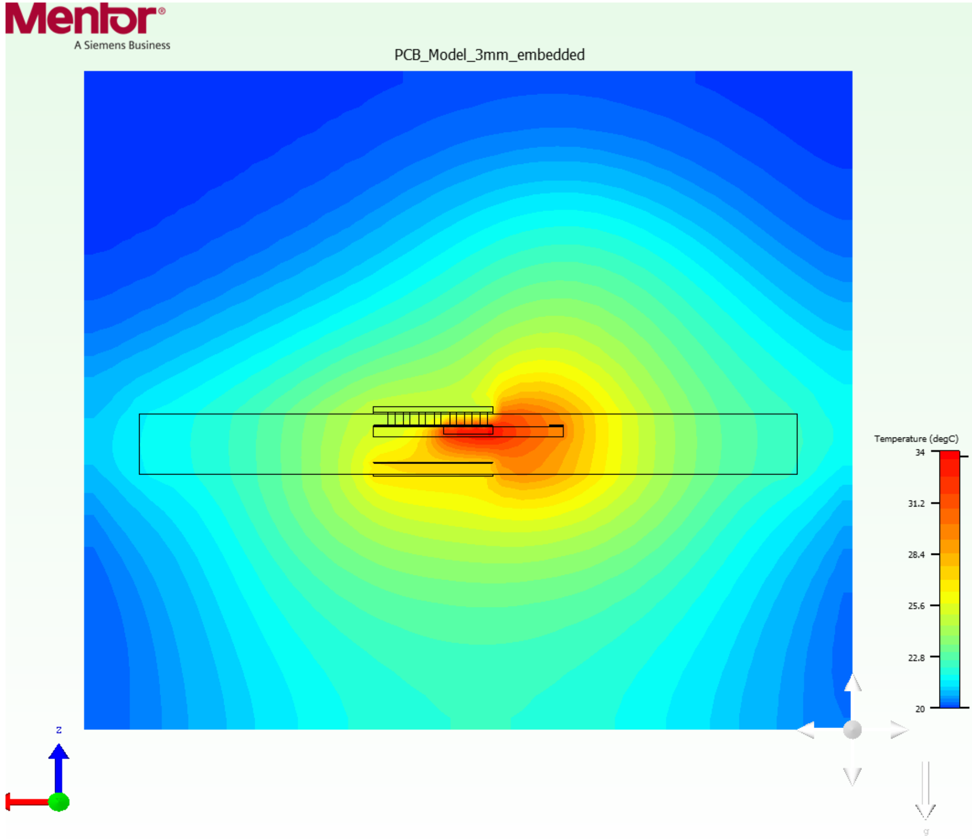


Figure 58 – Surface temperature plot in cross section for run 4.

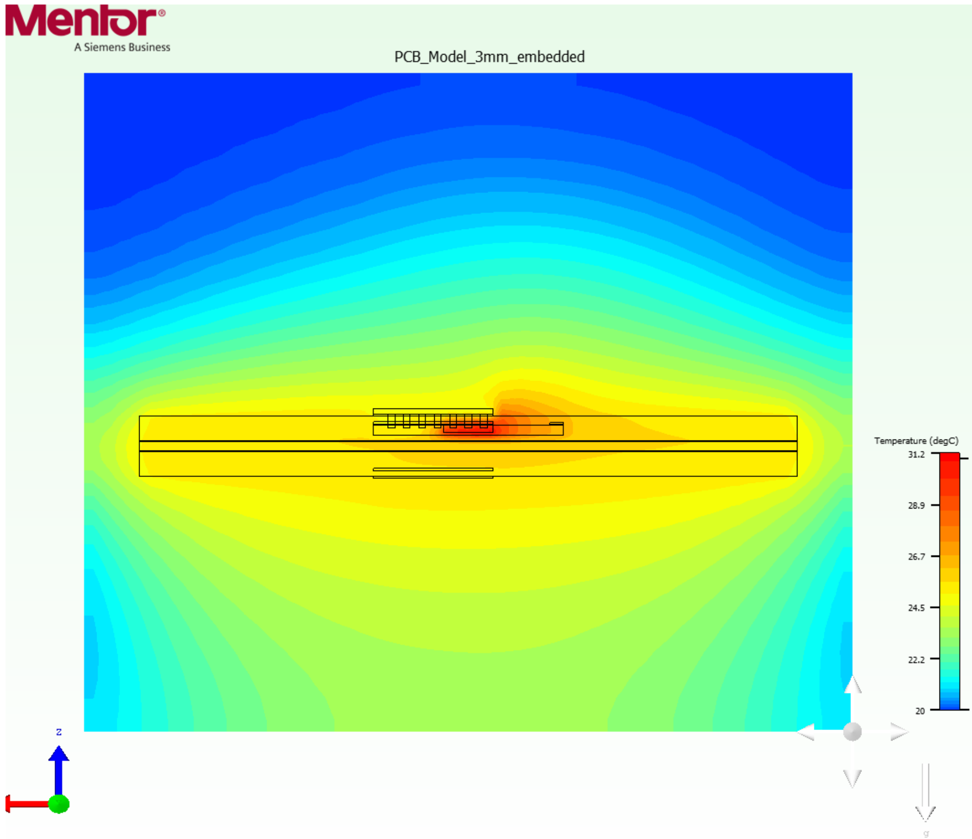


Figure 59 – Surface temperature plot in cross section for run 6.

6 Conclusions

This thesis presented a theoretical work for the application of the embedded component technology to a highly compact inverter, the *HiGaN* microinverter. First, the panorama of the application of such devices was presented giving the context of how the microinverters are in the market today and also what can be improved in order to make this branch of the solar energy market even more attractive. Additionally, the ECT was presented as a possible solution to reduce the size of the *HiGaN* microinverter and a deep analysis and review of this technology were presented.

With all the aspects regarding the ECT exposed, the development of a design methodology to use the ECT in order to reduce the size of the *HiGaN* motherboard was presented. The approaches and requirements of the design were exposed as well as an analysis of manufacturers capabilities and requirements to eventually manufacture a prototype of the new design developed. A review of the steps necessary to design a PCB using ECT in the Altium Designer software was also presented and serves as documentation to future use of this work not only as database but also possible guidelines.

With all the requirements and methodology established, five new versions of the *HiGaN* motherboard were designed. The results were shown in detail and data related to area reduction and component density was presented. A comparison between the versions designed was presented and the important points discussed to confront the bibliographic data with the application on this particular case. Although a prototype wasn't fabricated, an economical analysis was also conducted to better comprehend the state of the technology.

Throughout the thesis, although the ECT was applied to the components of a power converter, only low power components were considered in the different motherboard designs. Therefore, to understand the use of the ECT directly applied to power devices and to evaluate the thermal management improvement capabilities of the technology, thermal simulations of an embedded power transistor were conducted. The methodology and results were presented and gave a wider view of the spectrum of application of the ECT.

6.1 Final considerations

Regarding the objectives exposed in Section 1.2, all objectives were reached. The core purpose of this thesis was to construct an updated and resumed database of the ECT. This was achieved reviewing the principles of the technology and also investigating some of the industrial methods provided by several manufacturers. From this analysis it is possible to see that the ECT presents itself as a much mature technology compared to ten years

back although still being considered as a leading edge technology. The most concerning issue is the lack of a unique and definitive norm and the standardization of industrial methods, not only in procedures and final specifications, but also in methodology. This is somewhat still a good aspect because it pushes innovation forward but in most cases, hampers the process to choose the ECT as the manufacturing method.

Another concerning point during the development of the new versions of the motherboard was the lack of proper documentation on how to use the ECT with most of the new EDA software. In most cases the documentation is either completely missing or incomplete, not providing all necessary instructions. This ends up being another reason why the technology is still not quite as popular as it could be regarding the benefits that it brings. Nevertheless, after the modifications on the software and component libraries, the design process using the ECT showed to be simple and in some cases even simpler than designing with the standard technology and allow to attend PCB design rules more easily in most of the cases studied.

The main objective of using the ECT was to achieve size reduction on the *HiGaN* microinverter motherboard. The results of the final versions designed shows that this objective was achieved. It is imperative, however, to understand the particularities of the designs and how the ECT actually contributed to size reduction. In versions 3.0.2 through 3.0.5 there is the use of extra modules that take components out of the motherboard and, by being mounted in different configurations, allow for size reduction. This showed that a modular design can be a good approach for MLPEs such as the *HiGaN* but most importantly, showed the real potential for embedded passive components to achieve size reduction is indeed in low power and logic systems.

This is confirmed when comparing the size reduction achieved in the microcontroller module and the DC-DC breakout module. This was expected and confirms what was researched in the bibliography. It must be noted that this doesn't exclude the use of ECT from power electronics application, it only means that the ECT must be faced as an auxiliary tool to achieve size reduction in the case of power electronics.

In this project only standard substrate materials were studied as well as only standard layer stack configurations, meaning that, the attempt was to use the ECT as is provided by the manufacturers in the market. This can lead to conclude that there is a considerable amount of development to be made in this area, but most importantly, the development achieved in the academia must be used and incorporated by the industry in a more quick and efficient way.

Regarding the manufacturing level, the issue with standardization is more notable. Different requirements and different methodologies leads to considerable differences in prices and design rules and guidelines. It is possible to realize that the PCB manufacturing companies that offer the technology are still taking advantage of this being a "new" technology. This makes the prices of the technology very high for the final consumer,

especially in the case of small to prototype level manufacturing. This was one of the reasons the prototype designed wasn't manufactured.

Although an expensive alternative, the other advantages of the ECT must be taken into account when considering to use the technology. The thermal simulations presented are one example of what the ECT can bring besides size reduction, and in order to have a cost effective product the design must be done intelligently to unite the strong aspects of the ECT.

The use of the ECT in power electronics application must be pushed forward to achieve better systems and have more options of manufacturing techniques, therefore this project is a step in the right direction for the development of this field.

6.2 Main contributions

The main contribution of this project was to give more details and build a database, based on a real case, of the aspects of the ECT. This project shows comprehensively several of the multiple ways to achieve size reduction using the ECT but also brings alternatives to use the technology in different ways. This enables for future development of the *HiGaN* project and other MLPEs with a wider range of possibilities. Regarding the field of application of the *HiGaN* project, solar energy, this work is another step towards the expansion of solar energy systems because it attempts to make one of the core devices in such systems more reliable, efficient and cost effective.

Besides, this work introduces another point view of the application of the ECT in power electronics and helps to push not only the technology itself to be more popular among developers but also the whole field of power electronics.

6.3 Future works

One further design improvement would be integrate the microcontroller module directly to the motherboard, since in version 3.0.3, for example, the component density is very low and there is suitable space to further integration or even increasing functionalities. The next step would be the selection of one of the designs to be fabricated. This would enable to perform experiments and evaluate other aspects of the ECT.

This project will be continued focusing in the thermal management aspect, as discussed in Chapter 5. The development will specifically aim better thermal management on boards using GaN devices, since this is one of the major difficulties in order to achieve higher efficiencies with such devices. Different configurations will be studied as well as different materials and new cooling concepts applied on embedded stacks

In parallel, the shielding effect of the ECT will could also be studied in more detail, mainly the shielding against heavy ion radiation applied for the aerospace industry.

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