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Rafael Luciano Radin

A SELF-STARTUP ULTRA-LOW-VOLTAGE BOOST CONVERTER FOR THERMAL ENERGY HARVESTING

Florianópolis
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Rafael Luciano Radin

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O presente trabalho em nível de doutorado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Prof. Tales Cleber Pimenta, Ph.D.
Universidade Federal de Itajubá (UNIFEI)

Prof. Oscar da Costa Gouveia Filho, Dr.
Universidade Federal do Paraná (UFPR)

Prof. Cesar Ramos Rodrigues, Dr.
Universidade Federal de Santa Catarina (UFSC)

Eng. Paulo Augusto Dal Fabbro, Dr.
Chipus Microelectronics

Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de doutor em Engenharia Elétrica.

Bartolomeu Ferreira Uchoa Filho:47636211491

Assinado de forma digital por Bartolomeu Ferreira Uchoa Filho:47636211491
Dados: 2020.05.15 18:05:15 -03'00'

Prof. PhD Bartolomeu Uchôa-Filho
Coordenador do Programa

Marcio Cherem Schneider:08255679987

Assinado de forma digital por Marcio Cherem Schneider:08255679987
Dados: 2020.05.01 09:17:57 -03'00'

Prof. Dr. Márcio Cherem Schneider
Orientador

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RESUMO

Esta tese apresenta a análise e implementação de um conversor DC-DC operando em ultra baixa tensão para aplicações em colheita de energia térmica. O projeto foca na redução da mínima tensão de entrada para autoinicialização e operação do conversor elevador de tensão indutivo, bem como na melhoria da eficiência em toda faixa de tensão de entrada. O conversor elevador de tensão indutivo é analisado e equações de projeto são fornecidas considerando a operação em ultra-baixa tensão de entrada, onde as não-idealidades características de operação com disponibilidade de potência restrita são contabilizadas. A inicialização do conversor é realizada por um mecanismo composto de um oscilador em anel com excursão ampliada e um retificador. Com o intuito de minimizar a tensão de inicialização do sistema, uma metodologia de co-projeto para o oscilador e o retificador é proposta, bem como a implementação de um conversor elevador de tensão que utiliza a chave do ramo inferior com largura variável. O sistema de chaveamento em corrente zero proposto introduz escalamento não linear para modulação do pulso que controla o tempo de descarga do indutor do conversor elevador de tensão, incrementando a eficiência para baixas tensões de entrada. As expressões derivadas para a definição do atraso de medição do esquema de chaveamento em corrente zero aumentam a acurácia da detecção do cruzamento da corrente por zero, maximizando a eficiência de conversão. Resultados experimentais mostram avanços na mínima tensão requerida para inicialização do conversor elevador de tensão quando comparado ao atual estado da arte. O conversor inicializa para uma tensão de apenas 11 mV, proporcionado operação em regime permanente para tensões de entrada de até 7,3 mV. A eficiência é superior a 50% para tensões de entrada superiores a 10,5 mV. Os resultados obtidos possibilitam o uso do conversor para operação independente e contínua a partir de gradientes de temperatura da ordem de 1^{o}C.

Palavras-chave: Colheita de energia térmica. Ultra-baixa tensão, Gerador termelétrico. Conversor elevador de tensão. Autoinicialização. Chaveamento em corrente zero.

RESUMO EXPANDIDO

Introdução

Com a crescente miniaturização e aumento da capacidade computacional dos dispositivos eletrônicos, tornaram-se possíveis diversas aplicações no cenário da Internet das Coisas, onde dispositivos conectados realizam a aquisição de grandes quantidades de dados, que podem ser processados usando técnicas de aprendizado de máquina, permitindo a execução de tarefas cada vez mais complexas. Diversas são as aplicações no contexto de cidades inteligentes, como a implantação de uma rede elétrica inteligente, monitoramento de ruído e poluição, gerenciamento de tráfego e de resíduos, estacionamento e iluminação inteligentes, etc. Dispositivos inteligentes possuem diversas aplicações também em edificações, relacionadas a entretenimento, qualidade de vida, automação inteligente, etc. O corpo humano também tem um forte potencial para várias aplicações, como sensores para treinamento esportivo, dispositivos de monitoramento de saúde acoplados ao corpo humano, etc. Dada a vasta aplicação de dispositivos inteligentes na vida cotidiana, o número de dispositivos conectados tem aumentado constantemente. Este elevado número requer uma interação transparente e descomplicada com o usuário, sendo impraticável gerenciar, recarregar ou substituir baterias para cada aplicação. Neste sentido, um requisito importante para os dispositivos conectados é o suprimento de energia autônomo, que permite que o dispositivo seja independente de fiação ou baterias, diminuindo a frequência de manutenção e permitindo maior portabilidade para o dispositivo. Nesse contexto, a colheita de energia tornou-se uma solução importante, permitindo que esses dispositivos atendam aos requisitos de operação autônoma e ininterrupta. A colheita de energia térmica é de particular interesse para várias aplicações relacionadas ao corpo humano, pois pode fornecer energia ininterruptamente a partir do calor dissipado, em níveis de grandeza superiores a outras formas de colheita de energia. Em uma aplicação típica de colheita de energia, conversores de tensão são empregados para aumentar o nível de tensão gerado pelos geradores termoelétricos, que geralmente é da ordem de algumas dezenas de mV. As figuras de mérito mais relevantes para esses conversores são a faixa de tensão de entrada, eficiência, tensão mínima de entrada, tensão de inicialização e o tamanho do dispositivo.

Objetivos

Nesta tese foi desenvolvido um conversor de tensão para colheita de energia térmica, onde os seguintes tópicos foram propostos e pesquisados: análise do conversor elevador de tensão indutivo operando em ultrabaixa tensão e alimentado por uma fonte de alimentação limitada; desenvolvimento de uma topologia de conversor eficiente utilizando um esquema de crescimento da tensão de saída passo a passo; desenvolvimento de um procedimento de projeto para o bloco de inicialização do conversor com a premissa de minimizar a tensão mínima para inicialização; um esquema de comutação em corrente zero modificado que aumenta significativamente a precisão de detecção de corrente zero e eficiência de conversão.
O conversor de tensão para aplicações em colheita de energia térmica foi projetado objetivando-se as seguintes contribuições para o estado da arte: a redução da mínima tensão de entrada do conversor para operação em regime permanente; a redução da tensão de inicialização do conversor; a maximização da eficiência em toda a faixa de tensão de entrada. Estas características permitem o conversor inicializar e operar eficientemente em baixos gradientes de temperatura, permitindo que a colheita de energia térmica possa ser realizada de forma eficiente a partir do corpo humano, mesmo em condições adversas de temperatura.

Metodologia

Um modelo matemático para o conversor elevador de tensão indutivo foi desenvolvido, utilizando modificações necessárias às equações do conversor que refletem as condições de baixa tensão de entrada e a restrição da capacidade de corrente do gerador termoelétrico. As expressões derivadas permitem definir o tamanho ótimo para as chaves do conversor elevador de tensão indutivo, bem como definir a frequência de chaveamento para maximizar a extração da potencia provida pelo gerador termoelétrico. A arquitetura desenvolvida utiliza o conversor elevador de tensão indutivo para operação em regime permanente e um circuito auxiliar para realizar a inicialização do conversor, cuja metodológica de otimização foi empregada no intuito de minimizar a tensão de entrada para inicialização do conversor. Como o conversor elevador de tensão indutivo opera no modo de condução descontínuo, foi desenvolvido um circuito de chaveamento em corrente zero com escalamento não linear do pulso relacionado ao tempo de descarga do indutor, provendo aumento da eficiência de conversão para níveis mais baixos de tensão de entrada. Também foram definidos parâmetros temporais importantes para o circuito de chaveamento em corrente zero, minimizando o erro de detecção do cruzamento da corrente por zero, o que contribui positivamente para o aumento da eficiência de conversão. A fase de projeto do conversor foi realizada através de ferramenta de automação de design eletrônico Cadence, disponibilizada na École Polytechnique de Montréal, sendo possível a simulação de esquemático, realização de layout do circuito integrado e simulações pós-layout, de modo a garantir a convergência dos resultados após a integração.

Resultados e Discussão

O conversor DC-DC proposto foi integrado na tecnologia CMOS de 130 nm através da facilidade de integração disponibilizada pela CMC Microsystems. O chip fabricado possui uma área total de 1,5x1,5 mm^2. Alem do circuito integrado, o conversor elevador de tensão indutivo utiliza um indutor e dois capacitores externos. A inicialização do conversor foi realizada através do circuito auxiliar também integrado no mesmo chip, podendo ser implementado de maneira totalmente integrada ou utilizando quatro indutores externos além do circuito integrado no chip. Nos resultados experimentais obtidos, a tensão mínima de inicialização foi de 90 mV utilizando-se indutores integrados. Utilizando-se indutores discretos, o conversor inicializa para níveis de tensão de entrada da ordem de 11 mV. A tensão de entrada mínima capaz de sustentar a operação em regime permanente foi de 7,3 mV. A tensão mínima de entrada necessária para atingir eficiência de 50% é de aproximadamente 10,5 mV. Para tensões de entrada superiores a 40 mV, o conversor mantém eficiência sempre superior a 83%, já á máxima eficiência medida é de 85%. A eficiência de extração é superior a 95% para toda a faixa de tensão de entrada.

Considerações finais

A tensão de inicialização medida para o conversor é a mais baixa reportada até o momento, com avanço importante em relação ao estado da arte para esta figura de mérito. Os valores medidos para a eficiência em ultrabaixa tensão e mínima tensão de operação do conversor também foram compatíveis com o atual estado da arte. A combinação de alta eficiência para baixas tensões de entrada e inicialização em ultrabaixa tensão obtida neste trabalho permite a realização de colheita de energia térmica eficiente e autônoma mesmo quando o gradiente de temperatura é da ordem de 1 ^oC, possibilitando a operação autônoma e ininterrupta de dispositivos conectados alimentados pela energia térmica provida pelo corpo humano.

Palavras-chave: Colheita de energia térmica. Ultra-baixa tensão, Gerador termelétrico. Conversor elevador de tensão. Autoinicialização. Chaveamento em corrente zero.

ABSTRACT

This thesis describes the analysis and implementation of a DC-DC converter for ultra-low-voltage thermal energy harvesting applications. The design focuses on the reduction of the minimum input voltage to achieve self-startup and operation of the inductive boost converter, as well as on the improvement of the end-to-end efficiency throughout the input voltage range. The inductive boost converter is analyzed and design equations are provided considering the operation under ultra-low input voltages, where the non-idealities which arise under restricted power availability are taken into account. The startup of the converter is achieved by an auxiliary cold starter comprised of an enhanced-swing ring oscillator and a rectifier. In order to minimize the system startup voltage, a co-design methodology for the oscillator and the rectifier is proposed as well as the implementation of a boost converter using a low-side switch with variable width. The proposed zero-current switching scheme introduces non-linear time scaling for the modulation of the pulse that controls the boost inductor discharging time, which results in higher efficiency at low input voltages. The expression derived for setting the measurement delay of the zero-current-switching scheme increases the accuracy of the zero-current-crossing detection, improving the conversion efficiency. Experimental results show an improvement in the minimum startup voltage of the boost converter when compared to the current state-of-the-art devices. The converter starts up from an input voltage of only 11 mV and provides steady-state operation for input voltages as low as 7.3 mV. The end-to-end efficiency is higher than 50% for voltages above 10.5 mV. The results achieved enable the use of the converter for autonomous and uninterrupted operation from temperature gradients of the order of 1 ^{o}C.

Keywords: Thermal energy harvesting. Ultra low voltage. Thermoelectric generator. Boost converter. Self startup. Zero-current switching.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC – Alternating current

CCM – Continuous conduction mode

CSRO – Current-starved ring oscillator

DC – Direct current

DCM – Discontinuous conduction mode

DCP – Dickson charge pump

EDA – Electronic design automation

ESRO – Enhanced-swing ring oscillator

HSS – High-side switch

ILRO – Inductive-load ring oscillator

IoT – Internet of things

LSS – Low-side switch

MOS – Metal oxide semiconductor

MOSFET – Metal oxide semiconductor field-effect transistor

MPPT – Maximum power point tracking

NMOS – n-type metal oxide semiconductor

PMOS – p-type metal oxide semiconductor

TEG – Thermoelectric generator

ULV – Ultra-low-voltage

ZCS – Zero-current switching

ZVT – Zero-VT

LIST OF SYMBOLS

C_{OX} – Oxide capacitance per unit of area

C_{LHSS} – High-side-switch linear capacitance per unit of width

C_{LLSS} – Low-side-switch linear capacitance per unit of width

C_{MPAR} – Parasitic capacitance at node M

C_{OUT} – Output capacitance

C_{PAR} – Parasitic capacitance

D – Duty cycle (normalized inductor charging time)

D' – Normalized inductor discharging time

D'' – Normalized inductor idle time

E_L – Inductor energy

E_S – Power supply energy

E_{TPULSE} – Output energy for a given pulse width

E_{ZCS} – Output energy for ideal zero-current switching

f_{SW} – Frequency of switching

i_{CIN} – Input-capacitor current

i_{COUT} – Output capacitor current

I_D – MOSFET drain current

$\overline{i_L}$ – Average inductor current

i_L – Inductor current

I_L – Load current

I_{LP} – Inductor peak current

I_{OUT} – Output current

I_{PER} – Peripheral circuits current

i_r – Reverse inversion level

I_S – Reverse bias saturation current (from Shockley equation)

i_{TEG} – Thermoelectric generator current (without input capacitor)

I_{TEG} – Thermoelectric generator current

I_0 – Modified Bessel function of the first kind of order zero

I_1 – Modified Bessel function of the first kind of order one

L – Boost inductance

L – MOSFET channel length

L_{DIFF} – Length of drain/source diffusions

L_{HSS} – High-side-switch channel length

L_{LSS} – Low-side-switch channel length

M – Boost converter voltage gain (gain factor)

n – Slope factor

N – Number of stages of the rectifier

n_{st} – Number of CSRO stages

P_{AV} – Available power

P_{COND} – Conduction losses

P_{DHSS} – High-side-switch dynamic losses

P_{DLSS} – Low-side-switch dynamic losses

P_{DPAR} – Parasitic capacitance dynamic losses

P_{PER} – Peripheral circuit losses

P_{DYN} – Dynamic losses

P_{IN} – Input power

P_{LOSS} – Power loss

P_{OUT} – Output power

P_{RHSS} – High-side-switch conduction losses

P_{RIND} – Inductor conduction losses

P_{RLSS} – Low-side-switch conduction losses

P_{RPAR} – Parasitic resistance conduction losses

Q – Quality factor

R_{HSS} – High-side-switch series resistance

R_{IN} – Input resistance

R_{IND} – Inductor series resistance

R_{LSS} – Low-side-switch series resistance

R_{PAR} – Parasitic resistance

R_S – Power supply resistance

$R_{S,HSS}$ – High-side-switch sheet resistance

$R_{S,LSS}$ – Low-side-switch sheet resistance

R_{TEG} – Thermoelectric generator resistance

R_{TOFF} – Inductor discharging path resistance

R_{TON} – Inductor charging path resistance

S – Seebeck coefficient

SF – Scaling factor of the geometric pulse

S_N – Seebeck coefficient of the n-type material

S_P – Seebeck coefficient of the p-type material

T – Switching period

T – Temperature

t_D – Inductor idle time

t_{OFF} – Inductor discharging time

t_{ON} – Inductor charging time

t_P – Inverter propagation delay

t_{PULSE} – Pulse width

t_{SP} – Time from the start of the transient until the switching point

t_{SP0} – t_{SP} of $i_L(0)=0$

V_A – Oscillation amplitude

V_D – Drain terminal potential

V_{DD} – Supply voltage generated by the boost converter

V_{DDCS} – Supply voltage generated by the cold starter

v_{GPM1} – Gate potential of transistor PM_1

V_{IN} – Input voltage

$V_{IN,MAX}$ – Maximum input voltage

$V_{IN,MIN}$ – Minimum input voltage

v_L – Inductor voltage

v_M – Voltage at node M

V_{OUT} – Output voltage

V_P – Pinch-off voltage

V_P – Peak amplitude of the square-wave

V_{REF0} – Reference voltage

V_S – Power supply voltage

V_S – Source terminal potential

V_{SP} – Switching-point voltage

V_T – Transistor threshold voltage

V_{TC} –Open-circuit thermocouple voltage

V_{TON} – NMOS equilibrium threshold voltage

V_{TOP} – PMOS equilibrium threshold voltage

V_{TEG} – Thermoelectric generator open-circuit voltage

V_{TO} – Equilibrium threshold voltage

W – MOSFET channel width

W_{HSS} – High-side-switch channel width

W_{LSS} – Low-side-switch channel width

$ZCDE$ – Zero-current detection error

Δt_M – Measurement delay

ΔV_{IN} – Input voltage ripple

ΔV_{OUT} – Output voltage ripple

η_{CONV} – Conversion efficiency

$\eta_{END\text{-}TO\text{-}END}$ – End-to-end efficiency

η_{EXTR} – Extraction efficiency

$\eta_{EXTR,LIM}$ – Extraction efficiency for limited output voltage

η_L – Inductor charging efficiency

η_{ZCS} – Conversion efficiency when compared to ideal zero-current switching

μ_n – Electron mobility

μ_p – Hole mobility

ϕ_t – Thermal voltage

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1 INTRODUCTION

During the 20th century, advances in electronics allowed the development of new consumer products, notably automation, computing and biomedical devices, which had a significant impact on the development of modern society. The communication mechanisms, forms of entertainment and the sharing of knowledge were greatly modified with the availability of broadcast systems such as radio, television and the internet. The introduction of several new types of biomedical equipment enabled new approaches to diagnosis and treatments, contributing to the fast development of medicine. The industry has also evolved with adoption of control systems and robotics, which allow faster production and the development of more complex products.

In the same way as occurred in the past century, the recent developments in electronics are continuously changing several aspects of human life, with new applications that lead to the ever-growing computational capacity of devices. In the internet of things (IoT) scenario, connected devices, such as smart sensors, allow the acquisition of large amounts of data (big data), which can be processed using machine learning techniques, allowing electronic devices to perform more complex tasks [1].

The acquisition of data and the intelligent decision-making capabilities have enabled several new approaches in the development of smart cities, such as the deployment of a smart grid, which can reduce energy consumption and allow distributed generation, intelligent management of waste, noise and pollution monitoring, management of traffic congestion, smart parking and lighting, etc. [2]. Homes and buildings can also benefit, where the IoT devices can be used for the reduction of energy consumption along with entertainment and quality-of-life applications, intelligent automation, etc.

The human body also has a strong potential for several IoT applications related to promoting better quality of life and health, such as aids for sports training, wearable health monitoring devices, ambient assisted living, real-time streaming, etc. [3]. To perform the communication between on-body devices, protocol standards such as IEEE 802.15.6 have been developed, allowing the deployment of short range wireless body area networks [3], for which a low power consumption is the main design requirement.

With several applications for humans, the number of connected devices has been increasing constantly and, by 2010, it had already surpassed the human population [4]. Due to the large number of electronic applications, the interaction with such electronic devices should

be as transparent and uncomplicated as possible. It would be unpractical to manage, recharge or replace batteries for every application; hence, an important requirement for the connected devices is an autonomous energy supply for operation, which allows the device to be independent of any wiring needs or batteries, decreasing maintenance requirements and chemical waste generation, as well as allowing device portability.

In this context, energy harvesting has become an important solution to allow these devices to best fit the requirements of uninterrupted autonomous operation [5], being a feasible solution for power sensor nodes [6], [7] while meeting the requirements of performance and lifetime for such devices. To establish sensor networks, new communication standards such as ZigBee with the Green Power feature [8] have been developed, targeting the use of harvesters as the source of power. In this technology, a message containing the status of a light switch can be transmitted with only 50 uJ, and it can be supplied with several harvesting solutions.

1.1 ENERGY HARVESTING APPROACHES

In the energy harvesting scenario, the environment is exploited as a source to power electronic devices. The most common approaches used for energy harvesting [9] and the amount of ambient power and power harvested by the transducers are detailed for each approach in Table 1.

Table 1 - Energy harvesting approaches and the power level obtained [9].

Source	Source Power	Harvested Power
Ambient light – Indoor	0.1 mW/cm^2	10 $\mu W/cm^2$
Ambient light – Outdoor	100 mW/cm^2	10 mW/cm^2
Vibration/Motion – Human	0.5 mW/cm^2	4 $\mu W/cm^2$
Vibration/Motion - Industrial	1 mW/cm^2	100 $\mu W/cm^2$
Thermal Energy – Human	20 mW/cm^2	30 $\mu W/cm^2$
Thermal Energy - Industrial	100 mW/cm^2	1-10 mW/cm^2
Radiofrequency – Cell phone	0.3 $\mu W/cm^2$	0.1 $\mu W/cm^2$

The voltage level generated by miniature energy harvesting transducers is low and varies widely with the power available in the environment, requiring the use of voltage converters between the main transducer (antenna, thermoelectric generator, solar panel, etc.)

and the device which is being powered, to provide a stable and appropriate voltage level under several conditions of available power (P_{AV}). Hence, voltage converters capable of operation with ultra-low input voltages are essential to enable harvesting from the environment even when the available ambient energy is very low, as is the case of thermoelectric generators (TEG) operating under low temperature gradients or a weak radiofrequency signal captured by small antennas.

Thermal energy harvesting is of particular interest for several on-body applications since it can provide uninterrupted harvesting from human heat at levels superior to those of other energy harvesting approaches. In [10], a complete sensor node solution was powered by a TEG for the first time. The TEG was connected to a human wrist (Figure 1 (a)) and was able to measure and transmit data every 2 s, with an average power consumption of 50–75 μW, which is a feasible amount of power to be supplied by the attached TEG. Other authors have investigated the use of wearable TEGs integrated into clothes to perform human heat harvesting [11], [12], [13] (Figure 1 (b)). However, the use of bulky heat sinks attached to clothes would be unpractical in these applications and larger TEGs can induce the sensation of cold. In addition, the ambient temperature, the walking speed of the person and the wind speed affect considerably the amount of harvested energy.

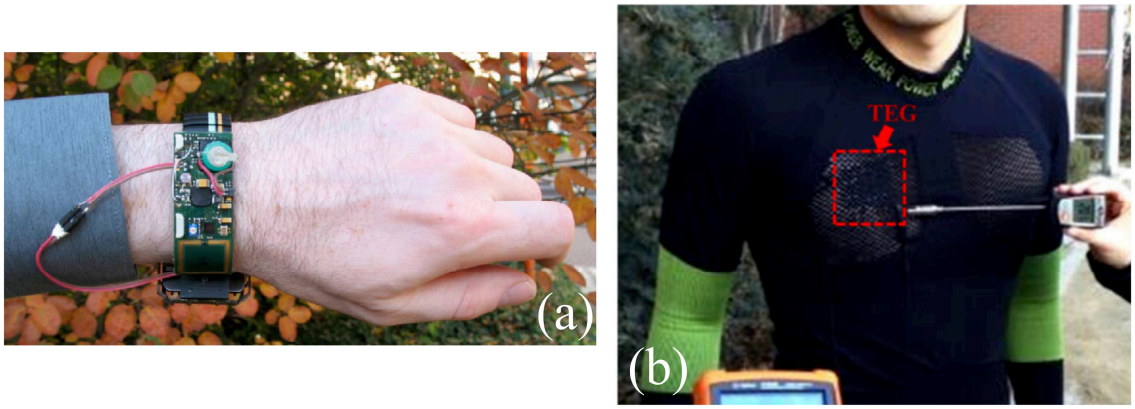


Figure 1 - (a) A sensor node prototype powered by a TEG [11] and (b) a TEG integrated into an athlete's clothes [13].

1.2 THE THERMOELECTRIC GENERATOR

The TEG converts a temperature difference into electricity through a physical process known as the Seebeck effect, which occurs in semiconductor or conductor materials. The basic

structure of a TEG is a thermocouple (Figure 2), which is comprised of two different semiconductor materials, a p-type material with a positive Seebeck coefficient (S_P) and an n-type material with a negative Seebeck coefficient (S_N). The thermocouples are joined by an electrically conductive material and sandwiched between two electrically insulated and thermally conductive plates, which form the cold and hot sides of the device [14]. The thermal gradient causes the diffusion of charge carriers from the hot side to the cold side, generating an electric field due to the gradient of charge carriers, and causing a current to flow once the circuit is closed.

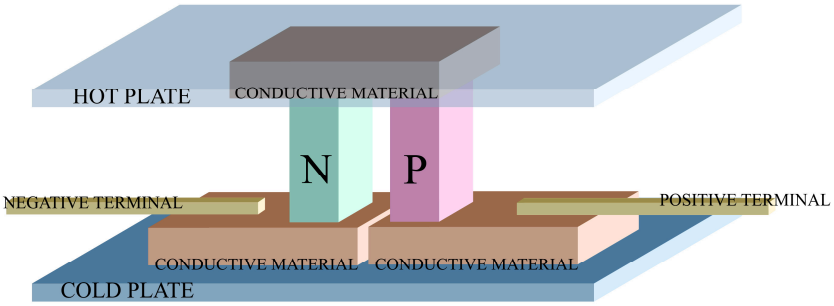


Figure 2 - The basic structure of the thermocouple.

The open-circuit voltage generated by each thermocouple (V_{TC}) is proportional to the temperature difference, and is given by

$$V_{TC} = S\Delta T = \left(S_P - S_N\right)\Delta T \,. \tag{1.1}$$

Due to the low values of the Seebeck coefficient (S), TEGs are generally constructed with a series of thermocouples to increase the voltage (Figure 3). When n_{TC} identical thermocouples are connected in series, the total voltage delivered by the TEG is given by

$$V_{TEG} = n_{TC} V_{TC} \,. \tag{1.2}$$

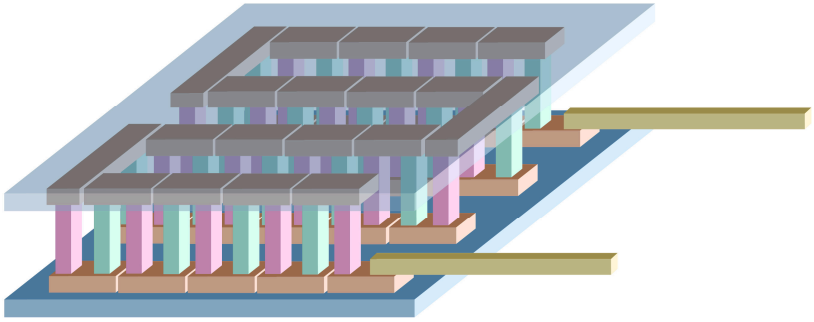


Figure 3 - Common TEG construction using a series of thermocouples.

Although higher voltages can be achieved with the series connection of thermocouples, the increase in the number of devices connected in series also causes the electrical resistance of the TEG and the total TEG area to increase. Hence, standard commercial TEG devices of a few cm^2 (Tellurex, Kryotherm, Marlow, TEGPro) deliver only around 30-60 mV/K under the open-load condition and have a resistance of around 1 to 10 Ω. More recent thin-film technologies achieve a higher Seebeck coefficient for the same TEG area, although the electrical resistance is also increased. The electrical model of a TEG is given in Figure 4. This model was used in this work to design the converter.

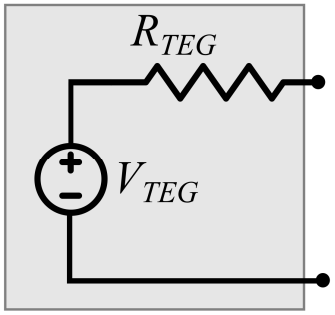


Figure 4 - The equivalent electric circuit of a TEG.

1.3 STATE-OF-THE-ART CONVERTERS FOR THERMAL ENERGY HARVESTING

In a typical energy harvesting application, voltage converters are employed to boost the voltage level generated by the TEGs. The most relevant figures of merit for these converters are generally:

• **Input voltage range** - Due to the typical variations that occur in the availability of ambient power, a wide range of input voltages is important to provide a stable and adequate output voltage under several input conditions;

• **End-to-end efficiency** - The converter should be designed to maximize the extraction of the available power and provide high conversion efficiency. Also, the power budget of the peripheral control circuits should be very low, so that the efficiency is not impaired at low available power (P_{AV});

• **Minimum input voltage** - In order to enable harvesting when the temperature gradients are very low, the minimum input voltage for steady-state operation should also be very low;

• **Startup voltage** - Low startup voltages allow the converter startup and power cycling at typically low P_{AV} levels;

• **Device size** - Since the converters are designed to power IoT devices, a compact form factor using a minimum number of off-chip components and chip area is desirable, increasing device portability and reducing implementation costs.

For energy harvesting applications, the most common types of converters used to achieve voltage boosting are the switched-inductor and switched-capacitor converters [15].

1.3.1 Switched-capacitor converters

Switched-capacitor converters [16]-[20] can be fully integrated, with minimal area requirements, although the minimum input voltage for operation of this type of converter is high (100 mV for [16], which is amongst the lowest input voltages reported for this type of converter). Also, the efficiency is low when compared to switched-inductor converters, especially at low at low input voltages, reaching to only 33% at V_{IN}=100 mV [16] and 23% a V_{IN}=150 mV [17].

1.3.2 Switched-inductor converters

Recent developments in thermal energy harvesting have been focused on low-voltage operation using switched-inductor converters as an efficient means of DC-DC conversion [21]-[46]. Although this type of converter provides high end-to-end efficiency (90.8% reported in [21]), due to low available power, the switching frequency (f_{SW}) is not higher than tens of kilohertz, leading to the need for an off-chip inductor and two off-chip capacitors, as will be explained in Section 2.3.2 and Appendices A and B. Also, this type of converter is not able to self-start at low input voltages, requiring auxiliary cold-starter circuits [47]. According to the design needs, the startup solution can be fully-integrated [21]-[32], which leads to relatively high startup voltages, or may rely on off-chip components with a high quality factor (Q) [33]-[41], for the achievement of low startup voltages.

1.3.2.1 On-chip startup mechanisms

To achieve system startup at 210 mV, in the work described in [22], two cold-starter circuits were used in series. Also, using a clock booster to control the low-side switch (LSS) of

the boost converter, in [23], startup from voltages as low as 190 mV is reported. In [24], a startup circuit based on power-on-reset is presented, in which a finite number of pulses are used to control the LSS of the boost converter, providing startup for a TEG voltage of 220 mV. The startup voltages reported in [22]-[25] are of the same order of magnitude achieved by switched capacitor converters, and are thus not appropriate when the aim is ultra-low-voltage (ULV) startup.

In [26], an oscillator comprised of Schmitt-trigger stages and a cross-coupled rectifier [48] were used, starting up the converter from an input voltage of 70 mV. By means of an inductive-load ring oscillator (ILRO), which uses on-chip inductors and an 8-stage charge pump, the work reported in [27] achieved startup with an input voltage of 65 mV at the cost of 0.65 mm^2 of silicon area for the inductors. Using stacked inverters to implement an on-chip oscillator, similarly to the works reported in [22], [23], and using cross-coupled complementary charge pumps, the approach described in [28] achieves startup for voltages as low as 57 mV, which is the lowest on-chip startup solution for the boost converter reported to date. The low-voltage harvesters described in [26]-[32] allow a trade-off between the minimum startup voltage and the number of off-chip components.

1.3.2.2 Off-chip startup mechanisms

Using off-chip components, such as inductors, capacitors and/or transformers, rather than on-chip components allows the lowering of the minimum voltage for system startup. One common approach to realize the cold starter is the use of a transformer in an LC oscillator, which is reused in the boost converter topology as the main inductor, as reported in [33], [34] and implemented in off-the-shelf products [35], [36]. The startup voltages obtained with this type of cold starter are amongst the lowest reported to date (21 mV for [34]), at the cost of the complex optimization of the transformer in terms of both low voltage startup and efficiency. In order to provide startup at low input voltages and, at the same time, high efficiency during steady-state, a recent publication describes the inclusion of a purpose-built transformer with a third coil, providing independent optimization of startup and efficiency [37]. A three-stage voltage converter is presented in [38]-[40], where an additional auxiliary stage between the steady-state boost converter and the cold starter is introduced, aiming to reduce the loading effects on the cold starter, at the cost of increased off-chip components and circuit complexity. In [41], a dual stage converter is described, where the inductor used in the cold-starter Colpitts

oscillator is reused by the boost converter in steady-state, achieving startup voltages lower than on-chip designs, but still higher than those provided by transformer-based oscillators.

1.3.3 Other converter technologies

Another approach to voltage boosting is the use of a ULV oscillator followed by a rectifier [49], [50]. In this type of converter, the minimum input voltage for startup and operation is low, fulfilling the requirements for ULV harvesting. The minimum input voltage for is only 17 mV for [49] and 10 mV for [50]. The main drawback of this approach is the low conversion efficiency, due to the power-hungry oscillator and the losses in the rectifier. The maximum conversion efficiency achieved is around 11% for [49], which is lower than other conversion approaches used for energy harvesting.

1.3.4 Defining the converter for thermal energy harvesting

In this work, the voltage converter for thermal energy harvesting applications was designed considering the following specifications:

- Achieve startup and operate efficiently at low temperature gradients provided by the human body; thus, the minimum input voltage level should be lower than a few tens of mV;
- Operate efficiently from different types of TEGs, accommodating a wide range of input voltages and commercial R_{TEG} values;
- Provide an output voltage level of around 0.7 to 1 V, which is high enough to supply low-power devices;
- Provide high efficiency when the P_{AV} ranges from the μW to the mW range, which is the common range of power demanded by low-power IoT devices.

Considering the required characteristics, the inductive boost converter was chosen for the implementation of converter architecture, since this converter structure can fulfill all the design specifications. The main drawback of this approach is the use of off-chip components, which are not necessary in switched-capacitor converters.

1.4 CONTRIBUTIONS OF THIS THESIS

In order to cover the whole process of designing an ULV converter for thermal energy harvesting applications, the following topics were proposed and researched:

- Analysis of the inductive boost converter operating under ultra-low-input voltages/high voltage gain and powered by a restricted power supply;
- A converter topology with low quiescent power using a step-by-step voltage buildup;
- An oscillator and charge-pump co-design procedure to minimize the minimum startup voltage of the converter;
- A modified zero-current switching (ZCS) scheme with non-linear time scaling for the modulation of the discharging time of the converter and proper modeling of the measurement delay block, which significantly increases the accuracy of the ZCS scheme.

All of these approaches contribute to the development of the state-of-the art for this type of converters, specifically targeting the following goals:

- The reduction of the minimum input voltage for converter steady-state operation;
- The reduction of the startup voltage of the converter;
- The maximization of both the extraction and conversion efficiencies across the whole input voltage range.

1.5 ORGANIZATION OF THE MANUSCRIPT

This manuscript is divided as follows: Chapter 2 presents a mathematical model of the boost converter under ULV operation for application to energy harvesting converters. In Chapter 3, the converter architecture and the peripheral blocks are detailed. The designing of the startup mechanism is detailed in Chapter 4, along with the co-design of the ULV oscillator and the rectifier. Chapter 5 describes the innovative ZCS scheme that improves the conversion efficiency as compared to other realizations. In Chapter 6, the experimental results of the fabricated chip are reported. The main results of this thesis and final conclusions can be found in Chapter 7. Supporting material and the list of publications are provided in the Appendices.

2 THE INDUCTIVE BOOST CONVERTER FOR THERMAL ENERGY HARVESTING APPLICATIONS

For thermal energy harvesting applications, the inductive boost converter shown in Figure 5 is commonly used as a means of DC-DC conversion.

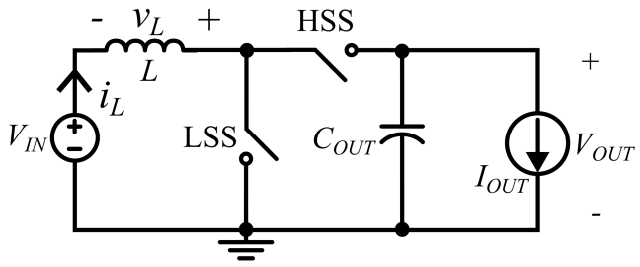


Figure 5 - Inductive boost converter topology.

The boost converter can be operated in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM, the inductor current is always greater than zero and the cycle of operation of the converter (T) is divided into two phases, as seen in Figure 6 (a), where

$$t_{ON} = DT \text{ , } t_{OFF} = D'T \text{ .} \tag{2.1}$$

During t_{ON}, the LSS is closed and the high-side switch (HSS) is open; thus, the inductor is charged by V_{IN}. During t_{OFF}, the LSS is open and the HSS is closed; therefore, part of the inductor energy as well as the energy from V_{IN} is transferred to the output capacitor and the load.

In DCM operation (Figure 6 (b)), there is an additional phase when both switches are open.

$$t_D = D''T \text{ .} \tag{2.2}$$

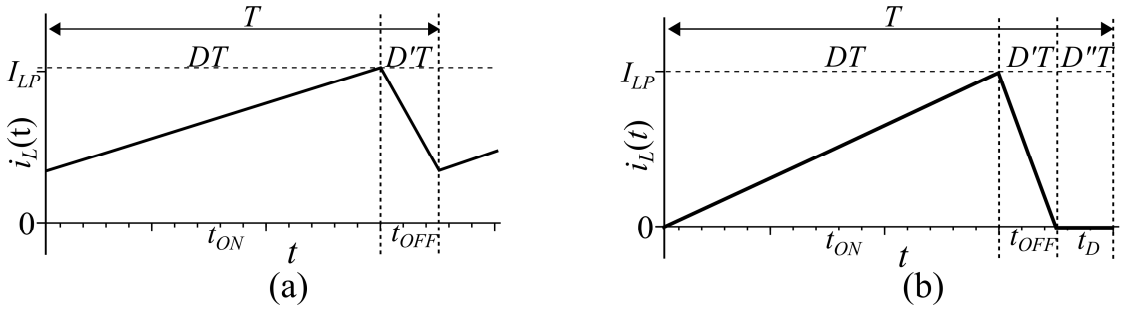


Figure 6 - Inductor current for (a) CCM and (b) DCM operation.

2.1 DCM VS CCM OPERATION

In order to select the use of either DCM or CCM, the inductor charging efficiency was analyzed. In Figure 7, the inductor is charged by an ideal voltage source. The total path resistance is R [51]. The inductor voltage and current, respectively, are given by

$$v_L(t) = \left(V_S - Ri_L(0)\right)e^{-t\frac{R}{L}}, \tag{2.3}$$

$$i_L(t) = \frac{V_S}{R} + \left(i_L(0) - \frac{V_S}{R}\right)e^{-t\frac{R}{L}}. \tag{2.4}$$

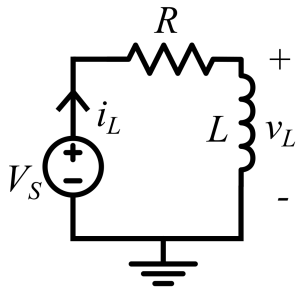


Figure 7 - Circuit used for the analysis of the inductor charging efficiency.

For any given charging time, the energy delivered by the power supply is given by

$$E_S(t) = \int_0^t V_S i_L(t)dt = \int_0^t V_S\left[\frac{V_S}{R} + \left(i_L(0) - \frac{V_S}{R}\right)e^{-t\frac{R}{L}}\right]dt \tag{2.5}$$

$$= \frac{V_S^2}{R}t + \left(V_S i_L(0) - \frac{V_S^2}{R}\right)\frac{L}{R}\left(1 - e^{-t\frac{R}{L}}\right). \tag{2.6}$$

Similarly, the energy transferred to the inductor is calculated by

$$E_L(t) = \int_0^t\left[\left(V_S - Ri_L(0)\right)e^{-t\frac{R}{L}}\right]\left[\frac{V_S}{R} - \frac{1}{R}\left(V_S - Ri_L(0)\right)e^{-t\frac{R}{L}}\right]dt\,. \tag{2.7}$$

Thus, the inductor charging efficiency is given by

$$\eta_L(t) = \frac{E_L(t)}{E_S(t)} = \frac{\left(1 - \frac{i_L(0)R}{V_S}\right)\left[\left(\frac{i_L(0)R}{V_S} + 1\right) + \left(1 - \frac{i_L(0)R}{V_S}\right)e^{-2t\frac{R}{L}} - 2e^{-t\frac{R}{L}}\right]}{2\left(\frac{tR}{L} + \left(\frac{i_L(0)R}{V_S} - 1\right)\left(1 - e^{-t\frac{R}{L}}\right)\right)}. \tag{2.8}$$

In Figure 8, the inductor charging efficiency is plotted as a function of $i_L(0)$ normalized to V_S/R for different values of tR/L. For fixed circuit parameters, the efficiency is

higher for lower values of $i_L(0)$, reaching the maximum value when $t<<L/R$. Since the charging of the inductor starting at $i_L(0)$ =0 is always the point of highest efficiency, the DCM was chosen to maximize the energy transfer.

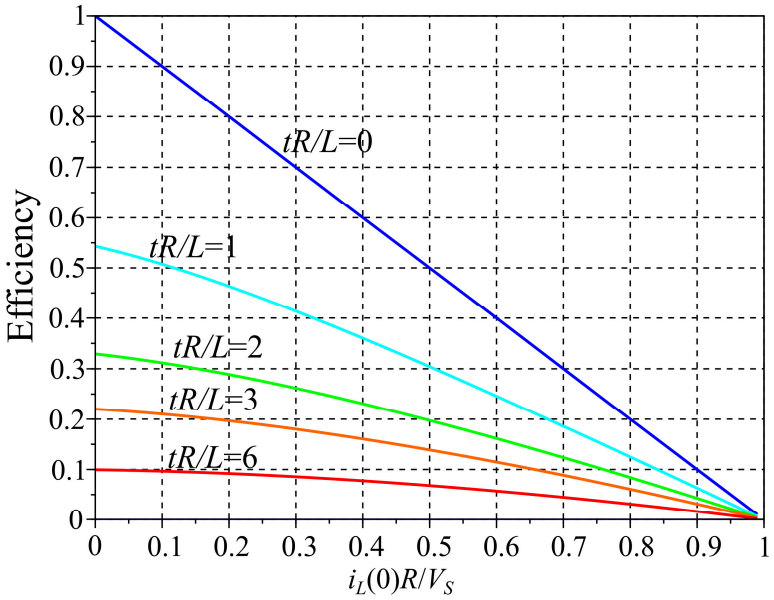


Figure 8 - Inductor charging efficiency.

2.2 THE IDEAL BOOST CONVERTER IN DISCONTINUOUS CONDUCTION MODE

During t_{ON}, the circuit shown in Figure 5 is equivalent to that shown in Figure 9. During this phase, V_{IN} charges the inductor and the output capacitor is responsible for providing the load current. For the ideal converter, the inductor current is given [51], [52] by

$$i_L(t) = \frac{V_{IN}}{L} t\,; \tag{2.9}$$

thus, the peak inductor current is expressed by

$$I_{LP} = \frac{V_{IN}}{L} t_{ON} = \frac{V_{IN}}{L} DT\,. \tag{2.10}$$

Since the output capacitor supplies current to the load, in this phase we have

$$i_{COUT}(t) = C_{OUT} \frac{dV_{OUT}(t)}{dt} = -I_{OUT}\,. \tag{2.11}$$

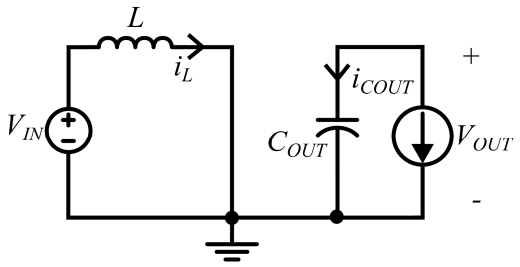


Figure 9 - Equivalent circuit of the inductive boost converter during t_{ON}.

Figure 10 represents the circuit during t_{OFF}. During this phase, the inductor energy is transferred to both the output capacitor and the load; therefore

$$i_L(t) = \frac{V_{IN}}{L} t_{ON} + \left(\frac{V_{OUT} - V_{IN}}{L} \right) \left(t_{ON} - t \right), \tag{2.12}$$

$$i_{COUT}(t) = i_L(t) - I_{OUT}. \tag{2.13}$$

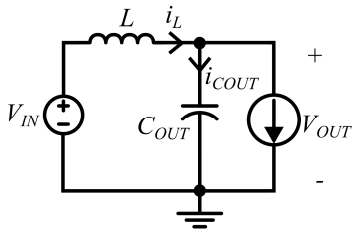


Figure 10 - Equivalent circuit of the inductive boost converter during t_{OFF}.

During t_D, the circuit reduces to that shown in Figure 11; thus

$$i_L(t) = 0, \tag{2.14}$$

$$i_{COUT}(t) = -I_{OUT}. \tag{2.15}$$

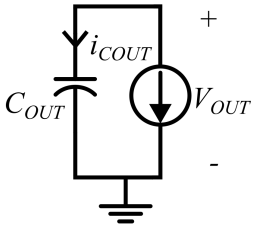


Figure 11 - Equivalent circuit of the inductive boost converter during t_D.

Assuming a full conversion period, the average inductor current is given by

$$\overline{i_L} = \frac{I_{LP}\left(t_{ON} + t_{OFF} \right)}{2T} = \frac{V_{IN} DT \left(D + D' \right)}{2L}. \tag{2.16}$$

Applying charge balance at C_{OUT}, the total charge provided by the inductor during t_{OFF} is delivered to the load; therefore

$$I_{OUT} = \frac{I_{LP} t_{OFF}}{2T} = \frac{V_{IN} DD'T}{2L}. \tag{2.17}$$

2.2.1 Gain factor

The voltage gain, conversion gain or the gain factor (M) of the boost converter is defined as

$$M = \frac{V_{OUT}}{V_{IN}}. \tag{2.18}$$

Applying the volt-second balance to the inductor, we have

$$\int_0^T v_L(t)dt = V_{IN} t_{ON} + \left(V_{IN} - V_{OUT}\right)\left(t_{OFF}\right) = 0; \tag{2.19}$$

hence

$$M = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{t_{ON}}{t_{OFF}} = 1 + \frac{D}{D'}. \tag{2.20}$$

Replacing D' given by (2.17) in (2.20), we obtain an expression for M of the boost converter in DCM

$$M = 1 + \frac{D^2 T V_{IN}}{2LI_{OUT}} = 1 + \frac{D^2 V_{IN}}{2Lf_{SW} I_{OUT}}. \tag{2.21}$$

For low-voltage energy harvesting applications, where $V_{IN} << V_{OUT}$, we can approximate (2.21) by

$$M \cong \frac{D^2 V_{IN}}{2Lf_{SW} I_{OUT}}. \tag{2.22}$$

2.3 HARVESTING FROM A LOW-VOLTAGE POWER SUPPLY

The TEG can be represented by an ideal power supply with a series resistance, as seen in Figure 12.

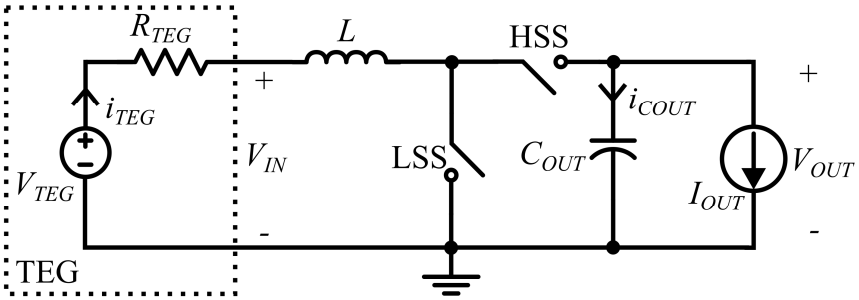


Figure 12 - Inductive boost converter connected to a TEG.

The available power, which is the maximum power that can be extracted from the TEG, is given by

$$P_{AV} = \frac{V_{TEG}^{\,2}}{4R_{TEG}}. \tag{2.23}$$

In energy harvesting applications, it is desired that all P_{AV} be delivered to the converter, maximizing the extraction efficiency, which is defined as

$$\eta_{EXTR} = \frac{P_{IN}}{P_{AV}}. \tag{2.24}$$

2.3.1 Peak inductor current for maximum extraction efficiency

Assuming that the input voltage is constant, we have

$$P_{IN} = \frac{1}{T}\int_0^T p_{IN}(t)dt = \frac{1}{T}\int_0^T \left[V_{TEG} - R_{TEG} i_{TEG}(t)\right] i_L(t)dt\,. \tag{2.25}$$

Since the power supply current is equal to the inductor current, using expressions (2.25), (2.9), (2.10) and (2.12) we obtain

$$P_{IN} = \frac{1}{T}\left\{\begin{array}{l}\displaystyle\int_0^{t_{ON}}\left[V_{TEG} - R_{TEG}\left(\frac{I_{LP}t}{t_{ON}}\right)\right]\frac{I_{LP}t}{t_{ON}}dt \\ \displaystyle+\int_{t_{ON}}^{t_{ON}+t_{OFF}}\left\{V_{TEG} - R_{TEG}\left[\frac{I_{LP}\left(t_{ON}+t_{OFF}-t\right)}{t_{OFF}}\right]\right\}\left[\frac{I_{LP}\left(t_{ON}+t_{OFF}-t\right)}{t_{OFF}}\right]dt\end{array}\right\} \tag{2.26}$$

$$= \left(\frac{t_{ON}+t_{OFF}}{T}\right)\left(\frac{V_{TEG}I_{LP}}{2} - R_{TEG}\frac{I_{LP}^{\,2}}{3}\right). \tag{2.27}$$

Replacing (2.27) in (2.24) gives

$$\eta_{extr} = \frac{\left(\frac{t_{ON}+t_{OFF}}{T}\right)\left(\frac{V_{TEG}I_{LP}}{2} - R_{TEG}\frac{{I_{LP}}^2}{3}\right)}{\frac{{V_{TEG}}^2}{4R_{TEG}}}. \tag{2.28}$$

Now the peak inductor current (I_{LP}) that delivers the maximum extraction efficiency can be calculated considering that

$$\frac{\partial \eta_{extr}}{\partial I_{LP}} = \left(\frac{\frac{t_{ON}+t_{OFF}}{T}}{\frac{{V_{TEG}}^2}{4R_{TEG}}}\right)\left(\frac{V_{TEG}}{2} - \frac{2}{3}R_{TEG}I_{LP}\right) = 0; \tag{2.29}$$

thus

$$I_{LP,MAX} = \frac{3}{4}\frac{V_{TEG}}{R_{TEG}}. \tag{2.30}$$

Substituting (2.30) in (2.28), we have

$$\eta_{extr} = \left(\frac{t_{ON}+t_{OFF}}{T}\right)\left(\frac{3}{4}\right). \tag{2.31}$$

For the case of zero dead time (t_D=0→ t_{ON}+t_{OFF}=T), the extraction efficiency reaches its maximum value of 75% for the circuit in Figure 12.

2.3.1.1 Modified Boost Converter

With the addition of a capacitor at the input of the converter (Figure 13) the input ripple caused by R_{TEG} can be made negligible.

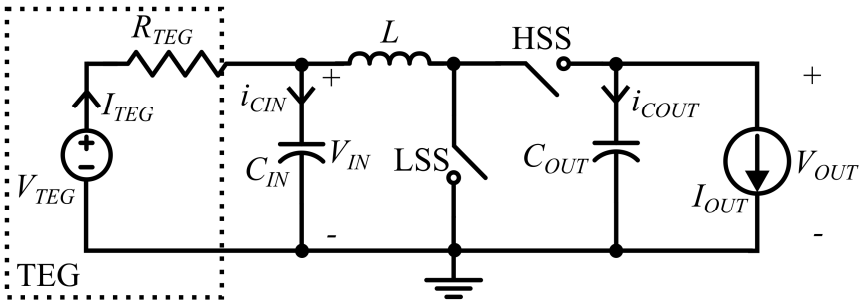


Figure 13 - Inductive boost converter using an input capacitor.

In this configuration, the mean TEG current is equal to the mean inductor current. Applying the same methodology used for the circuit without an input capacitor, the peak

inductor current (I_{LP}) that delivers maximum efficiency and the extraction efficiency are given, respectively, by

$$I_{LP,MAX} = \frac{V_{TEG}T}{R_{TEG}\left(t_{ON}+t_{OFF}\right)}, \tag{2.32}$$

$$\eta_{EXTR} = \frac{\frac{V_{TEG}I_{LP}\left(t_{ON}+t_{OFF}\right)}{2T} - R_{TEG}\frac{{I_{LP}}^2\left(t_{ON}+t_{OFF}\right)^2}{4T^2}}{\frac{{V_{TEG}}^2}{4R_{TEG}}}. \tag{2.33}$$

Substituting (2.32) in (2.33), the maximum extraction efficiency is 100% regardless of the parameters involved. This derivation leads to the conclusion that an input capacitor is absolutely necessary for maximizing the extraction efficiency when harvesting from a restricted power supply, as is the case of an energy harvesting application. Appendix A provides expressions for calculating the input capacitor as a function of the specified input ripple.

2.3.2 Converter input impedance for maximum extraction

Controlling the inductor peak current to achieve the maximum power point tracking (MPPT) would require a complex solution. Thus, one solution to perform the MPPT is to match the input impedance of the converter to the internal resistance of the power supply. Under this condition, we have

$$R_{IN} = R_{TEG}, \tag{2.34}$$

$$V_{IN} = \frac{V_{TEG}}{2}, \tag{2.35}$$

$$I_{TEG} = \frac{V_{TEG}}{2R_{TEG}}. \tag{2.36}$$

In order to express the input impedance of the converter as a function of other design parameters, we analyzed the energy stored in the inductor for each cycle of operation. During t_{OFF}, the total energy per cycle transferred from the inductor to the output is given by

$$E_L = \frac{L{I_{LP}}^2}{2}, \tag{2.37}$$

where I_{LP} is given by (2.10); therefore

$$E_L = \frac{\left(V_{IN}t_{ON}\right)^2}{2L}. \tag{2.38}$$

Since the converter is assumed to be lossless, the energy transferred by the inductor to the output is equal to the energy provided by the TEG during one cycle of operation, leading to

$$\frac{\left(V_{IN}t_{ON}\right)^2}{2L} = \frac{{V_{IN}}^2}{R_{IN}}T\,, \tag{2.39}$$

or

$$R_{IN} = \frac{2L}{t_{ON}D} = \frac{2Lf_{SW}}{D^2}\,. \tag{2.40}$$

In order to track the maximum power point, one must have R_{IN}=R_{TEG}; hence, (2.40) can be rewritten as

$$Lf_{SW} = \frac{D^2 R_{TEG}}{2}\,. \tag{2.41}$$

Since the internal resistance of the TEG is known and is approximately constant along the thermal gradient operational range, the inductor and frequency can be tuned to extract the available power.

Assuming that the system is matched for MPPT using (2.41), the gain factor (2.22) can be rewritten as

$$M \cong \sqrt{\frac{R_L}{R_{TEG}}}\,. \tag{2.42}$$

2.4 THE REAL BOOST CONVERTER IN DISCONTINUOUS CONDUCTION MODE

Up to this point, the boost converter was assumed to be lossless. Hence, the input power is equal to the output power. For the development of an appropriate model for the real boost converter, in this section, non-idealities are taken into account.

For a lossy converter, the output power is related to the input power by

$$P_{OUT} = P_{IN} - P_{LOSS}\,. \tag{2.43}$$

The conversion efficiency and the end-to-end efficiency are defined, respectively, as

$$\eta_{CONV} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}}\,, \tag{2.44}$$

$$\eta_{END-TO-END} = \eta_{EXTR}\eta_{CONV} = \frac{P_{OUT}}{P_{AV}}\,. \tag{2.45}$$

For energy harvesting applications, expression (2.45) is a more useful figure of merit than the conventional conversion efficiency (2.44), since it also takes into account the

extraction efficiency. The maximization of the extraction efficiency is achieved through the methods explained in Section 2.3.2. In order to maximize the conversion efficiency, the power losses in the converter should be modeled and minimized.

2.4.1 Converter Losses

The converter losses are divided into three main components: conduction losses, dynamic losses and losses due to the power consumption in the peripheral blocks.

$$P_{LOSS} = P_{COND} + P_{DYN} + P_{PER}. \tag{2.46}$$

2.4.1.1Conduction Losses

The conduction losses (P_{COND}) are due to the parasitic resistance in the components and metal tracks. We can simplify them as

$$P_{COND} \approx P_{RIND} + P_{RLSS} + P_{RHSS}, \tag{2.47}$$

where P_{RIND} represents the inductor conduction losses, P_{RLLS} the conduction losses in the LSS series resistance (R_{LSS}) and P_{RHSS} the conduction losses in the HSS series resistance (R_{HSS}). Assuming that the inductor time constant is much higher than the clock period, we have

$$P_{RIND} = \frac{1}{T}\int_0^T R_{IND} i_L(t)^2 dt \tag{2.48}$$

$$= \frac{R_{IND}}{T}\left\{\int_0^{t_{ON}} \left(\frac{I_{LP} t}{t_{ON}}\right)^2 dt + \int_{t_{ON}}^{t_{ON}+t_{OFF}} \left[\frac{I_{LP}\left(t_{ON}+t_{OFF}-t\right)}{t_{OFF}}\right]^2 dt\right\} \tag{2.49}$$

$$= \frac{R_{IND} {I_{LP}}^2 \left(D + D'\right)}{3}. \tag{2.50}$$

The substitution of (2.10) in (2.50) yields

$$P_{RIND} = \frac{R_{IND} {V_{IN}}^2 D^2 \left(D + D'\right)}{3\left(Lf_{SW}\right)^2} = \frac{4R_{IND} {V_{IN}}^2}{3{R_{TEG}}^2 D}. \tag{2.51}$$

Similarly, we can find the conduction losses in the switches

$$P_{RLSS} = \frac{R_{LSS} {V_{IN}}^2 D^3}{3\left(Lf_{SW}\right)^2} = \frac{4R_{S,LSS} L_{LSS} {V_{IN}}^2}{3W_{LSS} {R_{TEG}}^2 D}, \tag{2.52}$$

$$P_{RHSS} = \frac{R_{HSS} V_{IN}^{\ 2} D^2 D'}{3\left(L f_{SW}\right)^2} = \frac{4 R_{S,HSS} L_{HSS} V_{IN}^{\ 2} D'}{3 W_{HSS} R_{TEG}^{\ 2} D^2}. \tag{2.53}$$

The sheet resistances $R_{S,LSS}$ and $R_{S,HSS}$ of the switches can be calculated using the MOSFET model in strong inversion presented in Appendix C.

Using (2.51) through (2.53), the total conduction losses can be expresses by

$$P_{COND} \approx \frac{4 V_{IN}^{\ 2}}{3 D R_{TEG}^{\ 2}} \left[R_{IND} + \frac{R_{S,LSS} L_{LSS}}{W_{LSS}} + \frac{1}{M-1}\left(R_{IND} + \frac{R_{S,HSS} L_{HSS}}{W_{HSS}} \right) \right]. \tag{2.54}$$

Under high conversion gain, (2.54) can be reduced to

$$P_{COND} \approx \frac{4 V_{IN}^{\ 2}}{3 D R_{TEG}^{\ 2}} \left[R_{IND} + \frac{R_{S,LSS} L_{LSS}}{W_{LSS}} \right]. \tag{2.55}$$

2.4.1.2 Dynamic losses

The dynamic losses are due to the switching of high capacitance nodes. The most relevant capacitances are the gates of the LSS and HSS and the sum of the remaining parasitic capacitances connected to the clock (C_{PAR}). Hence, the dynamic losses can be written as

$$P_{DYN} = P_{DLSS} + P_{DHSS} + P_{DPAR}, \tag{2.56}$$

$$P_{DLSS} = \frac{C_{OX} W_{LSS} L_{LSS} f_{SW} V_{OUT}^{\ 2}}{2}, \tag{2.57}$$

$$P_{DHSS} = \frac{C_{OX} W_{HSS} L_{HSS} f_{SW} V_{OUT}^{\ 2}}{2}, \tag{2.58}$$

$$P_{DPAR} = \frac{C_{PAR} f_{SW} V_{OUT}^{\ 2}}{2}, \tag{2.59}$$

where C_{OX} is the oxide capacitance per unit of area. Thus, the total dynamic losses can be expressed as

$$P_{DYN} = \frac{f_{SW} V_{OUT}^{\ 2}}{2}\left(C_{LLSS} W_{LSS} + C_{LHSS} W_{HSS} + C_{PAR} \right), \tag{2.60}$$

where C_{LLSS} and C_{LHSS} are the linear capacitances of the MOS switches per unit of width.

2.4.1.3 Losses in peripheral blocks

These losses represent the static power consumption that the peripheral blocks need for circuit operation (control circuit, reference circuits, clock circuit, etc.). Careful design and application of each of the building blocks should be carried out to keep these losses much lower than the minimum specified P_{AV}.

2.4.1.4 Sizing of boost switches

The size of the boost switches must be chosen in order to minimize the sum of the dynamic and conduction losses; therefore, making the conduction losses equal to the dynamic losses for each of the switches yields the optimum transistor width, given by

$$W_{LSS} = \frac{V_{IN}}{R_{TEG}} \frac{2}{V_{OUT}} \sqrt{\frac{2R_{S,LSS}}{3Df_{SW}C_{OX}}}, \tag{2.61}$$

$$W_{HSS} = \frac{V_{IN}}{R_{TEG}} \frac{2}{V_{OUT}} \sqrt{\frac{2V_{IN}R_{S,HSS}}{3D(V_{OUT}-V_{IN})f_{SW}C_{OX}}} \approx W_{LSS}\sqrt{\frac{R_{S,HSS}}{R_{S,LSS}M}}. \tag{2.62}$$

Using these expressions, the optimization of the boost converter switches can be performed once the V_{IN} range and commercial R_{TEG} range are defined. In Figure 14, the widths of the LSS and the HSS are plotted as a function of R_{TEG} and V_{IN} for the 130 nm technology.

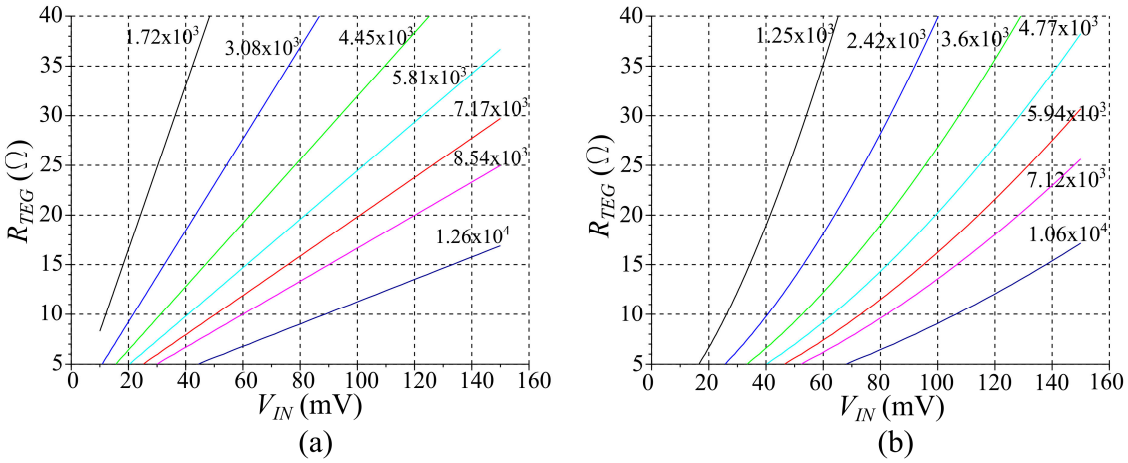


Figure 14 - Optimum (a) W_{LSS} (µm) and (b) W_{HSS} (µm) as a function of R_{TEG} and V_{IN} for the 130 nm technology. V_{OUT}=1 V, f_{SW}=40 kHz.

2.4.2 Non-ideal converter equivalent circuit and expressions

A first-order equivalent circuit of the non-ideal boost converter that includes the parasitic resistance of the components is shown in Figure 15. In this model, the peripheral and dynamic losses, which are usually negligible for an efficient converter, are neglected. The input and output capacitors are assumed to have negligible equivalent series resistance and high capacitances and thus V_{IN} and V_{OUT} are constant, which is a realistic assumption due to the availability of off-the-shelf capacitors with a high quality factor.

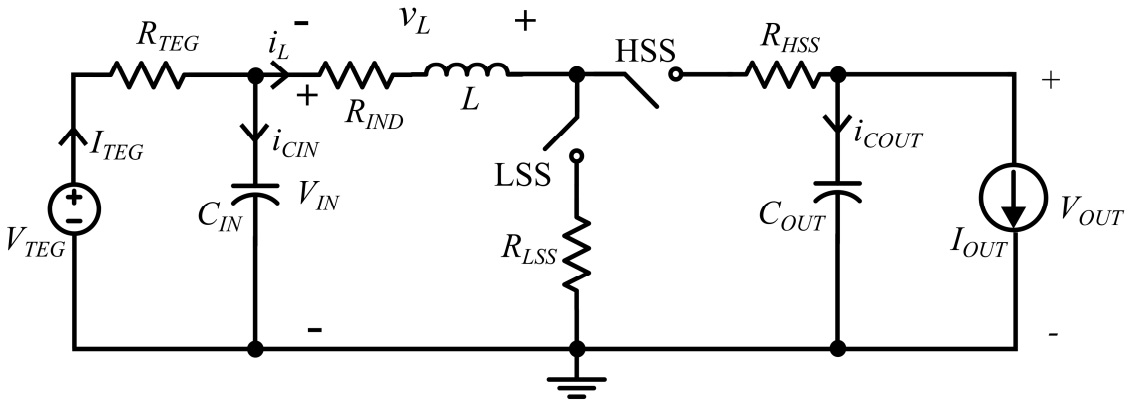


Figure 15 - Model of the inductive boost converter.

For the equivalent circuit in Figure 15, the inductor current during t_{ON} is given by

$$i_L(t) = \frac{V_{IN}}{R_{TON}}\left(1 - e^{-t\frac{R_{TON}}{L}}\right) = \frac{I_{LP,IDEAL}L}{t_{ON}R_{TON}}\left(1 - e^{-t\frac{R_{TON}}{L}}\right). \tag{2.63}$$

where $I_{LP,IDEAL}$ is the peak current for the ideal converter, which is given by (2.10), and R_{TON} is the equivalent series resistance of the inductor-current path during t_{ON}, which can be approximated by

$$R_{TON} \approx R_{IND} + R_{LSS}. \tag{2.64}$$

Similarly, the equivalent series resistance of the inductor-current path during t_{OFF} can be approximated by

$$R_{TOFF} \approx R_{IND} + R_{HSS}. \tag{2.65}$$

Since for ULV energy harvesting applications $V_{IN} << V_{OUT}$ or $t_{OFF} << t_{ON}$, and R_{LSS} is of the same order of magnitude as R_{HSS}, we assume that the discharge of the inductor during t_{OFF} is linear.

To find an expression for the voltage gain of the converter, we apply charge balance to C_{OUT} and volt-second balance to the inductor, and I_{LP} given by (2.63) is used when $t=t_{ON}$, which yields

$$M = 1 - \frac{R_{TOFF}I_{OUT}\left(1 - e^{-t_{ON}\frac{R_{TON}}{L}}\right)}{2R_{TON}I_{OUT}} + \frac{V_{IN}L\left(1 - e^{-t_{ON}\frac{R_{TON}}{L}}\right)^2}{2{R_{TON}}^2 I_{OUT}T}. \tag{2.66}$$

Under high conversion gain and assuming $R_{TON} \approx R_{TOFF}$, expression (2.66) can be rewritten in terms of the ideal conversion gain (M_{IDEAL}) given by (2.22), yielding

$$M \approx \left[\frac{L}{t_{ON} R_{TON}} \left(1 - e^{-t_{ON} \frac{R_{TON}}{L}} \right) \right]^2 M_{IDEAL} . \tag{2.67}$$

In order to obtain the Lf_{SW} expression, we assume that the energy delivered by the inductor during t_{OFF} is approximately the harvested energy at the input minus the energy lost in R_{TON}; thus

$$E_{IN} = E_L + E_R = \frac{L I_{LP}^{\ 2}}{2} + T R_{TON} \overline{i_L}^{2} , \tag{2.68}$$

which yields

$$R_{IN} = \frac{4 R_{TON}^{\ 2}}{\left(2 L f_{SW} + R_{TON} D^2 \right) \left(1 - e^{-t_{ON} \frac{R_{TON}}{L}} \right)^2} . \tag{2.69}$$

For low values of $t_{ON}R_{TON}/L$, we express (2.69) in terms of $R_{IN,IDEAL}$ which is given by (2.40), yielding

$$R_{IN} = \frac{R_{IN,IDEAL}}{\left(1 + \frac{R_{TON}}{R_{IN,IDEAL}} \right)} . \tag{2.70}$$

Setting R_{IN}=R_{TEG} and using the value of the Lf_{SW} product of the ideal converter given by (2.41), gives

$$Lf_{SW} = D^2 R_{TEG} \left(\frac{1 + \sqrt{1 + \frac{4 R_{TON}}{R_{TEG}}}}{4} \right) = \left(Lf_{SW} \right)_{IDEAL} \left(\frac{1 + \sqrt{1 + \frac{4 R_{TON}}{R_{TEG}}}}{2} \right) . \tag{2.71}$$

Using expressions (2.63), (2.67), (2.70) and (2.71), the deviations of the main converter parameters due to the non-idealities are plotted in Figure 16. When designing the converter, the deviation of these parameters can be evaluated once D, f_{SW}, R_{TEG} and L are defined and R_{IND} and R_{LSS} are measured or estimated by datasheet or technological parameters values. The knowledge of these parameter deviations is especially important to correctly set the MPPT for the non-ideal converter.

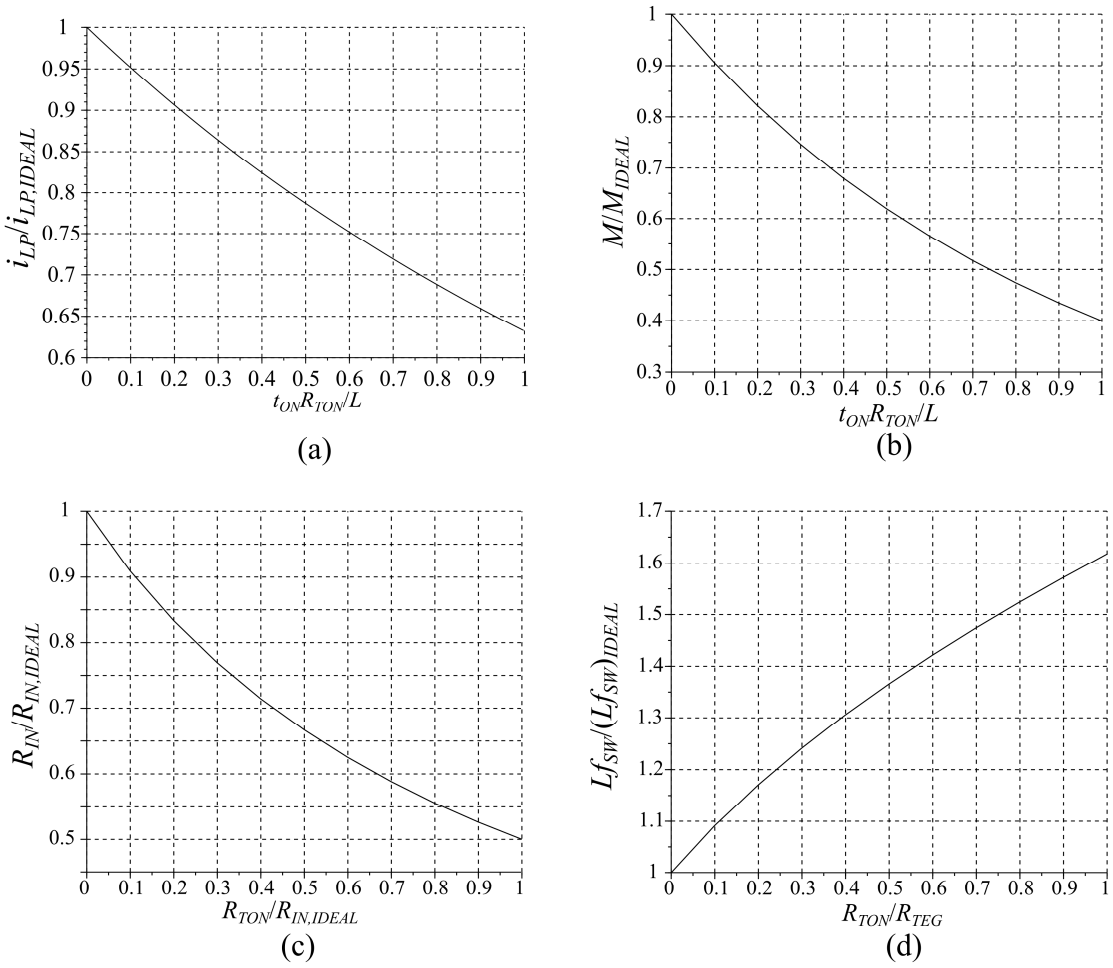


Figure 16 - Normalized (a) peak inductor current during t_{ON}, (b) voltage gain, (c) input resistance and (d) Lf_{SW} product for the non-ideal boost converter.

3 CONVERTER ARCHITECTURE

Using the model detailed in Chapter 2, a boost converter for ULV thermal energy harvesting applications was designed and integrated. A block diagram of the converter architecture is shown in Figure 17.

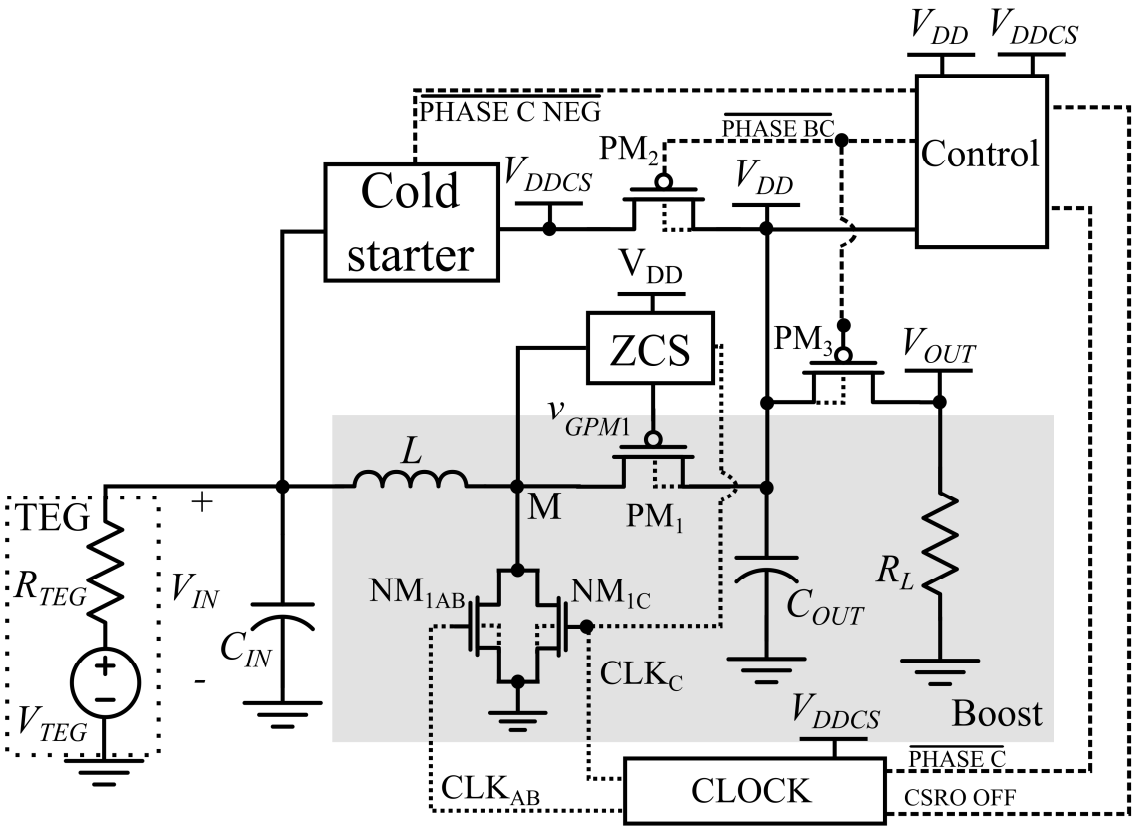


Figure 17 - Developed converter topology.

The converter is comprised of a cold starter, control and clock circuits, a zero-current switching (ZCS) block and the main boost converter. PM_1 is the HSS of the boost converter, while $NM1_{AB}$ and NM_{1C} are the LSSs used during startup and steady-state operation, respectively.

The cold starter is used during startup to establish a temporary supply voltage (V_{DDCS}) at the beginning of the converter operation to power the clock circuit and part of the control block. The main requirement for the cold starter is to provide V_{DDCS} of approximately 500 mV and a current of 100 nA, enabling the switching of the converter by the clock circuit. The complete design of the cold starter is detailed in Chapter 4.

A five-stage current-starved ring oscillator (CSRO) is used as the clock for the boost converter, performing the switching of the converter at a constant duty cycle (D). For the converter control, hysteretic comparators with static power consumption around 55 nW at V_{DD}=1 V were designed. Detailed information on the control and clock circuits is provided in Sections 3.3 and 3.4, respectively.

A ZCS scheme is used to guarantee efficient DCM operation for both low and high input voltages, generating a pulse that keeps PM_1 open during t_{ON} and t_D and closed during t_{OFF}. The ZCS scheme is detailed in Chapter 5.

The sizes of the transistors used for the converter switches are provided in Table 2.

Table 2 - Sizes of the transistors of the converter switches.

Device	Type	W (μm)	L (nm)
$MN1_{AB}$	Low-VT (LVT) NMOS	60x20	120
MN_{1C}	LVT NMOS	150x20	120
PM_1	Standard PMOS	120x20	120
PM_2	Standard PMOS	60x20	120
PM_3	Standard PMOS	150x20	120

3.1 V_{DD} BUILDUP

Once the converter starts up, it commutes between three distinct phases of operation, building up the V_{DD} voltage from zero volt to steady-state operation.

•**Phase A** - Once the primary source (V_{TEG}) is connected to the converter input, the cold starter is turned on, establishing the voltage V_{DDCS} which powers the clock circuit; hence, providing the switching of the boost converter, giving rise to the buildup of node V_{DD}. During this phase, node V_{DDCS} powers only the clock circuit and some logic circuits which are necessary to keep switches PM_2 and PM_3 open. The equivalent circuit in phase A is shown in Figure 18.

The load is disconnected from the output to avoid unnecessary consumption during startup; hence, V_{OUT} = 0 V. In order to reduce the dynamic losses, a small switch (NM_{1AB}), with an area close to a third that of NM_{1C}, is used for the LSS during startup. The dynamic losses of the LSS, which impose a significant load at the cold starter output node (V_{DDCS}), should be minimized to achieve a low startup voltage. A narrower switch increases the conduction losses,

but this is not of concern with regard to the inefficient cold starter, since these losses are supplied by the TEG directly. During this phase, the ZCS block is bypassed and $v_{GPM1}=V_{DD}$; thus, switch PM_1 is equivalent to a diode connected MOSFET.

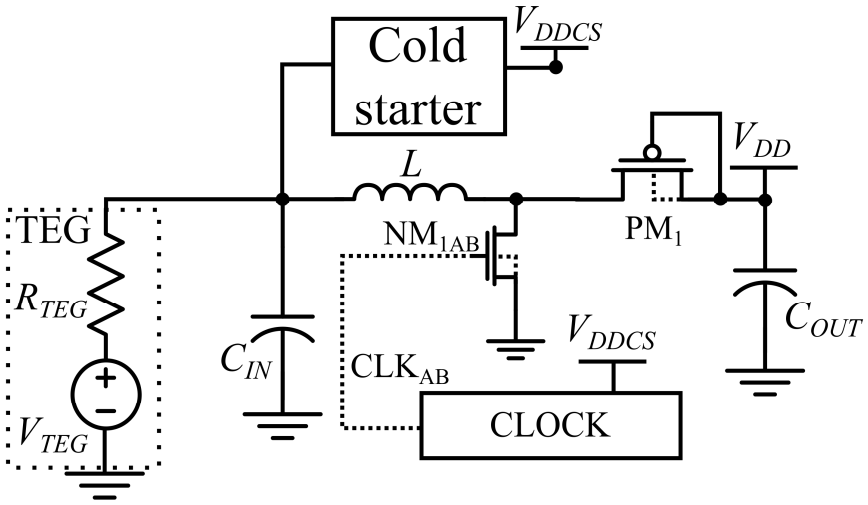


Figure 18 - Converter equivalent circuit during Phase A.

•**Phase B** - This phase starts at V_{DD} close to 530 mV. During this phase, V_{DD} and V_{DDCS} are connected to each other. Node V_{DD} is now responsible for powering the whole circuit, as represented in Figure 19. The load is connected to the output, thus, $V_{OUT}=V_{DD}=V_{DDCS}$.

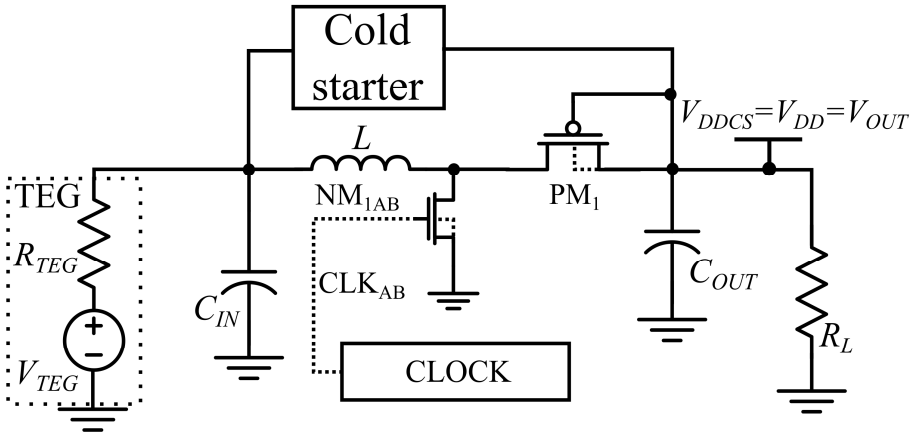


Figure 19 - Converter equivalent circuit during Phase B.

•**Phase C** - When V_{DD} equals 660 mV, the cold starter is turned off to improve the circuit efficiency. Switch NM_{1AB} is replaced by a wider switch, NM_{1C}, which is sized to

minimize the overall (conduction + dynamic) losses. Signal CLK_C activates the ZCS circuit. The equivalent circuit for this phase is shown in Figure 20.

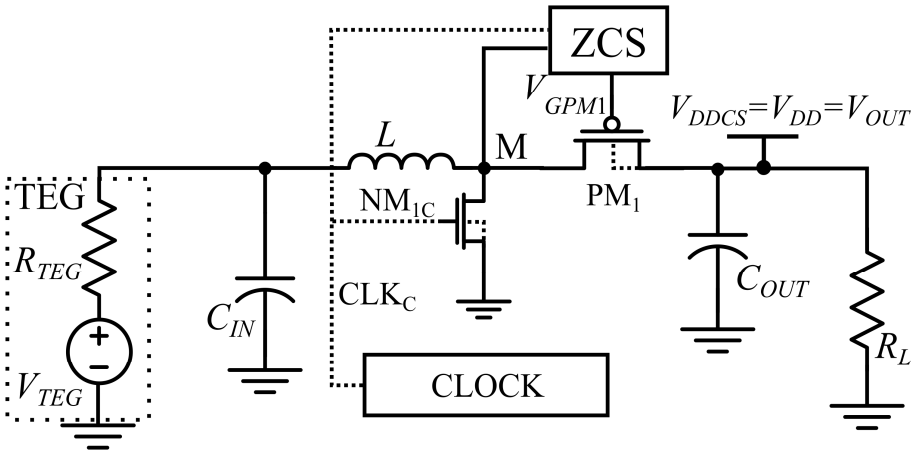


Figure 20 - Converter equivalent circuit during Phase C.

3.2 STEADY-STATE OPERATION

Steady-state operation herein is associated with phase C, in which the output voltage can be in the range of around 0.66 V to around 1 V. When the boost converter operates in DCM under high conversion gain, the output voltage can be determined using expression (2.22), which yields

$$V_{OUT} = \frac{D^2 V_{IN}^{\ 2}}{2Lf_{SW}I_{OUT}}. \tag{3.1}$$

In our design, f_{SW}, L and D are fixed parameters; therefore, during circuit operation the output voltage is dependent only on V_{IN} and I_{OUT}. In order to avoid an increase in the output voltage under the condition of low output current and/or high input voltage, the control circuit temporarily disables the clock, interrupting the boost operation for a certain amount of time, to limit the output voltage to a value around 1 V.

Thus, in steady-state operation, the converter can operate in two distinct ways:

Non-limited V_{OUT} – When V_{IN} and I_{OUT} lead to a value of V_{OUT} between 0.6 and 1.0 V, the boost operation is continuously maintained. The output ripple for non-limited V_{OUT} is a function of C_{OUT} and the detailed analysis for determining its value is described in Appendix B. The MPPT condition is given by (2.41), which sets the value of the Lf_{SW}.

Limited V_{OUT} – If V_{IN} and/or I_{OUT} lead to a value of V_{OUT} which tends to be above 1 V, the limiting of V_{OUT} to 1 V takes place. The converter alternates between active (clock is on)

and inactive (clock is off) states. During the inactive state, the output capacitor provides the load current. Simulations of V_{OUT} limiting as well as of the clock voltage are shown in Figure 21. For limited V_{OUT}, the output ripple, which can be observed in Figure 22, is dependent on the hysteresis width set by the comparator that enables or disables the clock. In the active state, the MPPT is achieved for the value of the Lf_{SW} in (2.41). During the inactive state, after the completion of the current cycle of boost operation, the harvesting ceases; therefore, the extraction efficiency is around zero. Hence, for the case of converter operation under limited V_{OUT}, the total extraction efficiency is given by the proportion of time the converter is in the active state, yielding

$$\eta_{EXTR,LIM} \approx \eta_{EXTR} \frac{t_{ACTIVE}}{t_{ACTIVE} + t_{INACTIVE}}. \tag{3.2}$$

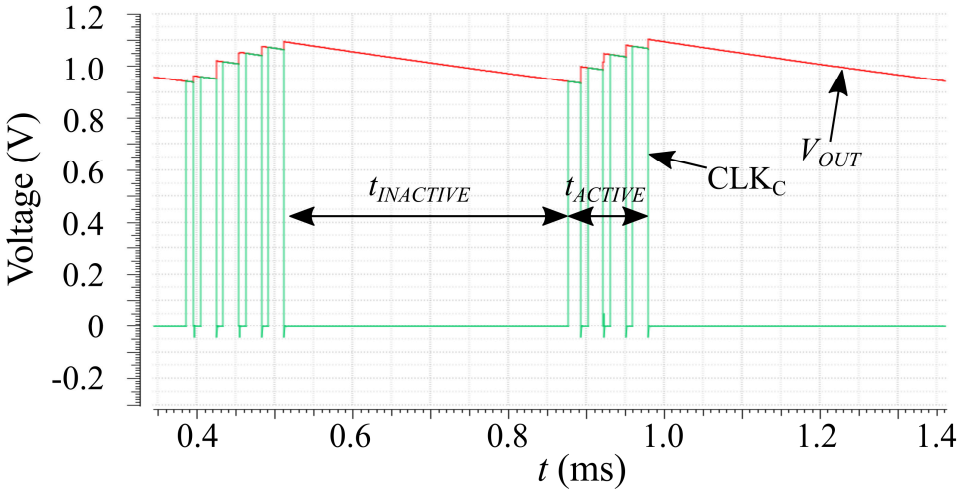


Figure 21 - Simulation of V_{OUT} limiting.

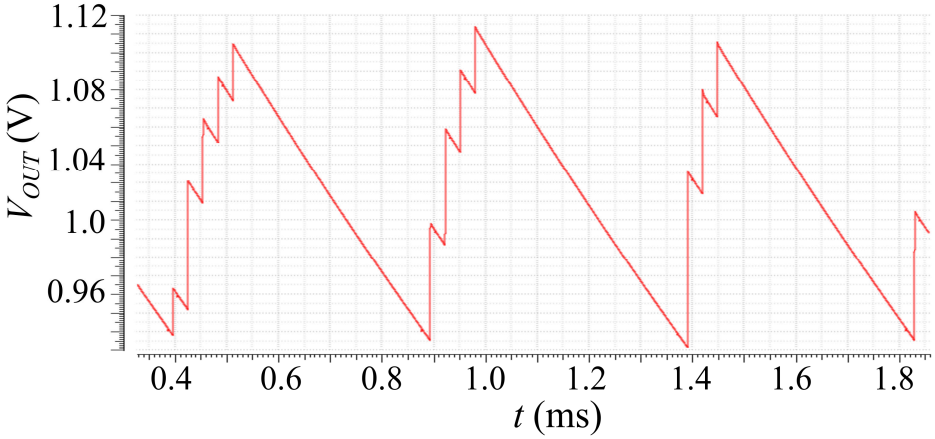


Figure 22 - Output ripple for V_{OUT} limited to approximately 1 V.

3.3 CONTROL CIRCUIT

The control block (Figure 23) is comprised of three comparators, logic inverters, a negative voltage doubler, the V_{DD} sensing circuit and the voltage reference circuit. It is used for the commutation between the different phases of operation during the buildup sequence and to limit of V_{OUT} during steady-state operation. The main input to the control block is V_{DD}, which is sensed and compared with a reference voltage. The control signals are used for opening and closing the switches of the converter, enabling different circuit configurations for each of the phases. Figure 24 shows the simulation results of the control signals generated in the control block during V_{DD} buildup.

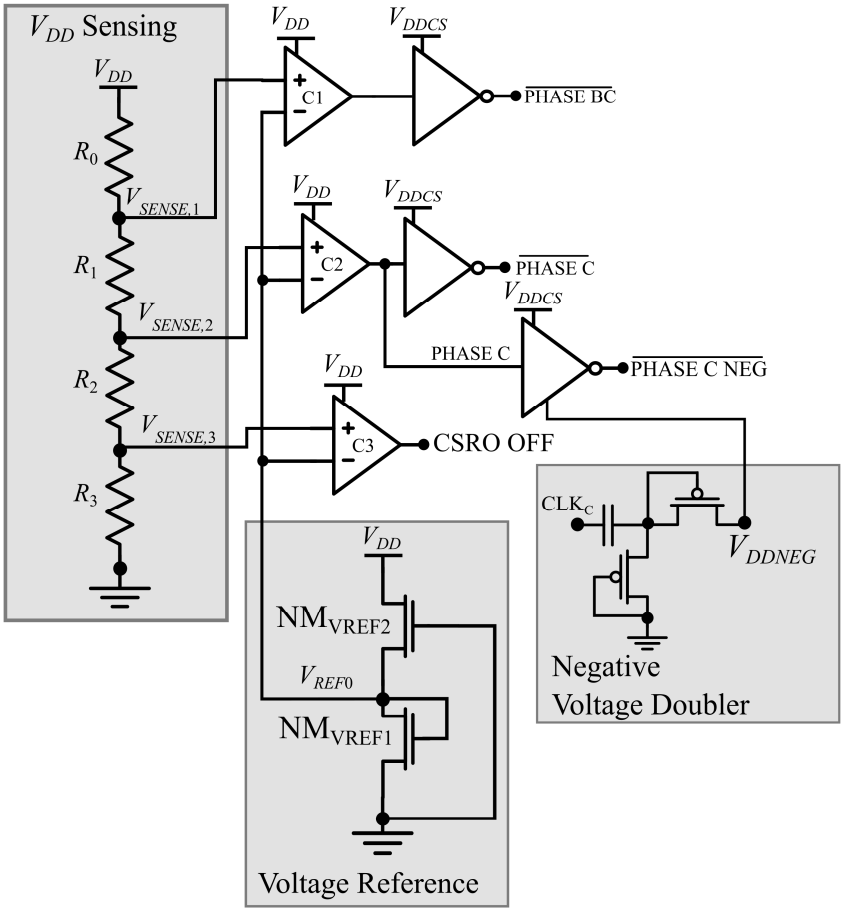


Figure 23 - Control circuit schematic.

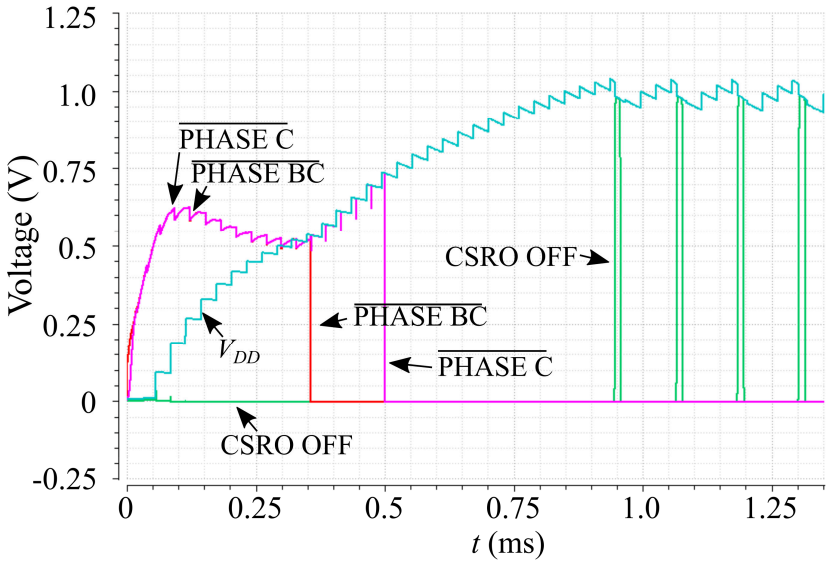


Figure 24 - Simulation results of the control signals.

3.3.1 Voltage Reference

The voltage reference generator (Figure 23), using two transistors, sets the voltage reference used by the control circuit. The principle of operation of this circuit is detailed in [53]. For the proper functioning of the circuit, devices with different threshold voltages should be employed. Transistor NM_{VREF1} is a standard-VT thick oxide device and NM_{VREF2} is a zero-VT (ZVT) thick oxide device. Using the transistor model described in [54], and assuming that both transistors operate in weak inversion and have equal drain current (I_D), we have

$$V_{REF0} = \frac{1}{1+n_1}\left(n_1 \phi_t \ln\left(\frac{\mu_{n2} n_2 \frac{W_2}{L_2}}{\mu_{n1} n_1 \frac{W_1}{L_1}} \right) + \left(V_{TO1} - \frac{n_1}{n_2} V_{TO2} \right) \right). \tag{3.3}$$

where n is the slope factor, $W_{1(2)}$ and $L_{1(2)}$ are the MOSFET channel width and length of $NM_{VREF1(2)}$, respectively, $V_{TO1(2)}$ is the equilibrium threshold voltage of $NM_{VREF1(2)}$, $\mu_{n1(2)}$ is the electron mobility of $NM_{VREF1(2)}$ and ϕ_t is the thermal voltage.

The first term of the V_{REF0} expression is proportional to the absolute temperature whereas the second term is complementary to the absolute temperature. Therefore, the sizing of the transistors can be chosen in order minimize the dependence of V_{REF0} on the temperature, given that longer devices provide less power consumption and have better stability in terms of variations in V_{DD}, due to the minimization of short-channel effects. Figure 25 (a) shows the dependence of V_{REF0} on the temperature for several NM_{VREF1} width values. The width of 28 µm

was selected, since this value provided the best performance regarding temperature stability. In Figure 25 (b), the simulation results for the dependence of V_{REF0} on temperature for the final transistor dimensions are shown. As can be seen, the variation in V_{REF0} is around 0.048% for a temperature range of -10 to 80 ^{o}C.

The circuit was also simulated to verify the stability regarding V_{DD} and process variation, and the results are shown in Figure 26. For V_{DD} >0.4 V, V_{REF0} varies 0.2% for V_{DD} varying from 0.4 to 1.2 V. For the extreme corners, a variation of 3.2% in V_{REF0} was observed.

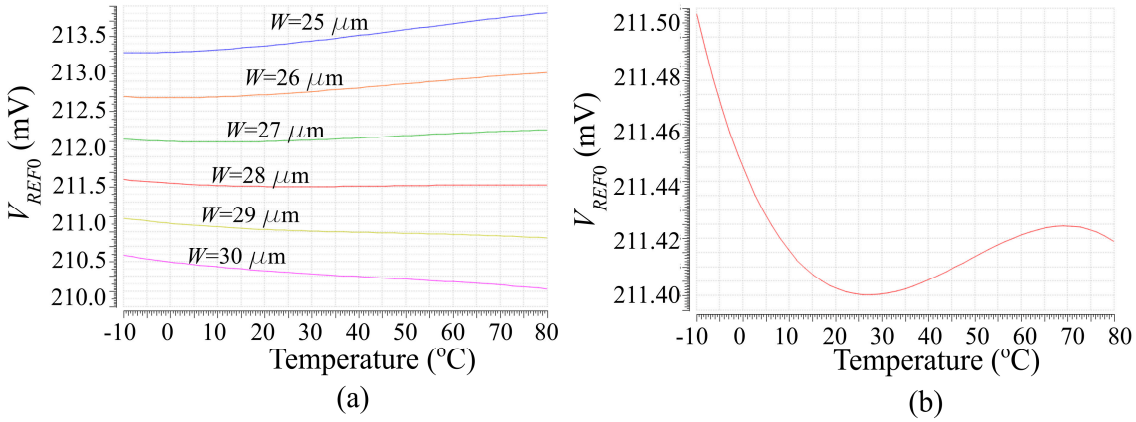


Figure 25 - V_{REF0} vs temperature for (a) different NM_{VREF1} widths and (b) final dimensions.

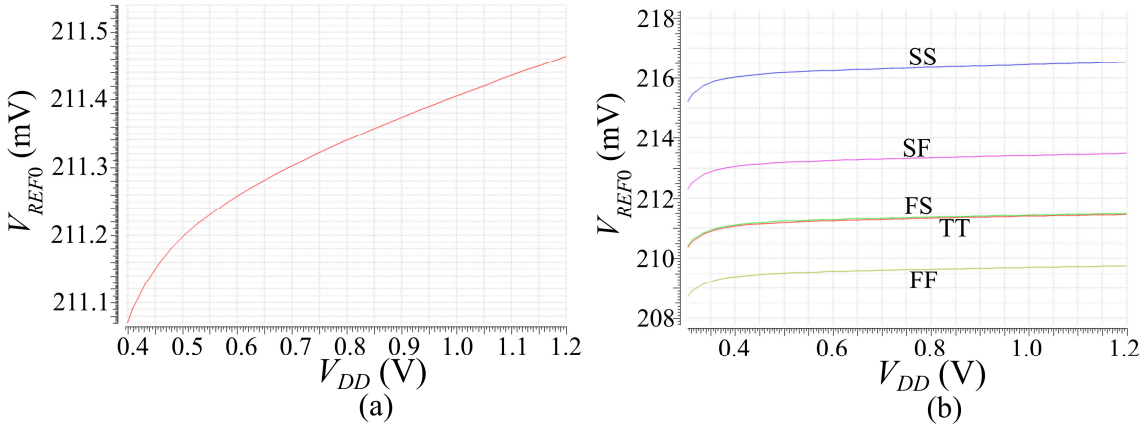


Figure 26 - (a) V_{REF0} vs V_{DD} for TT corner and (b) for different corners.

The simulated results for V_{REF0} show that the circuit stability regarding the main variables is suitable for the requirements of this particular application, since the tolerance of V_{DD} levels for transitioning between phases is higher than the variations observed in simulations. The transistor sizes are shown in Table 3.

Table 3 - Sizing of the reference generator transistors.

Transistor	*W/L*	Type
NM_{VREF1}	28 μm/30 μm	Thick-oxide NMOS
NM_{VREF2}	33 μm/30 μm	Thick-oxide ZVT NMOS

3.3.2 Sensing circuit

The V_{DD} level is sensed by the resistive voltage divider in accordance with

$$V_{SENSE,n} = k_n V_{DD} . \tag{3.4}$$

When comparing V_{REF0} with the sensed voltages ($V_{SENSE,n}$), a change in the comparator state occurs for

$$V_{SENSE,n} = V_{REF0} \pm V_{HYS} . \tag{3.5}$$

V_{HYS} is the effect of the hysteresis, intentionally introduced in the comparator to avoid improper triggering. Thus, using expressions (3.4) and (3.5), transitions occur for

$$V_{DD} = \frac{V_{REF0} \pm V_{HYS}}{k_n} . \tag{3.6}$$

Table 4 shows the values for the resistors of the voltage divider, the ratio k_n and the V_{DD} values for the transition between phases. The simulation results for the voltages generated by the sensing circuit during the V_{DD} buildup are shown in Figure 27.

Table 4- Parameters related to the sensing circuit.

n	R_n (MΩ)	k_n	V_{DD} transition (V)
0	7	-	-
1	1	0.4	0.53 ±0.038
2	1.25	0.32	0.66 ±0.046
3	2.5	0.21	1.0 ±0.07

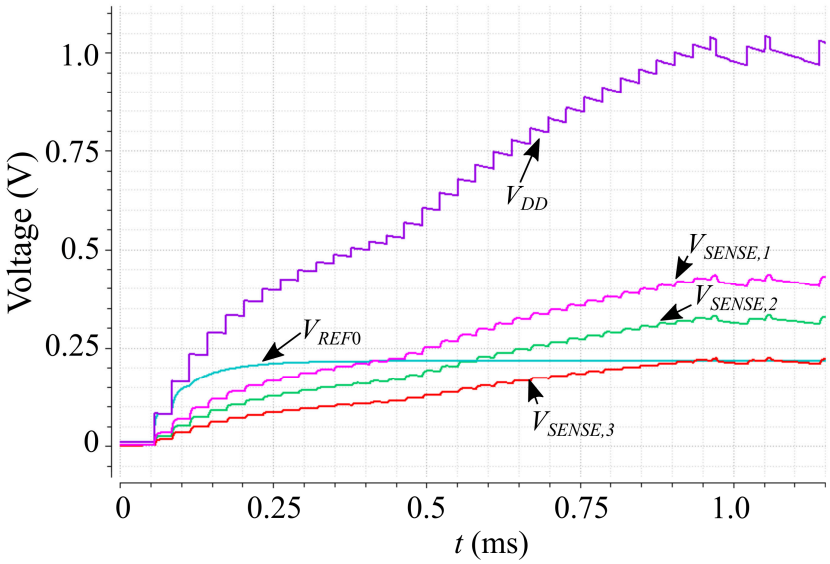


Figure 27 - Sensed voltages and V_{REF} during V_{DD} buildup.

3.3.3 Hysteretic comparators

The comparators (Figure 28) are used to control the state of switches PM_2 and PM_3 and activating/deactivating CLK_{AB} and CLK_C. Comparator C1 is responsible for the transition between phase A and phase B, controlling the state of PM_2 and PM_3. Comparator C2 controls the transition from phase B to phase C, activating CLK_C, deactivating CLK_{AB} and setting a control signal used by a negative voltage doubler to turn off the cold starter. C3 is responsible for activating/deactivating CLK_C when V_{OUT} is being limited.

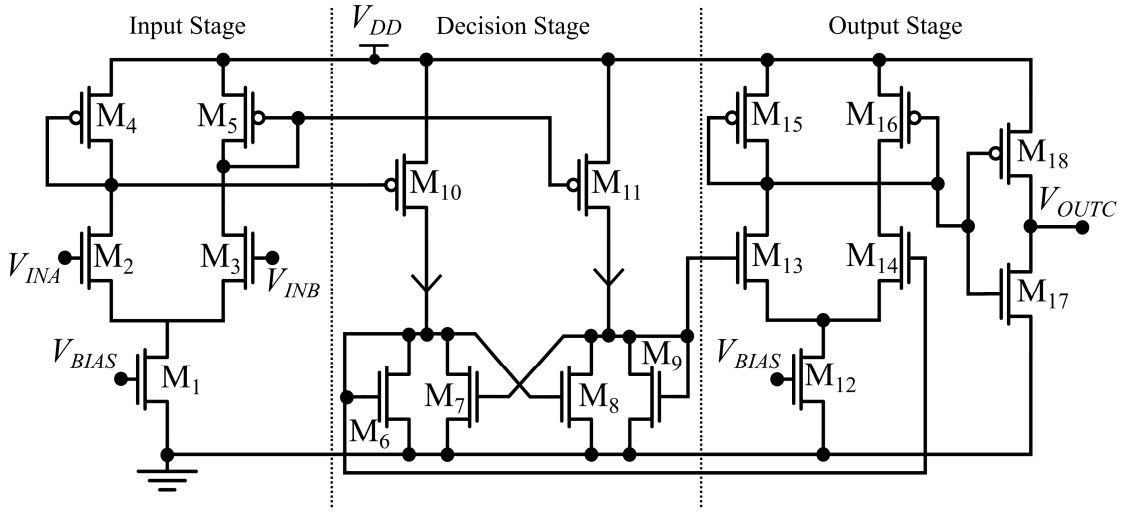


Figure 28 - Comparator schematic.

In order to avoid undesirable transitions at the output, the comparators were implemented with hysteresis [55]. The comparators are composed of three stages; the preamplifier stage, the decision stage and the output stage (Figure 28). In the decision stage, the difference in the transistor sizes directly affects the switching point ($M_6 = M_9 \neq M_7 = M_8$) and sets the hysteresis magnitude. The transistor sizes obtained from the parametrical simulation are shown in Table 5.

Figure 29 shows the DC transfer curve for the comparator. Since $V_{REF0} \approx 211$ mV, a hysteresis of approximately ±15 mV around V_{REF0} reflects in a hysteresis level of ±38 mV around V_{DD} for C1, ±46 mV for C2 and ±70 mV for C3, as shown in Table 4.

Table 5 - Comparator devices.

Device	*W*/*L* (µm)	Device	*W*/*L* (µm)	Device	*W*/*L* (µm)
M_1	6.75/1	M_7	5/1	M_{13}	1/1
M_2	1.25/1	M_8	5/1	M_{14}	1/1
M_3	1.25/1	M_9	1/1	M_{15}	2/1
M_4	5/1	M_{10}	2.5/1	M_{16}	2/1
M_5	5/1	M_{11}	2.5/1	M_{17}	0.48/0.12
M_6	1/1	M_{12}	½	M_{18}	1.8/0.12

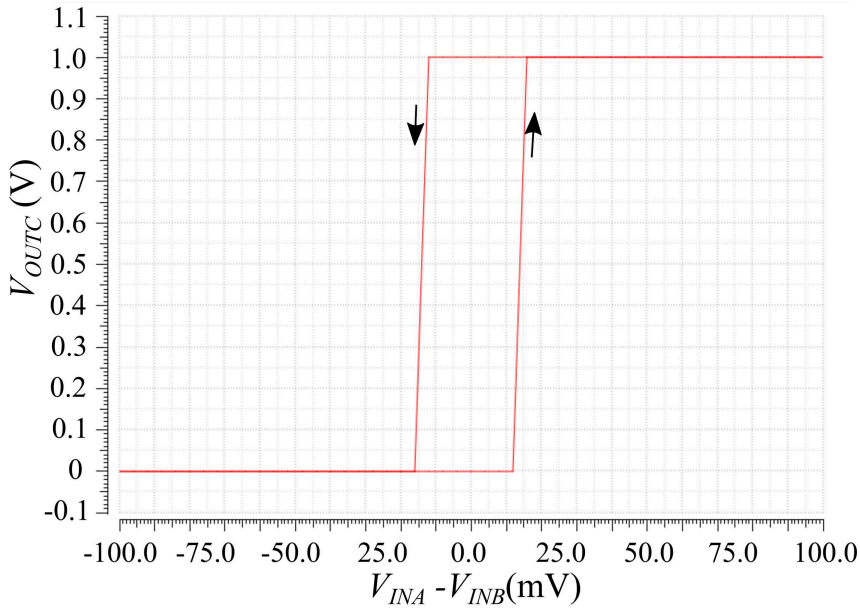


Figure 29 - DC transfer curve for the comparator showing the hysteretic behavior.

The transition time of the comparator can be relatively high, due to the slowness of the signals being controlled (V_{DD} signal ramps up slowly, in the ms range). A transient analysis of the comparator is presented in Figure 30, where the DC level of both V_{INA} and V_{INB} is equal to $V_{DD}/2$ and a sinusoidal signal is applied to V_{INA}. The comparator consumption is also measured by transient simulation, as shown in Figure 31. The static consumption of each comparator is around 55 nW for a settling time of around 1 µs under a load capacitance of 100 fF, which is adequate for this design.

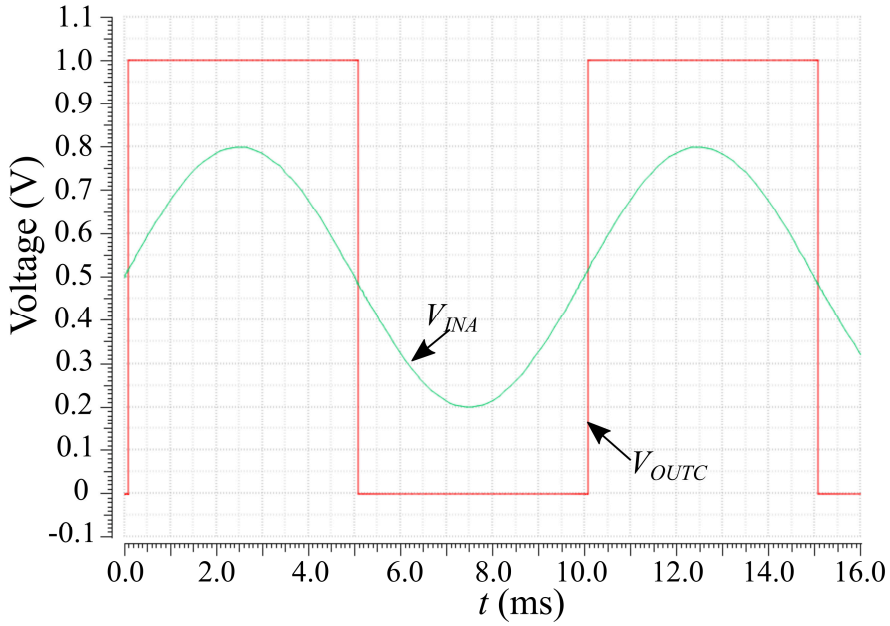


Figure 30 - Transient response of the comparator (V_{INB}=0.5 V).

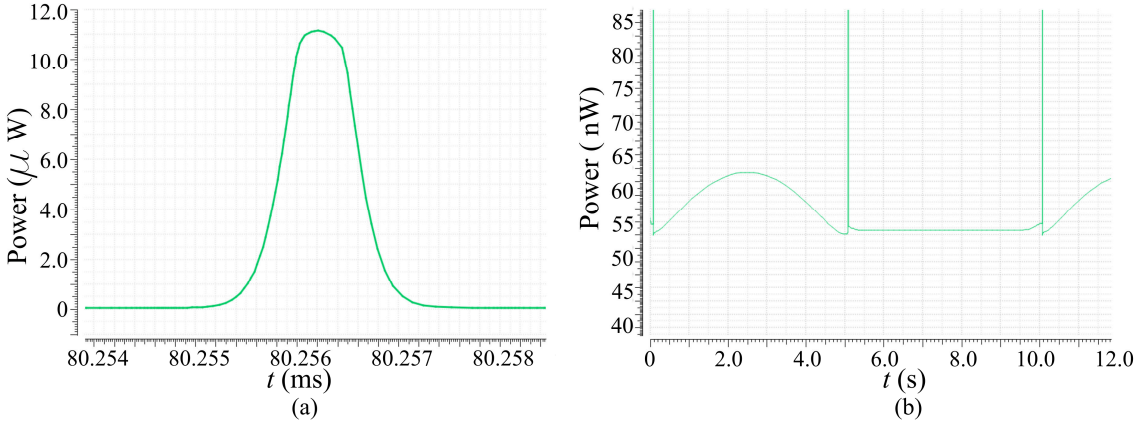


Figure 31 - (a) Power consumption during a change in comparator state and (b) static consumption of the comparator.

3.3.4 Negative voltage doubler

In steady-state, the consumption of the cold starter is around 115 µW for V_{IN}=80 mV (R_{TEG}=5 Ω); hence, it should be turned off after startup in order to improve the system efficiency. In this work, the cold starter is comprised by an ULV oscillator and a rectifier. Therefore, a ZVT NMOS transistor is used as a switch to interrupt the ULV oscillator connection to ground in steady-state, effectively interrupting the operation of the cold starter. Due to the ZVT transistor characteristics, the effective transistor turn-off only occurs for voltages below zero volts; thus, a negative voltage needs to be generated for this purpose.

Using the CLK_C signal, we implemented a negative voltage doubler (Figure 23) using the conventional topology of a clamp followed by a peak detector in order to generate a negative voltage (V_{NEG}). The output capacitor of the voltage doubler is the input capacitance of the ZVT transistor used as a switch; hence, the ZVT transistor should be sized with regard to three distinct aspects: firstly, the ON series resistance should not significantly affect the minimum V_{IN} for startup; secondly, the switch should effectively turn off the oscillator in steady-state; and thirdly the gate capacitance of the switch should provide an adequate ripple level.

For the oscillator shutdown in phase C, we use an inverter for which V_{DDCS} and V_{NEG} are the supply rails (Figure 23); therefore, in phases A and B, the inverter outputs V_{DDCS}, while in phase C, the inverter outputs V_{NEG}. Figure 32 shows the transient simulation of the control signal that turns off the ULV oscillator of the cold starter when the converter commutes from phase B to phase C.

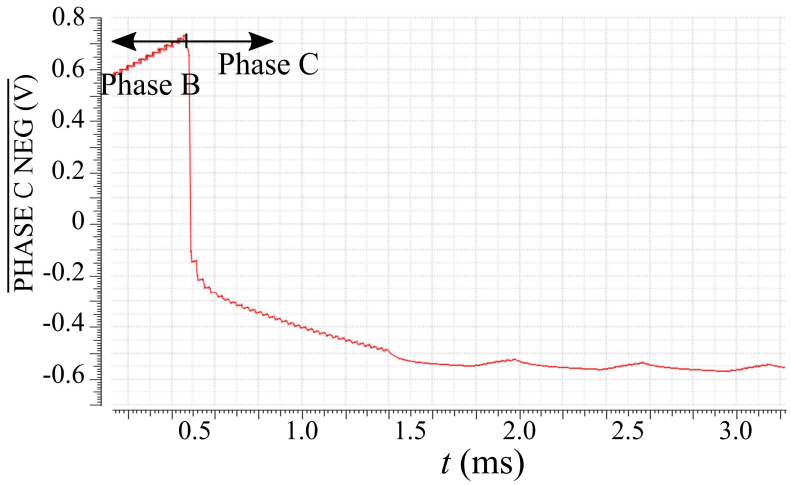


Figure 32 - Transient simulation of control signal used for the shutdown of the cold starter.

3.4 CLOCK CIRCUIT

The clock circuit (Figure 33) provides the signal for switching the LSS. It is also used for both the timing of the ZCS circuit and as the oscillatory signal used in the negative voltage doubler.

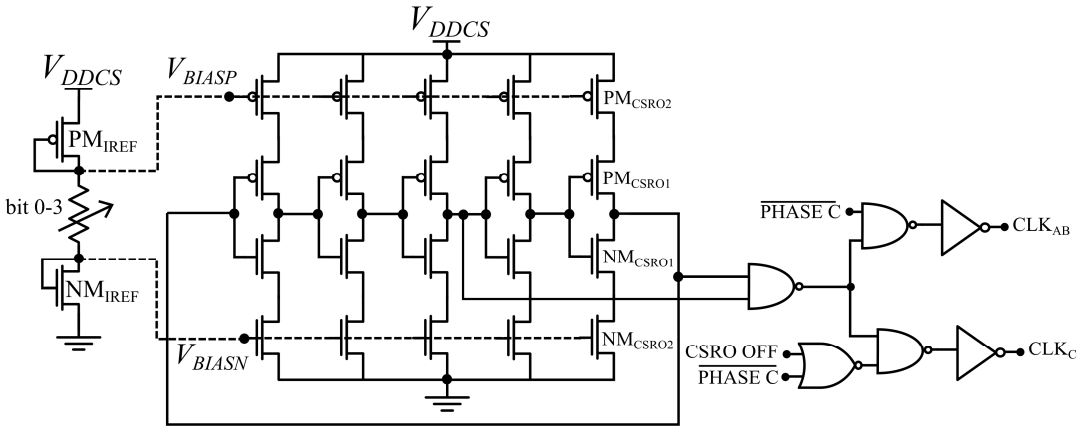


Figure 33 - Clock circuit schematic.

The clock is a 5-stage CSRO and its frequency can be fine tuned by four external trimming bits in order to maintain $V_{IN}=V_{TEG}/2$. The switching frequency is set at around 30-40 kHz, this being a trade-off between dynamic losses, practical inductor values (2.41) and switch sizes (2.61), (2.62). The external trim bits enable the value of the current reference resistor to be adjusted from 16 MΩ to 22 MΩ, and this range allows a variation of around 33% in f_{SW}. The f_{SW} variation can be used to compensate tolerances of off-the-shelf inductors and process variation, and is given by

$$f_{SW} = \frac{1}{2t_P n_{st}}, \tag{3.7}$$

where n_{st} is the number of stages and t_P is the propagation delay of a single inverter stage. Due to the difficulty associated with determining t_P analytically, the transistor sizes were defined by parametrical simulation, in order to achieve the desired f_{SW} in the range of 30-40 kHz, as seen in Table 6. The CSRO frequency was simulated for the different corners, and a variation of -5.3% (FF), -0.8% (FS), -1.5% (SF) and +0.36% (SS) in f_{SW} was observed.

The post-layout simulations of the signals from each of the five CSRO stages are shown in Figure 34.

Table 6 - Sizes of the clock circuit transistors.

Transistor	*W/L*	Type
PM_{CSRO1}	2.5 µm/1 µm	Standard PMOS
PM_{CSRO2}	2 µm/2 µm	Standard PMOS
PM_{IREF}	8 µm/2 µm	Standard PMOS
NM_{CSRO1}	700 nm/1 µm	Standard NMOS
NM_{CSRO2}	1 µm/2 µm	Standard NMOS
NM_{IREF}	4 µm/2 µm	Standard NMOS

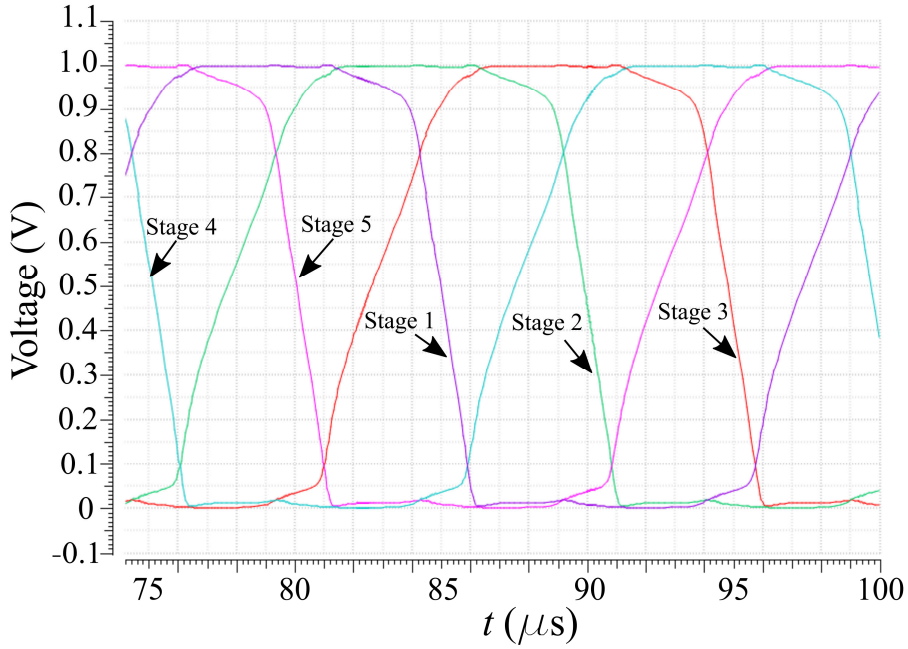


Figure 34 - Simulated outputs of the 5-stage CSRO.

3.4.1Duty cycle and clock logic

In order to select a duty cycle appropriate for a high converter efficiency, we used (2.46) to (2.60) to plot η_{CONV} as a function of R_{TEG} for different values of D for the case of V_{IN}=10 mV and 100 mV, as shown in Figure 35.

For the commercial TEG range indicated in Figure 35, the mean overall efficiency is greater for higher values of D. Hence, at the output of the CSRO, two signals from different stages are used by a NAND gate to generate an asymmetrical waveform with a duty cycle higher than 0.5. On combining the output of the third stage with the output of the fifth stage,

the duty cycle obtained is close to 0.7. This value limits the minimum voltage gain to 3.3 or, equivalently, the maximum input voltage to 300 mV for V_{OUT}=1 V under MPPT. However, since the converter is designed to operate in a range of approximately 10 to 150 mV, this limitation is not of concern. The results of post layout simulations of the outputs of the third and fifth stages as well as the asymmetrical clock signal after the NAND gate can be observed in Figure 36.

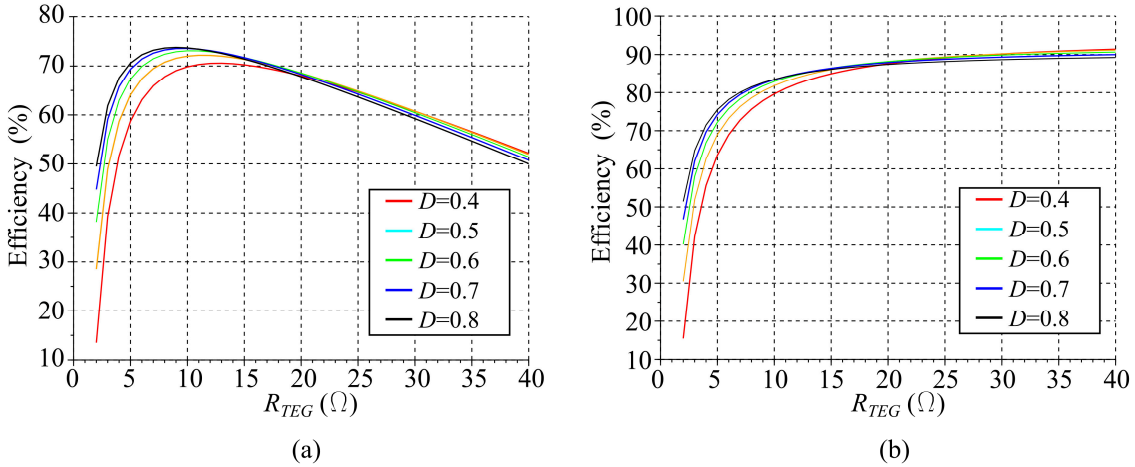


Figure 35 - Efficiency vs R_{TEG} for different values of D when (a) V_{IN}=10 mV and (b) V_{IN}=100 mV, f_{SW}=40 kHz, inductor Q=40, R_{LSS}=2050 Ω, R_{HSS}=8508 Ω, C_{PAR}=5 pF, P_{PER}=800 nW.

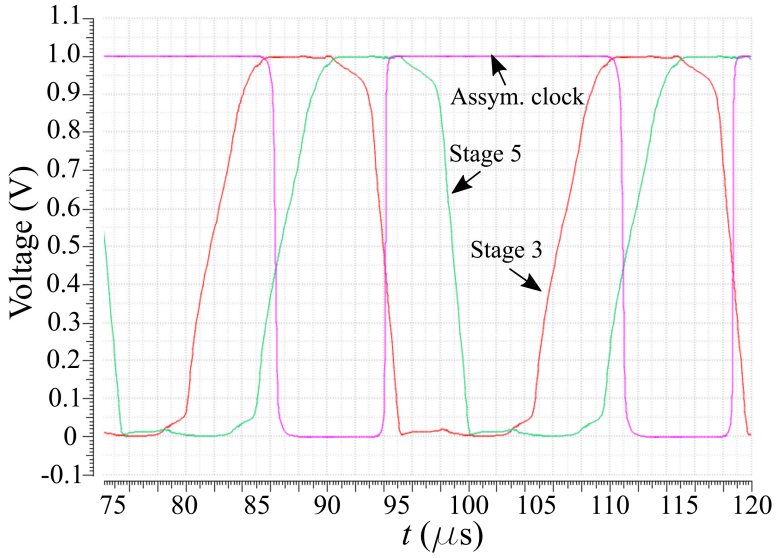


Figure 36 - Simulation of the output signals from the third and fifth stages and the asymmetrical clock.

After the generation of the asymmetrical clock, logic gates are used to enable and disable the signals CLK_{AB} and CLK_C during the different phases of operation. During phases A

and B, CLK_{AB} is enabled and CLK_C is disabled. In phase C, CLK_{AB} is always disabled and CLK_C is enabled if the converter is active and disabled if it is inactive (V_{OUT} limited). Figure 37 shows the simulation of CLK_{AB} and CLK_C during V_{DD} buildup and in steady-state for a case in which V_{OUT} is limited after reaching Phase C.

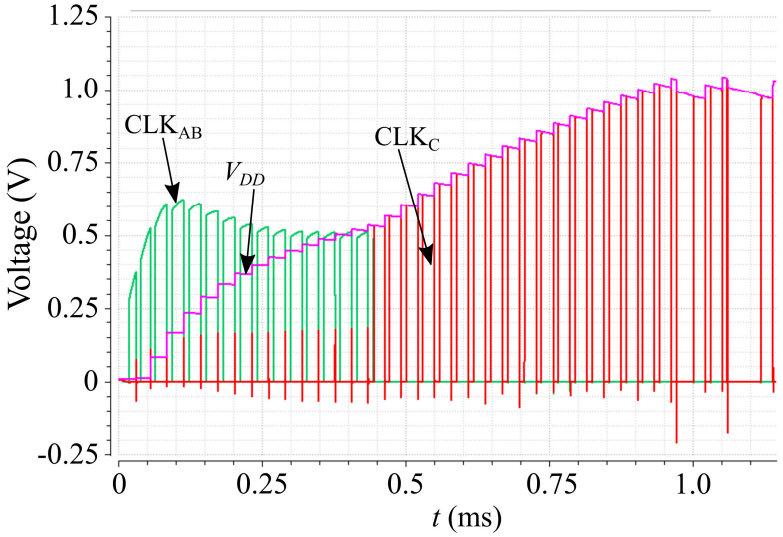


Figure 37 - Simulation of CLK_{AB} and CLK_C during V_{DD} buildup.

4 ULTRA-LOW-VOLTAGE STARTUP

In order to perform the startup of the converter at low voltages, an auxiliary cold starter converter is implemented.

Oscillator topologies [27], [33], [34], [37], [38], [39], [40], [41] that can provide oscillations beyond the TEG voltage are an important solution to start up from low input voltages. The oscillatory signals generated by the oscillator are applied to a rectifier to provide a temporary DC voltage much higher than V_{TEG} at startup. Figure 38 shows a simplified equivalent circuit of the oscillator loaded by the rectifier. In order to properly design an efficient cold starter circuit, the co-design of the oscillator and the rectifier is fundamental since the amplitude of the oscillatory signals generated by oscillators is dependent on the load imposed by the rectifier (input impedance of the rectifier) while the input impedance and output voltage of the rectifier, are in turn, dependent on the amplitude of the oscillation, as well as on the load current which is imposed by the boost converter during startup.

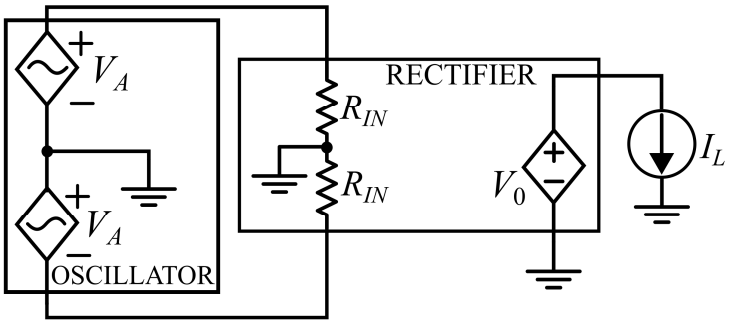


Figure 38 - Simplified equivalent circuit of the oscillator loaded by the rectifier.

The target of this design was to obtain a DC voltage of around 500 mV at the rectifier output, which is a voltage level high enough to drive the clock circuit and accomplish the full V_{DD} buildup. During startup, the cold starter powers the clock circuit, a few logic gates and LSS, the latter representing the greatest load to the cold starter, in which the dynamic losses should be minimized to achieve a low startup voltage. After the cold starter load minimization, the current drawn from node V_{DDCS} is of the order of 100 nA for $V_{DDCS} \approx 500$ mV.

4.1 THE ULTRA-LOW-VOLTAGE OSCILLATOR

Ultra-low-voltage LC oscillators are generally used in the cold starter to generate AC voltage levels much higher than the voltage delivered by the TEG, providing voltage boosting. In [56], [57], the enhanced-swing Collpits oscillator, the ILRO and the enhanced-swing ring oscillator (ESRO) were analyzed and modeled. Although no analytical expression for the oscillation amplitude of the oscillators is available, simulation and experimental results [56], [57] indicate promising applications in ULV converters. The ESRO (Figure 39 (a)) delivered the best performance at low V_{DD}, although the ILRO has the advantage of using fewer inductors.

A simplified small-signal equivalent circuit of a single stage of the ESRO is shown in Figure 39 (b), where C_T is the total capacitance of the gate terminal, g_m is the gate transconductance [54], g_{md} is the drain transconductance, G_1 and G_2 are the parallel conductances of the L_1 and L_2 inductors, respectively, and G_0 is the output conductance, which in this case, is the input conductance of the rectifier (G_O=1/R_{IN}).

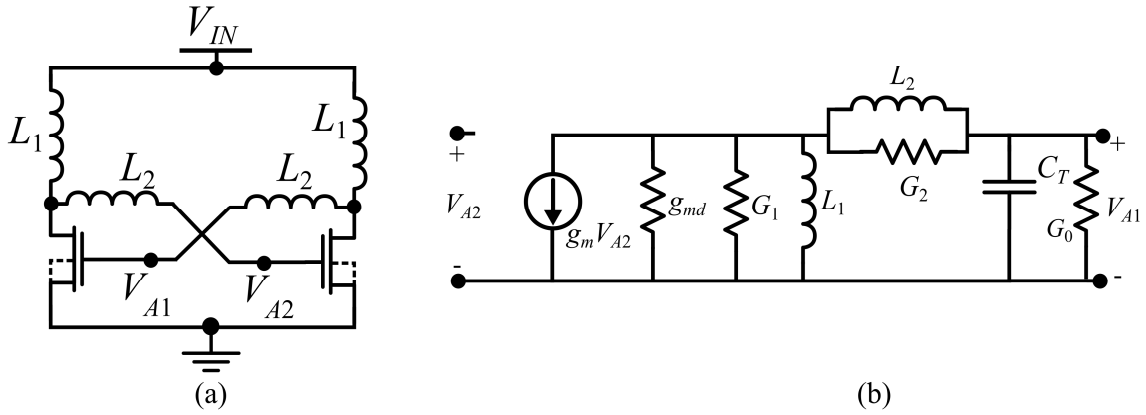


Figure 39 - (a) A two-stage ESRO schematic and (b) its simplified small-signal equivalent circuit.

Using the equivalent signal in Figure 39 (b) and the derivation presented in [56],[57], assuming equal Q values for the inductors and disregarding the effect of losses on the frequency of oscillation, the oscillation condition for the ESRO is

$$\frac{g_{ms}}{g_{md}} > 1 + n\left[\frac{1}{1+L_2/L_1} + \frac{1}{g_{md}Q}\sqrt{\frac{C}{L_1}}\sqrt{\left(1+L_2/L_1\right)} + \frac{G_O}{g_{md}}\left(1+L_2/L_1\right)\right] \tag{4.1}$$

$$= 1 + n\left[\frac{1}{1+L_2/L_1} + \frac{1}{g_{md}Q}\sqrt{\frac{C}{L_2}}\sqrt{L_2/L_1\left(1+L_2/L_1\right)} + \frac{G_O}{g_{md}}\left(1+L_2/L_1\right)\right] \tag{4.2}$$

where g_{ms} is the source transconductance. As can be seen, the effect of the losses on the inductors (low Q) and G_O can be compensated through the use of wide transistors (high g_{md}). Using the MOSFET modeling available in [54], the relation between the g_{ms}/g_{md} ratio and the drain-to-source voltage (V_{DS}) is given by

$$\frac{V_{DS}}{\phi_t} = \left(\sqrt{1+i_r} - 1\right)\left(\frac{g_{ms}}{g_{md}} - 1\right) + \ln\left(\frac{g_{ms}}{g_{md}}\right), \tag{4.3}$$

where i_r is the MOSFET reverse inversion level. Thus, regardless of the inversion level, V_{DS} increases monotonically with g_{ms}/g_{md}. Since the source potential of the ZVT transistors is connected to ground and the drain DC level is V_{IN}, V_{DS} expressed in (4.3) is equal to V_{IN}. Hence, through (4.1) and (4.3) one can find the minimum input voltage for achieving oscillations.

With the aid of (4.2), in Figure 40 we plot the g_{ms}/g_{md} ratio obtained with the ESRO for different L_2/L_1 ratios for the unloaded oscillator. For comparison purposes, the g_{ms}/g_{md} ratio of the ILRO is also plotted. The value of the ILRO inductor (L) as well as L_1 or L_2 will generally be the on-chip inductor with the highest available inductance value, maximizing (4.2). Hence, when $L_2/L_1 \geq 1$, $L=L_2$, and when $L_2/L_1 \leq 1$, $L=L_1$.

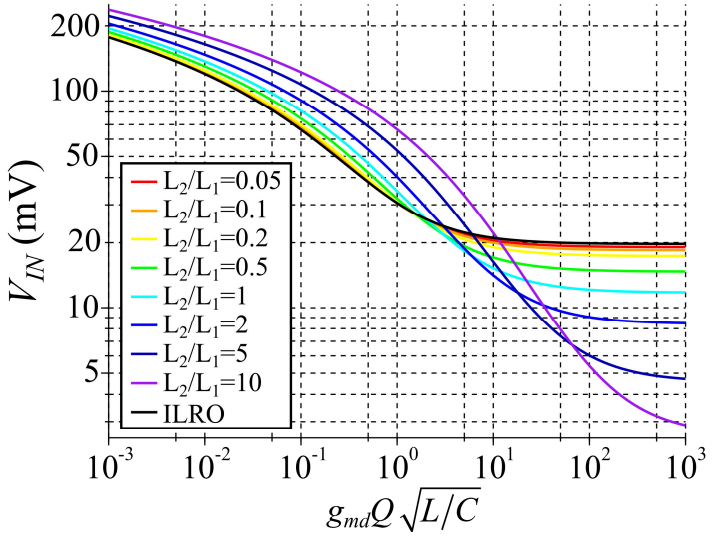


Figure 40 - Condition for achieving oscillations using the ESRO and the ILRO (n=1).

As can be noted, when losses are low, a high L_2/L_1 ratio minimizes the oscillation condition. As the losses increase, the ILRO starts showing better performance. This is especially relevant for the integrated cold starter, since the Q of on-chip inductors is generally poor. Since the startup at low input voltages is intended, the ESRO was chosen as the ULV oscillator of the cold starter. Therefore, the choice of appropriate inductors with high Q at the oscillation frequency should be made in order to take advantage of the ESRO characteristic.

4.2 RECTIFIERS

A model of the rectifier is required in order to determine its DC output voltage as well as the input resistance which loads the oscillator outputs.

In [58],[59],[60], the n-stage half-wave voltage multiplier was analyzed and expressions for the input resistance, output voltage and efficiency were derived considering the Shockley equation for the diodes, enabling the optimization of the rectifier as a function of the number of stages (N) and the ratio of the load current to the saturation current (I_L/I_S). Here, we modify the derived expressions to comply with the connections using complementary signals.

Also, using the Shockley equation, the Dickson charge pump (DCP) [61] was analyzed in [56]. We modify the input resistance equation in order to express the input resistance seen from each of the oscillator output nodes, as represented in Figure 38. Although the load can be slightly asymmetric when using this type of rectifier, we approximate the input impedance to be equally distributed between the two oscillator outputs.

Another common rectifier topology used in low-voltage applications is the cross-coupled rectifier [48]. By cross-coupling the gates of the transistors, this type of rectifier dynamically compensates the threshold voltage of the transistors in order to reduce the forward voltage drop and decrease the leakage current. In [62], we proposed a modification on the transistor arrangement, where a static compensation of the threshold voltage is added by connecting the gates of the transistors to a different rectifier stage, enabling the use of smaller transistors, which allows a reduction in the overall losses by decreasing the dynamic losses. In Appendix E, the expressions for the input resistance and output voltage of the cross-coupled rectifier are derived.

Table 7 summarizes the expressions for the input impedance and output voltage of the rectifier topologies that were analyzed, for a sine-wave input of amplitude V_A and load current I_L.

Table 7 - Summary of the output voltage and input resistance of rectifiers.

Rectifier	Output voltage	Input resistance
Voltage multiplier	$2Nn\phi_t \ln\left[\frac{I_0(V_A/n\phi_t)}{1+I_L/2I_S}\right]$	$\frac{V_A}{2N(2I_S+I_L)}\frac{I_0(V_A/n\phi_t)}{I_1(V_A/n\phi_t)}$
DCP	$2.n\phi_t \ln\left[\frac{I_0(V_A/n\phi_t)}{1+I_L/I_S}\right] + (N-2)n\phi_t \ln\left[\frac{I_0(2V_A/n\phi_t)}{1+I_L/I_S}\right]$	$\frac{V_A}{2(I_S+I_L)\left[\frac{I_1(V_A/n\phi_t)}{I_0(V_A/n\phi_t)}+(N-2)\frac{I_1(2V_A/n\phi_t)}{I_0(2V_A/n\phi_t)}\right]}$
Cross-coupled rectifier	$2N\phi_t \ln\frac{I_0(2V_A/n\phi_t)-i_L/2I_{SEQ}}{I_0((2-n)V_A/n\phi_t)}$	$\frac{V_A}{2N\left\{\left(i_L-2I_{SEQ}I_0\left(\frac{2V_A}{n\phi_t}\right)\right)\frac{I_1\left(\frac{(2-n)V_A}{n\phi_t}\right)}{I_0\left(\frac{(2-n)V_A}{n\phi_t}\right)}+2I_{SEQ}I_1\left(\frac{2V_A}{n\phi_t}\right)\right\}}$

In the expressions shown, I_{SEQ} is defined in Appendix F and $I_0(z)$ and $I_1(z)$ are the modified Bessel functions of the first kind of order zero and one, respectively.

Figure 41 and Figure 42 show plots of the output voltage and input resistance for different rectifiers, targeting V_{DDCS} around 500 mV and I_L=100 nA for $V_A = n\phi_t$ and $V_A = 3n\phi_t$ respectively. The main objective is to define a design point that delivers the specified output voltage at the highest input resistance possible, minimizing the loading of the ULV oscillator and at the same time, maximizing the conversion efficiency of the rectifier. Since for these simulations V_A is kept constant, the variation in V_A with R_{IN} is neglected.

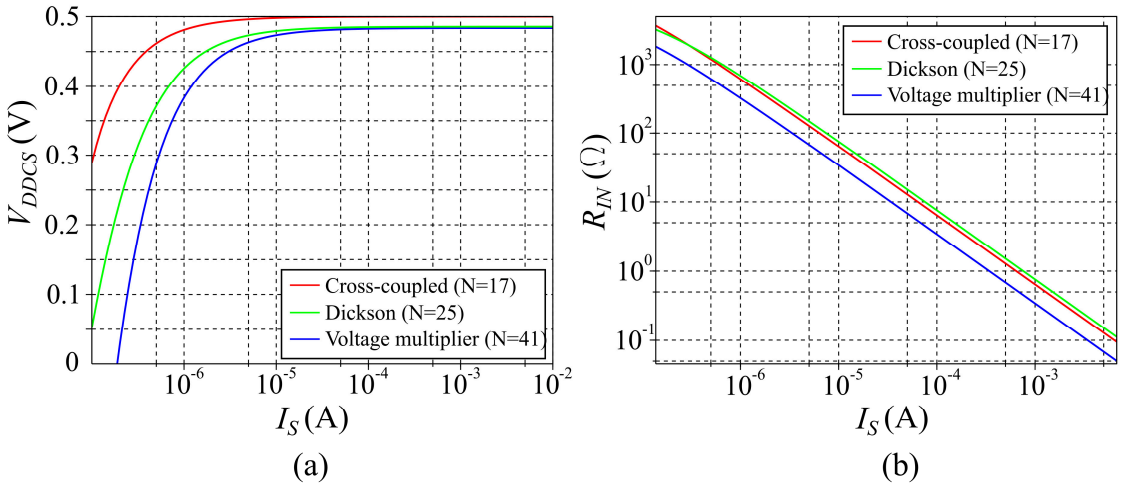


Figure 41 - (a) V_{DDCS} x I_S and (b) R_{IN} x I_S for V_A=$n\phi_t$, n=1, I_S=I_{SEQ}.

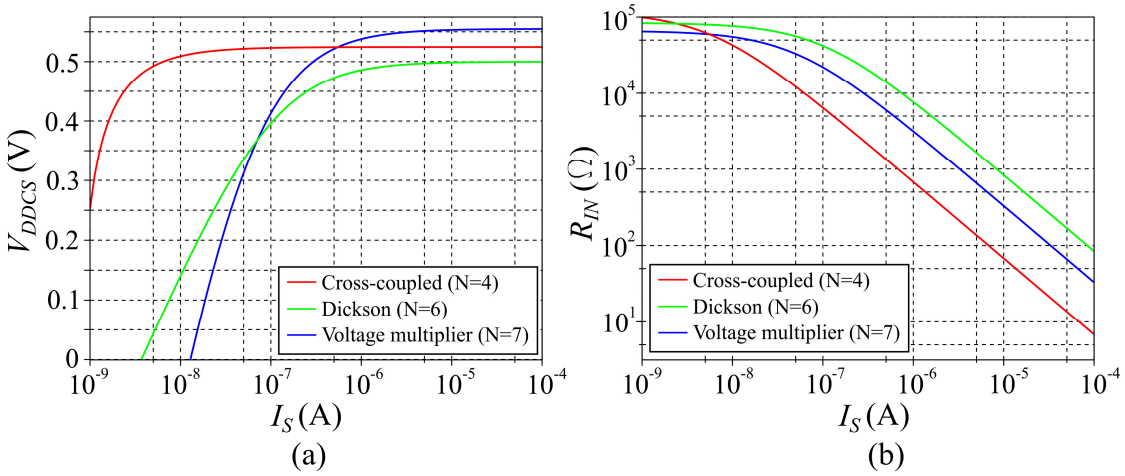


Figure 42 - (a) V_{DDCS} x I_S and (b) R_{IN} x I_S for V_A=3$n\phi_t$, n=1, I_S=I_{SEQ}.

4.3 OSCILLATOR AND RECTIFIER CO-DESIGN

The target of the oscillator and rectifier co-design is to minimize the input voltage required to start up the boost converter and reach steady-state operation. The first step is to minimize the minimum V_{IN} to achieve oscillations for the unloaded oscillator, but taking into account the inductor losses, which can be estimated, for instance, by the post-layout parasitic extraction of on-chip inductors or quality factor graphs. In this step, the goal is to identify a combination of inductors and transistor width which provides oscillation at the minimum V_{IN}. Once the oscillator is defined, the optimization of the rectifier is performed considering the interaction between oscillator and rectifier, due to the mutual dependence of the input resistance and oscillation amplitude. Since an analytical expression for V_A is not available, this part of the design can be performed using an automated procedure similar to that described in [63], where the oscillator is simulated using time domain equations in Matlab, or by parametrical analysis using electronic design automation (EDA) tools.

For the simulation using time domain equations, a resistive load that simulates the rectifier R_{IN} is connected to the output of the oscillator, and a feedback process is set up to achieve the convergence of R_{IN} and V_A. At each iteration, R_{IN} and V_A approach convergence, and the feedback process can be interrupted once R_{IN} is considered to be stable within a tolerance margin, from which is possible to determine the output voltage of the rectifier for a given N-I_S pair. Figure 43 shows a flowchart of the complete procedure for determining the rectifier parameters.

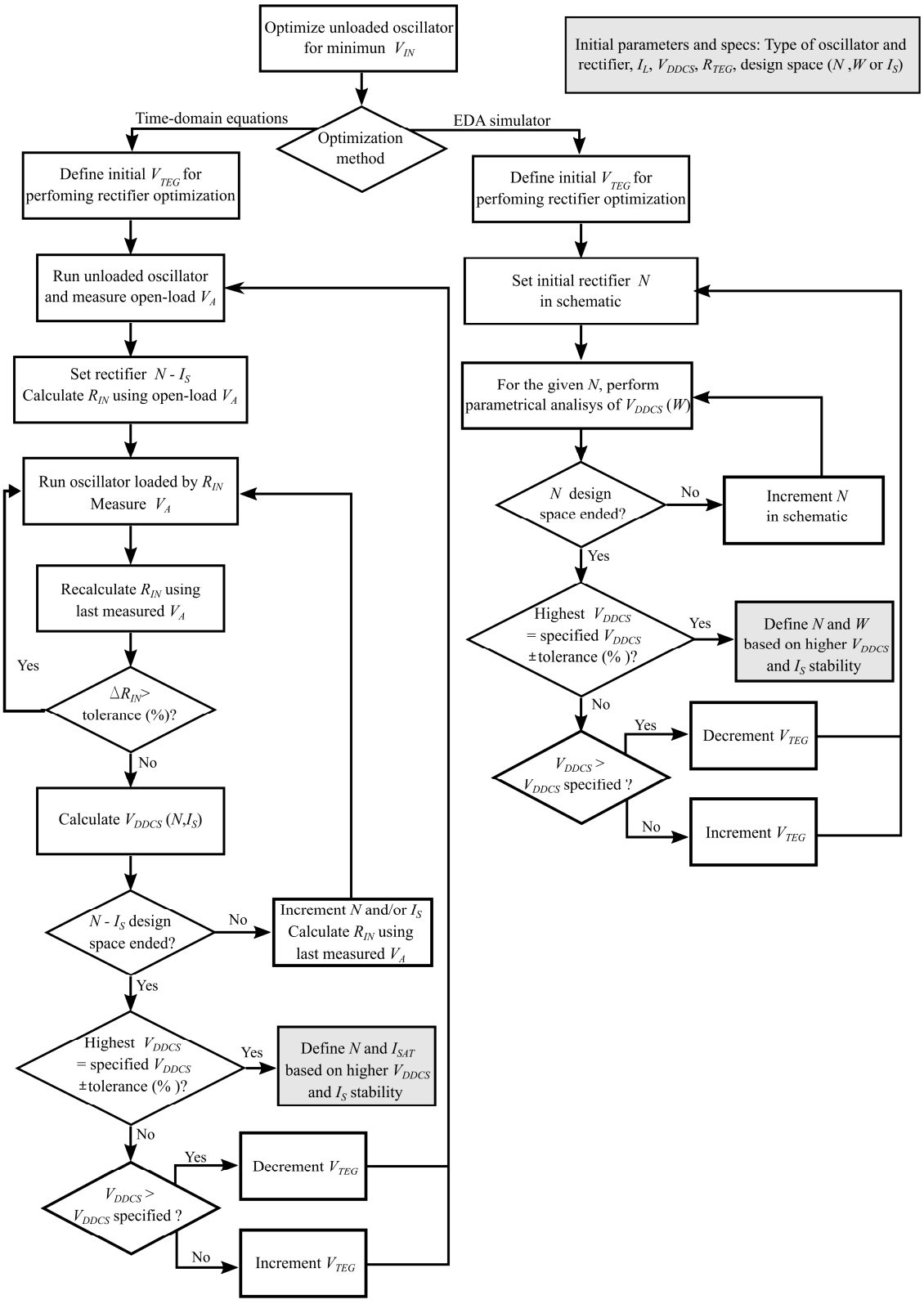


Figure 43 - Rectifier design procedure focusing on the minimization of the converter startup voltage.

The simulation using EDA tools is performed by varying the number of stages in the rectifier (N) and performing parametrical analysis of V_{DDCS} as a function of the width of rectifier transistors (W) for each N, as described in the flowchart of Figure 43, using a resistive load at the output of the rectifier, which corresponds to the boost converter current drawn at the specified V_{DDCS}.

The important target in this design is to minimize the input voltage for delivering the specified output voltage and load current, in order to minimize the startup voltage of the converter. Hence, the optimization procedure is performed around the minimum V_{IN} capable of delivering the specified V_{DDCS} (including a tolerance range), as can be seen by the flowchart. At the end of the procedure, the design points (N-I_S or N-W) that provide higher V_{DDCS} can be chosen in a trade-off between area and output voltage stability (design points less affected by variations in I_S).

4.4 IMPLEMENTED COLD STARTER

Figure 44 shows a schematic of the implemented cold starter, which is comprised of an ESRO and a 3-stage DCP.

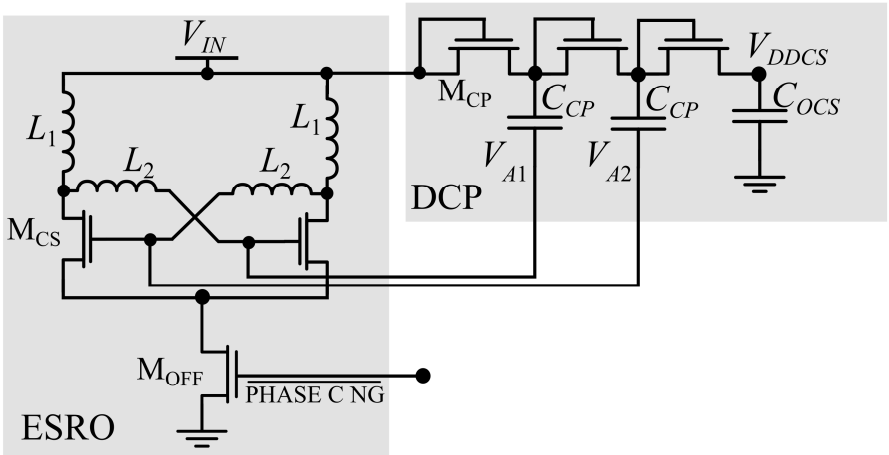


Figure 44 - Schematic of the implemented cold starter.

The ESRO was implemented with both on-chip and off-chip inductors. Table 8 presents the component values and sizes of devices used in the cold starter.

The integration of the circuit shown in Figure 44 was carried out prior to the analysis described in this chapter. The criterion for the rectifier optimization was to minimize the V_{IN} for

the oscillator startup. Thus, the use of a rectifier with a minimum number of stages was implemented since this provides higher input resistance.

In post-layout corner simulations, the startup of the boost converter was achieved for 9.8 mV (TT), 9.2 mV (FS), 12.3 mV (SF), 9.2 mV (FF) and 12.3 mV (SS) for the off-chip ESRO inductors. For the ESRO using integrated inductors, the startup was 70 mV (TT).

Table 8- Devices used in the cold starter.

On-chip inductors		Off-chip inductors	
Device	Value or size	Device	Value or size
L_1	4.29 nH	L_1	see Table 11
L_2	20.74+19.65 nH	L_2	see Table 11
M_{CS}	ZVT - (110x20) μm/420 nm	M_{CS}	ZVT - (90x20) μm/420 nm
M_{OFF}	ZVT - (100x20) μm/420 nm	M_{OFF}	ZVT - (100x20) μm/420 nm
M_{CP}	50 μm/120 nm	M_{CP}	8 μm/120 nm
C_{OCS}	12.8 pF	C_{OCS}	12.8 pF
C_{CP}	2.3 pF	C_{CP}	1.41 pF

4.4.1 Optimization of the implemented cold starter

Although providing oscillations at minimum input voltages is desirable, the main target when designing a cold starter is to minimize the V_{IN} that provides the output voltage and load current necessary for the boost converter to reach steady-state operation. Hence, using the EDA simulator, for the specified V_{DDCS} of around 500 mV and I_L=100 nA (which are the required specifications at the cold starter output to properly drive the boost converter), we simulated the same on-chip ESRO, as described in Table 8, connected to a DCP. The simulation results for the cold starter output voltage (V_{DDCS}) as a function of N and the width of the transistors of the DCP (W_{DPC}) are given in Figure 45. As can be seen, the integrated cold starter could still be further optimized when targeting the specified V_{DDCS} as a main design criterion. In this design, the use of N=11 or 13, and W_{DPC} ranging from around 30 to 100 μm, minimizes the input voltage required to achieve the boost converter startup.

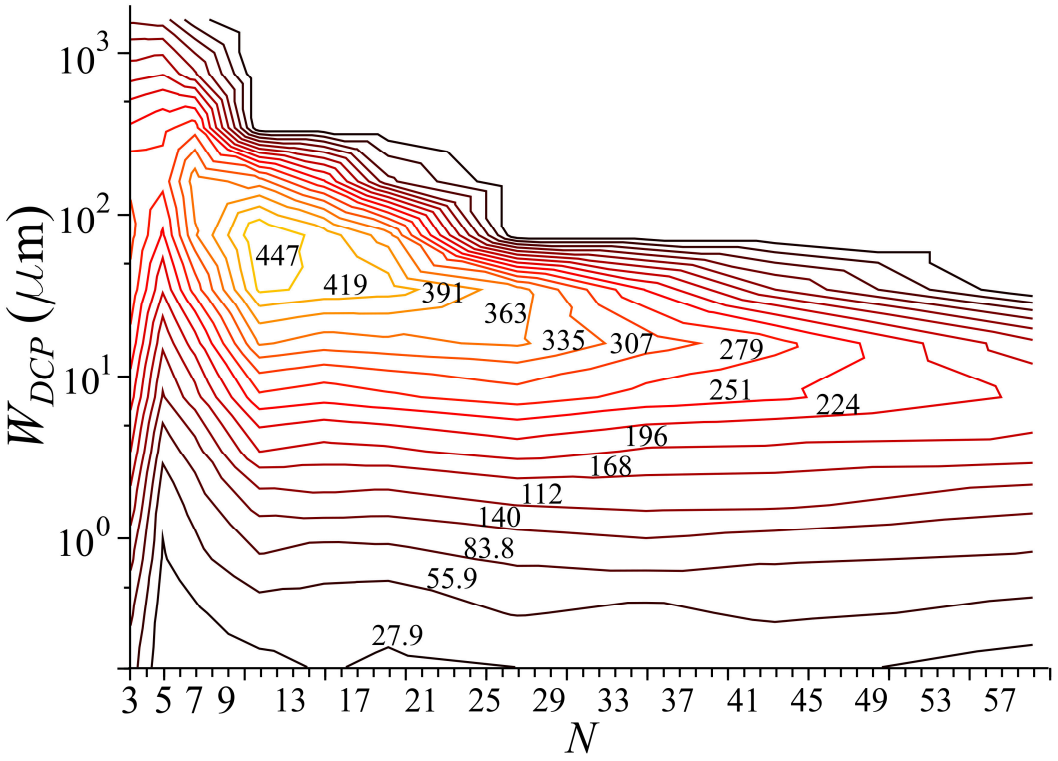


Figure 45 - Level curves for V_{DDCS} (mV) as a function of N and W_{DCP} using EDA tools (V_{TEG}=45 mV, and rectifier load of 5 MΩ).

5 ZERO-CURRENT SWITCHING

When the inductive boost converter is operated in discontinuous conduction mode, the HSS needs to be opened when the inductor current crosses zero, to avoid the inductor current becoming negative, which leads to a reverse energy flow that drains charges from the output capacitor. A common approach to this problem is the use of a diode as the HSS [33], [34], [35], [36]. However, this strategy is not appropriate for ULV applications due to the diode leakage current and forward voltage drop.

In order to improve the conversion efficiency, a MOS switch controlled by zero-current switching (ZCS) schemes is usually employed as the HSS. ZCS circuits are used for the opening of the HSS of the boost converter at the instant close to the zero crossing of the inductor current.

Some designs use voltage comparators to sense the voltage drop through the HSS in order to detect the zero-current crossing. However, since the HSS resistance is low when the switch is closed, the voltage drop across the HSS is low. The consumption of comparators can also impair considerably the conversion efficiency, especially at low P_{AV}. In [25], a duty-cycled comparator with offset cancelation is implemented to detect the zero-current crossing. Although the comparator is duty-cycled, the mean power consumption of the comparator is around 8 μW for V_{IN}=20 mV and 180 μW for V_{IN}=300 mV, which can be too high depending on P_{AV}.

Another common approach to performing the ZCS involves the use of digital schemes to detect the zero-current crossing through an indirect variable, which is the voltage at node M (v_M) [38], [42], [43]. In this solution, the static power consumption of the ZCS scheme is reduced due to the adoption of a digital solution. The main challenges associated with this type of implementation are to overcome the high detection error at low V_{IN} and to properly set the measurement delay (Δt_M) included in the ZCS circuit. In order to detect the zero-current crossing for the ultra-low V_{IN} provided by the TEG, in [46] the resolution is increased with the use of coarse and fine delay stages, which set the width of the pulse that opens the HSS. However, the ZCS circuit in [46] uses an external 0.6 V power supply to reduce the power consumption and operates only in a narrow input range (20-50 mV).

To open the HSS (PM_1) close to the zero-crossing of the current, we implemented the ZCS circuit shown in Figure 46, which shares some of the operation principles detailed in [38], but improves the detection accuracy, especially at low V_{IN}.

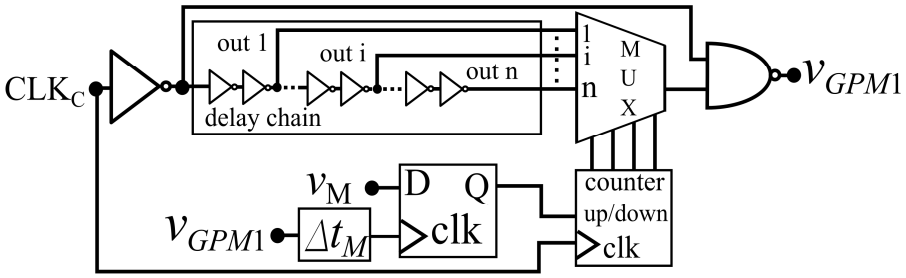


Figure 46 - ZCS circuit.

5.1 CIRCUIT OPERATION

Ideally, the ZCS circuit shown in Figure 46 generates a pulse signal (v_{GPM1}) that closes PM_1 during t_{OFF} and keeps it open during t_D and t_{ON}. Through the relation given by (2.20), each pulse width fits a specific input voltage level; and for high voltage gain, this is an almost linear relation. Thus, at each cycle of operation, the circuit needs to select the pulse width that best fits V_{IN}. For the adopted 4-bit system, 16 different values for the pulse width (t_{PULSE}) are generated.

The ZCS circuit (Figure 46) is comprised of a delay chain with 16 stages implemented with current-starved inverters (Figure 47), to generate a pulse with variable width, the sensing flip-flop, the measurement delay (Δt_M) block and the pulse selection circuit (multiplex + 4-bit counter). The ZCS block is supplied with V_{DD}, since this block is used only after the converter has started up and reached phase C.

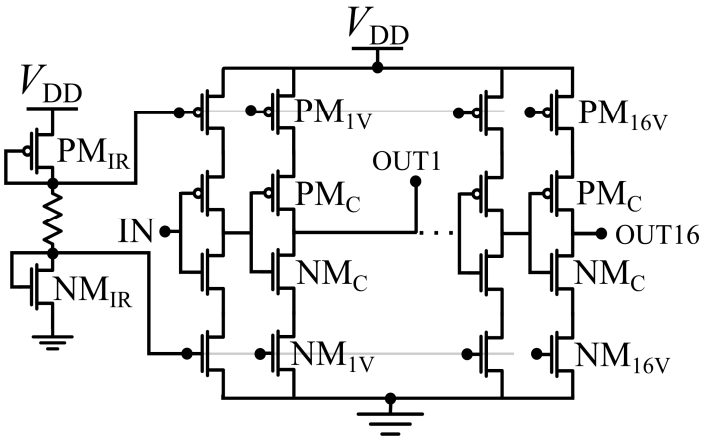


Figure 47 - Delay chain using current-starved inverters.

Using a D flip-flop, the circuit senses the voltage at node M a certain time after the opening of PM_1 (Δt_M) to evaluate whether the switch has opened before or after the inductor

current has crossed zero. If PM_1 opens after the zero-current crossing, the initial condition for the inductor current at the opening of PM_1 ($i_L(0)$) is negative and v_M will shift rapidly from V_{OUT} to zero. On the other hand, if PM_1 opens before the zero-current crossing ($i_L(0)>0$), the inductor current will still discharge through PM_1, which is now a high-resistance path, causing an overshoot at v_M (Figure 48). Only after complete inductor discharging will v_M shift from V_{OUT} to zero. Thus, if v_M is still higher than a specified switching point (logic high) a short time (Δt_M) after the opening of PM_1, early opening is detected. If v_M is lower than the switching point (logic low), late opening is detected by the sensing flip-flop. Based on these two measurement results, the counter is then incremented or decremented, in order to, respectively, increase or decrease the current pulse width applied to the gate of PM_1. The 4-bit counter controls a multiplexer which connects one of the outputs of the 16-stage delay chain to the pulse generation circuit, setting the pulse width.

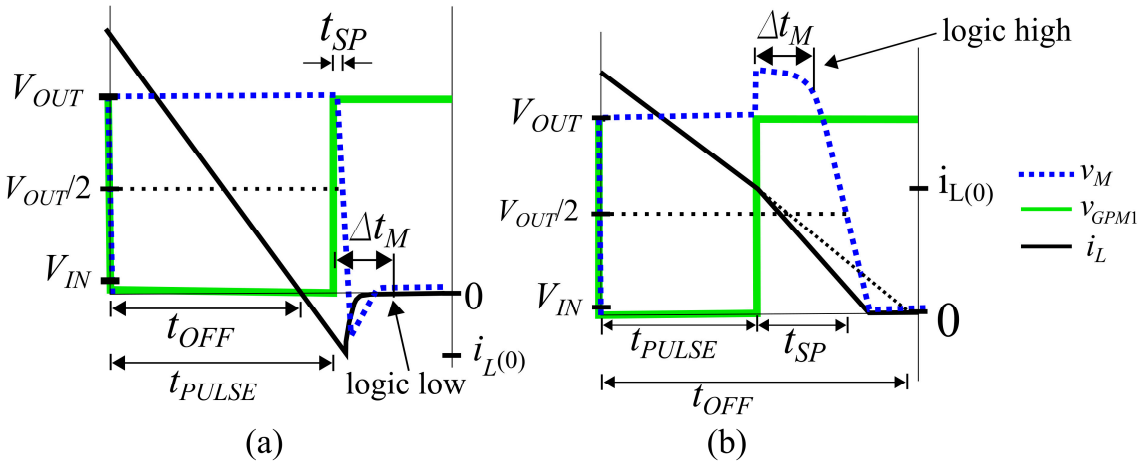


Figure 48 - Representation of inductor current, v_{GPM1} and v_M for the case of (a) late opening (b) early opening.

In steady state, the pulse width generated by the ZCS circuit (t_{PULSE}) will alternate around t_{OFF}. At one cycle of operation, t_{PULSE} will be slightly narrower than t_{OFF}; thus, early opening is detected and a control signal is sent to the counter in order to increase t_{PULSE}. In the next cycle, t_{PULSE}, which was increased in the previous cycle, is now slightly wider than t_{OFF}, and late opening is detected by the flip-flop. Similarly, the counter decreases the pulse width, returning to the previous condition where t_{PULSE} is slightly narrower than t_{OFF}, performing a loop and keeping t_{PULSE} at around the t_{OFF} value. Figure 49 shows the simulation results for i_L, v_{GPM1} and v_M for the case of the alternating early and late opening.

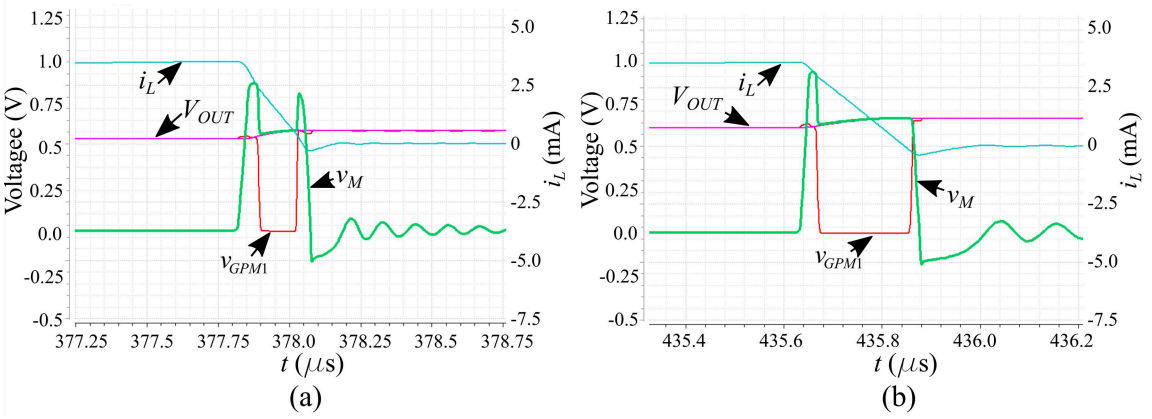


Figure 49 - Simulated i_L, v_{GPM1} and v_M for (a) early and (b) late opening.

5.2 THE MEASUREMENT DELAY

The time (Δt_M) after the opening of PM_1 at which node M is sensed is set by the measurement delay block, comprised of two inverters calibrated for the required delay (Δt_M). The discrimination between low and high logic levels at node M is performed by the sensing flip-plop, where a v_M value above the switching point ($v_M > V_{OUT}/2$) is considered as early opening and a value lower than the switching point ($v_M < V_{OUT}/2$) is considered to be late opening. Although in other works the measurement of node M has been used to detect early or late zero-current crossing, no specific criterion for determining the value of Δt_M is proposed.

The time interval between the opening of PM_1 and the crossing of v_M through the switching point of the sensing flip-flop ($V_{OUT}/2$) is defined as t_{SP}, as represented in Figure 48. The t_{SP} is not constant and it is a function of circuit parameters and initial conditions at the opening of PM_1. If Δt_M is set too short as compared to t_{SP}, late opening can be interpreted as early opening. On the other hand, if Δt_M is set too long, early opening can be interpreted as late opening. Therefore, the accuracy in detecting late or early opening for this type ZCS scheme is strongly related to the timing of the sensing circuit, which is set by the measurement delay (Δt_M).

The dependence of t_{SP} on the inductor current at the opening of PM_1 ($i_L(0)$) was analyzed by simulation for L=33 µH and L=220 µH, where the initial condition for the inductor current was swept and t_{SP} was measured by transient simulation. The results are shown in Figure 50 for the normalized $i_L(0)$.

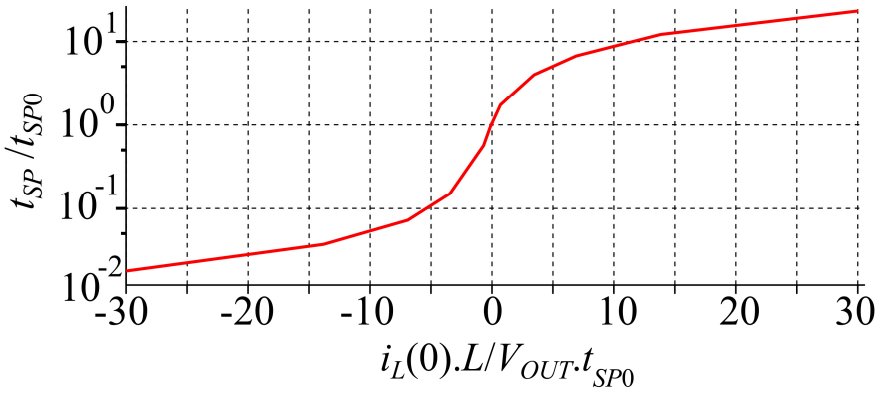


Figure 50 - Post-layout results for normalized t_{SP} vs $i_L(0)$.

As can be seen in Figure 50, t_{SP} is a monotonic function of $i_L(0)$. Therefore, the measurement delay Δt_M should be set at a value higher than the t_{SP} of negative $i_L(0)$, allowing v_M to reach to the switching point and late opening to be correctly detected. Also, Δt_M should be lower than the t_{SP} of positive $i_L(0)$, preventing v_M from reaching the switching point and allowing early opening to be correctly detected. Hence, setting Δt_M equal to the value of t_{SP} for $i_L(0)=0$ (t_{SP0}) allows the early or late opening of PM_1 to be correctly discriminated. For L=33 µH, the simulated value of t_{SP0} was 13 ns, and for L=220 µH it was 33ns, as shown in Figure 51.

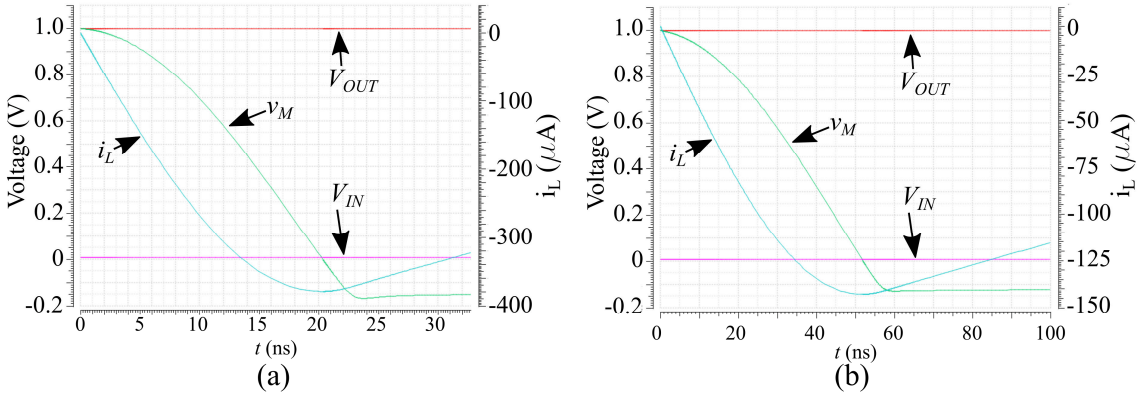


Figure 51 - Measured waveforms after opening of PM_1 for $i_L(0)=0$ and (a) L=33 µH or (b) L=µ220 H.

Figure 52 shows how the incorrect choice of the measurement delay affects the readings of logic levels.

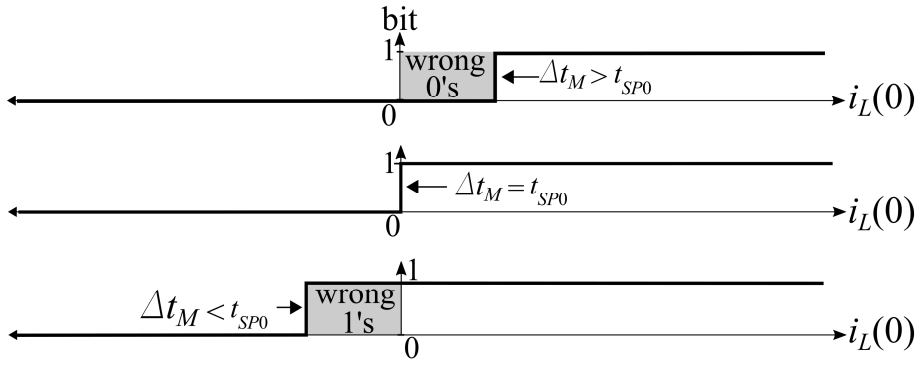


Figure 52 - Representation of the sensed logic levels for different Δt_M values.

In order to obtain an analytical expression for t_{SP0}, in Appendix D we analyze the time response of the second-order system comprised of the capacitance at node M (C_{MPAR}), the inductance (L) and the parasitic resistance of the switches (Figure 53), yielding

$$t_{SP0} = \sqrt{LC_{MPAR}} \arccos 0.5 \approx 1.05\sqrt{LC_{MPAR}} \,. \tag{5.1}$$

Hence, setting Δt_M equal to t_{SP0} given by expression (5.1) minimizes the detection error. The result obtained with (5.1) is in close agreement with the simulation results.

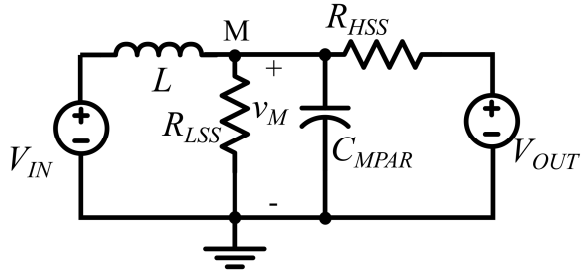


Figure 53 - Equivalent circuit for time response calculations.

In steady-state, the circuit is designed to alternate between two consecutive values of pulse width that cause alternating logic level readings. If Δt_M is equal to t_{SP0}, these pulse width values also generate alternating late and early openings (as represented in Figure 48), keeping $i_L(0)$ as close as possible to zero. However, inadequate values of Δt_M can lead to an alternation around a value of $i_L(0)$ different from zero. In this case, the pulse width values could generate only early or only late openings, which increases the detection error and decreases the conversion efficiency.

5.3 PULSE SCALING

The range of t_{PULSE} provided by the delay chain should cover the range of t_{OFF}, which is dependent on the specified range of V_{IN}. For a system with b number of bits, there are 2^b values of t_{PULSE}. Thus, to increase the accuracy of the ZCS scheme, the number of bits could be increased, but the power consumption of the ZCS block increases roughly by a factor of two for each additional bit of resolution.

In order to make t_{PULSE} as close as possible to t_{OFF}, we first define the zero-current detection error ($ZCDE$) for a given t_{OFF} and t_{PULSE} as

$$ZCDE = \frac{|t_{PULSE} - t_{OFF}|}{t_{OFF}}. \tag{5.2}$$

Since in steady state the system alternates between two t_{PULSE} values, one slightly narrower and one slightly wider than t_{OFF}, the overall $ZCDE$ for the given t_{OFF} is the average of the $ZCDE$ for the two alternating t_{PULSE} values. Using (5.2), the $ZCDE$ was plotted as a function of V_{IN} in Figure 54 for different bit resolutions, dividing the t_{PULSE} range linearly.

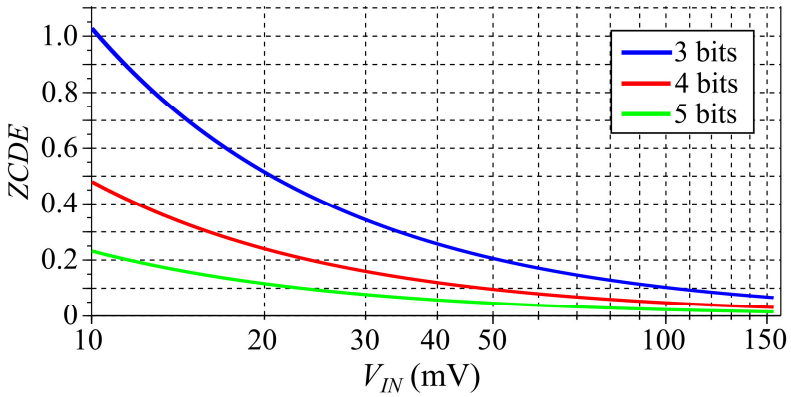


Figure 54 - Detection error for different bit resolutions.

As can be seen, the $ZCDE$ is increased for low input voltages, since the step size in this range is greater when compared to the respective t_{OFF}. To overcome this problem, we propose the use of the geometric scaling of the t_{OFF} range, decreasing the step size for low t_{PULSE}. Hence, the scaling factor (SF) and the pulse width generated by each of the delay outputs (t_{PULSE}(i)) are given by

$$SF = \left(\frac{V_{IN,MAX}}{V_{IN,MIN}} \right)^{\frac{1}{n-1}}, \tag{5.3}$$

$$t_{PULSE}(i) = SF^{i-1} t_{PULSE}(1). \tag{5.4}$$

where $V_{IN,MIN}$ and $V_{IN,MAX}$ are the specified minimum and maximum specified V_{IN}, respectively, and $n=2^b$ is the number of delay stages. The value of $t_{PULSE}(1)$ is equal to t_{OFF} for the case of $V_{IN}=V_{IN\_MIN}$, and can be determined by the boost gain expression (2.20), since V_{OUT}=1 V and t_{ON} is fixed (2.1). The detection error is plotted in Figure 55, where the geometric scaling is compared with the linear scaling of t_{PULSE} for a 4-bit system.

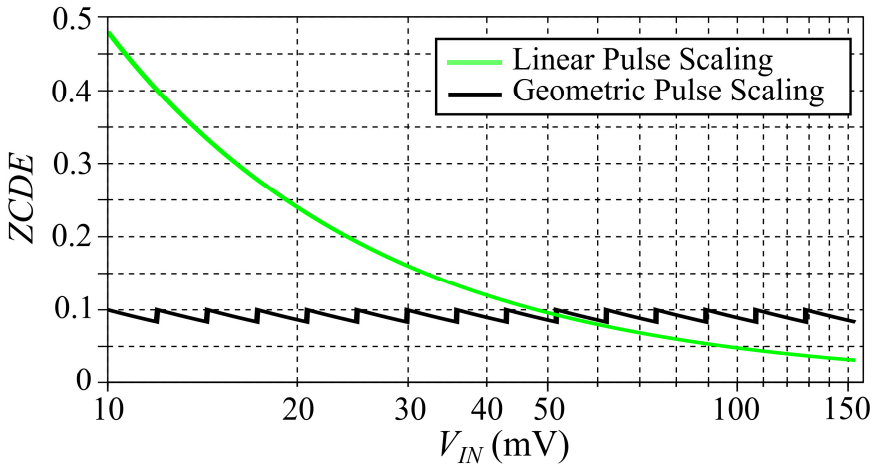


Figure 55 - Detection error for geometric and linear pulse scaling.

It can be seen that the geometric scaling equalizes the *ZCDE* throughout the whole V_{IN} range, mitigating the problems of detection accuracy in the low V_{IN} range, which reflects in a loss in the conversion efficiency. For early opening, some energy is lost in the PM_1 series resistance during the remaining discharging period of the inductor. On the other hand, late opening generates a reverse energy flow that partially discharges the output capacitor. Thus, with the aid of Figure 48, we define the ZCS conversion efficiency (η_{ZCS}) as the ratio of the energy transferred to the load for a given t_{PULSE} (E_{TPULSE}) to the energy transferred to the load for the case of ideal ZCS (E_{ZCS}), which is obtained when $t_{PULSE} = t_{OFF}$, leading to

$$\eta_{ZCS} = \frac{E_{TPULSE}}{E_{ZCS}} = 1 - \frac{k_L \left(t_{OFF} - t_{PULSE}\right)^2}{t_{OFF}^{\ 2}}. \tag{5.5}$$

For the case of $i_L(0)<0$ (late opening), k_L has no meaning and is equal to 1. For the case of $i_L(0)>0$ (early opening), k_L represents the fraction of the energy stored in the inductor at the opening of PM_1 that is lost in PM_1, and it can be estimated by the change in the inductor current slope after the opening of the HSS (Figure 48 (b)).

Since in steady-state the system alternates between two values of t_{PULSE}, the efficiency of the proposed ZCS scheme is given by the average of the efficiency given by (5.5) for the two alternating values of t_{PULSE}. Using (5.5), η_{ZCS} is plotted for the case of linear and geometric pulse scaling for a 4-bit system in Figure 56.

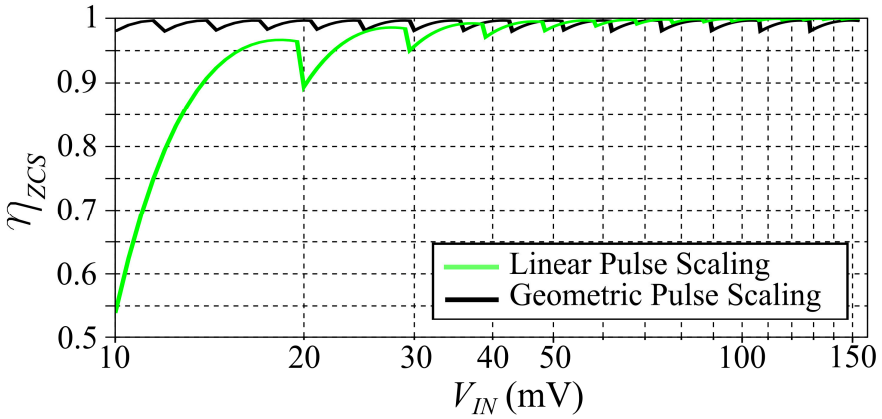


Figure 56 - η_{ZCS} for geometric and linear pulse scaling (k_L =0.3).

Using the proposed scaling strategy, the pulse width and the delay introduced by each stage should be in accordance with the values shown in Table 9. The final sizing of the delay chain devices, determined by simulation, as reported in [64], can be seen in Table 10.

Table 9 - Pulse width and delay.

Stage	Pulse width	Delay	Stage	Pulse width	Delay
1	250 ns	250 ns	9	1.07 µs	179 ns
2	300 ns	50 ns	10	1.29 µs	215 ns
3	360 ns	60 ns	11	1.55 µs	258 ns
4	432 ns	72 ns	12	1.86 µs	310 ns
5	518 ns	86 ns	13	2.23 µs	372 ns
6	622 ns	104 ns	14	2.68 µs	446 ns
7	746 ns	124 ns	15	3.21 µs	535 ns
8	895 ns	149 ns	16	3.85 µs	642 ns

Table 10 - Sizing of current-starved inverters and delay time of each stage.

Device	Width	Length	Device	Width	Length
PM_C	1.6 µm	1.2 µm	$N(P)M_{8V}$	3.05 µm	1.2 µm
NM_C	960 nm	1.2 µm	$N(P)M_{9V}$	2.6 µm	1.2 µm
$N(P)M_R$	960 nm	3 µm	$N(P)M_{10V}$	1.87 µm	1.2 µm
$N(P)M_{1V}$	5.5 µm *	1.2 µm	$N(P)M_{11V}$	1.54 µm	1.2 µm
$N(P)M_{2V}$	6.83 µm	1.2 µm	$N(P)M_{12V}$	1.35 µm	1.2 µm
$N(P)M_{3V}$	5.9 µm	1.2 µm	$N(P)M_{13V}$	1.17 µm	1.2 µm
$N(P)M_{4V}$	5.4 µm	1.2 µm	$N(P)M_{14V}$	1 µm	1.2 µm
$N(P)M_{5V}$	4.85 µm	1.2 µm	$N(P)M_{15V}$	850 nm	1.2 µm
$N(P)M_{6V}$	4.15 µm	1.2 µm	$N(P)M_{16V}$	720 nm	1.2 µm
$N(P)M_{7V}$	3.5 µm	1.2 µm			

* The first stage is comprised of five cascaded stages, each stage calibrated for a 50 ns delay.

Figure 57 shows the simulation results for the pulse width obtained for each stage [64] and the proportional deviation of each of the corners. It should be noted that the current reference uses an on-chip resistor of 8.1 M Ω, with tolerance of ± 20%, which also affects the precision of the system.

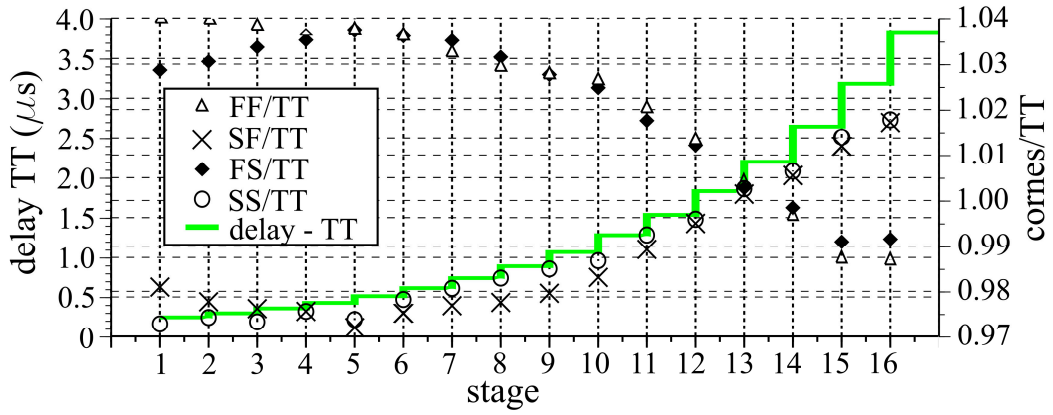


Figure 57 - Pulse width and corner deviation of each delay chain stage.

In order to evaluate the effect of Δt_M on the *ZCDE* and η_{ZC}, we use the relation given in Figure 50 and (2.12) to determine the two alternating values of t_{PULSE} for any given Δt_M and

V_{IN}, enabling (5.2) and (5.5) to be calculated for the geometric pulse scaling. Considering our design parameters (L =220 µH, $V_{IN,MIN}$ =10 mV, $V_{IN,MAX}$ =154 mV, SF=1.2 and n=16), we plot $ZCDE$ and η_{ZCS} vs V_{IN} for different values of Δt_M in Figure 58 and Figure 59, respectively.

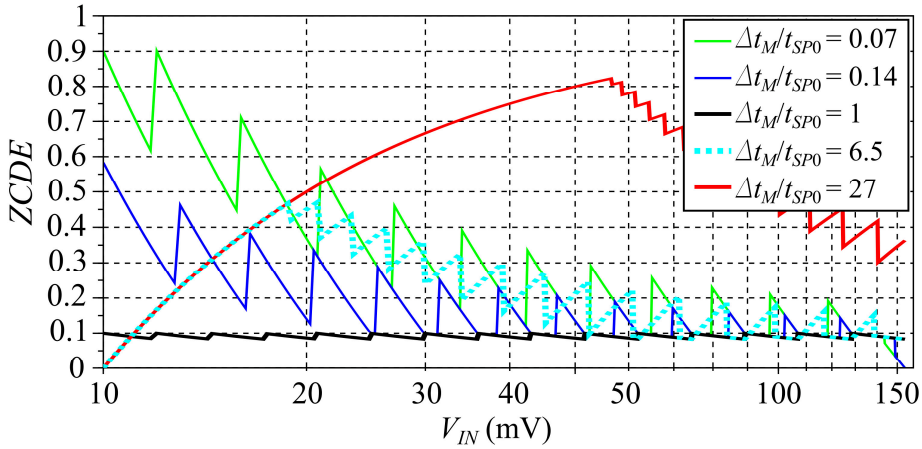


Figure 58 - $ZCDE$ vs V_{IN} for different Δt_M values using geometric pulse scaling.

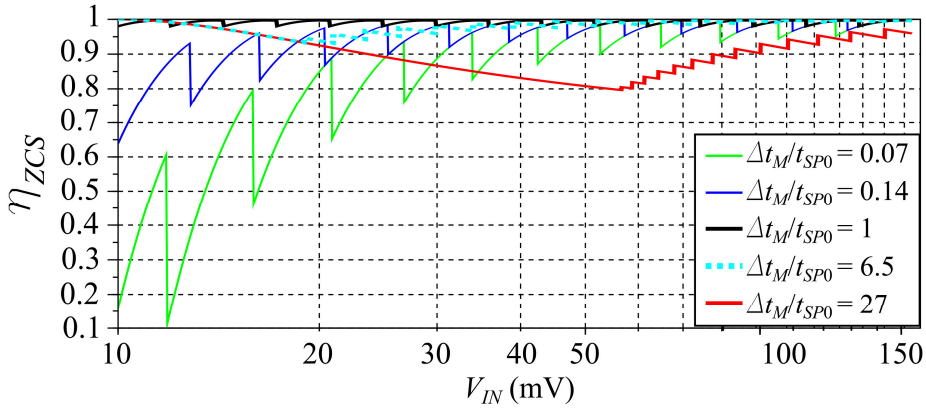


Figure 59 - Plot of η_{ZCS} vs V_{IN} for different Δt_M values using geometric pulse scaling (k_L =0.3).

As can be observed, setting Δt_M according to (5.1) maximizes the efficiency, which can be significantly impaired as Δt_M deviates from t_{SP0}. Values of Δt_M much lower than t_{SP0} have a strong influence on the efficiency, especially at low V_{IN}. It should be noted that when Δt_M is properly set by (5.5), the results are equal to those in Figure 55 and Figure 56 for the geometric scaling, as expected.

6 EXPERIMENTAL RESULTS

The DC-DC converter was integrated in Global Foundries 130 nm CMOS technology supported by Cadence EDA tools in the design phase. The availability of ZVT transistors used in the ESRO is an important requirement when determining the technology. The complete circuit architecture is shown in Figure 60. The off-chip components are the boost inductor L, C_{IN}, C_{OUT} and the four ESRO inductors. Three chips were measured and the results are shown for chip 1 unless otherwise stated.

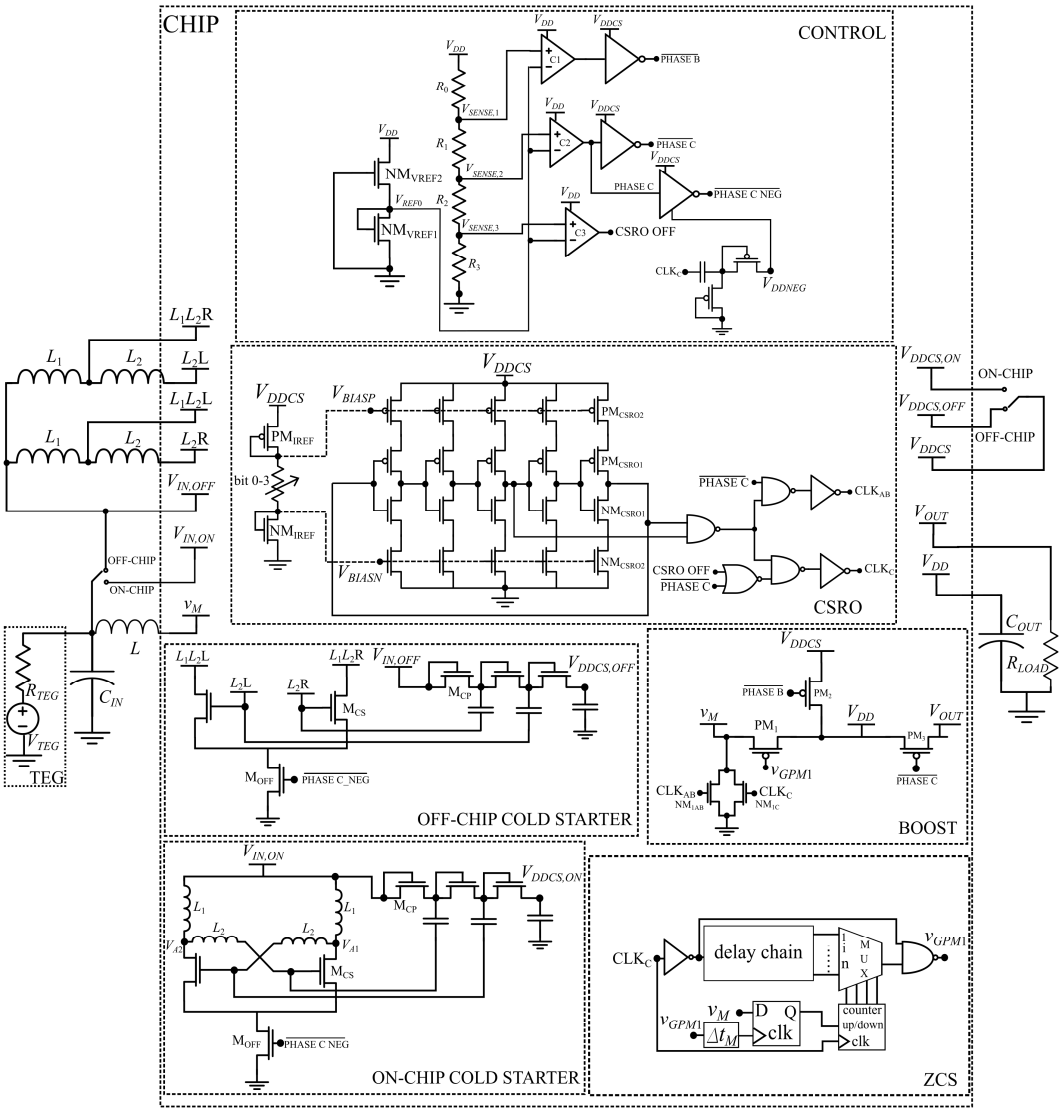


Figure 60- Schematic of the implemented converter.

Figure 61 shows a micrograph of the fabricated chip with a total area of 1.5x1.5 mm^2, including the pads. For the measurements, V_{TEG} was emulated by a variable power supply (Keithley 2401 Source Meter) and R_{TEG} was set with series resistances of either 6 Ω or 40 Ω, combined with an off-the-shelf inductor of either 33 µH or 220 µH, setting the MPPT as defined by (2.71). The input and output capacitors are defined by (A.11) and (B.8), targeting a proportional ripple of 10% for L=33 µH, which leads to the adopted commercial values of C_{IN}=22 µF and C_{OUT}=2.2 µF. A photograph of the test bench setup is shown in Figure 62.

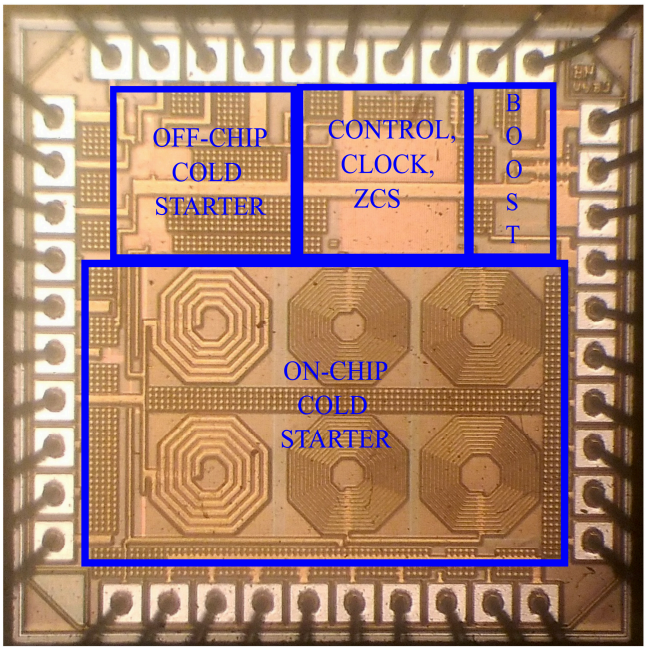


Figure 61 - Micrograph of the fabricated chip.

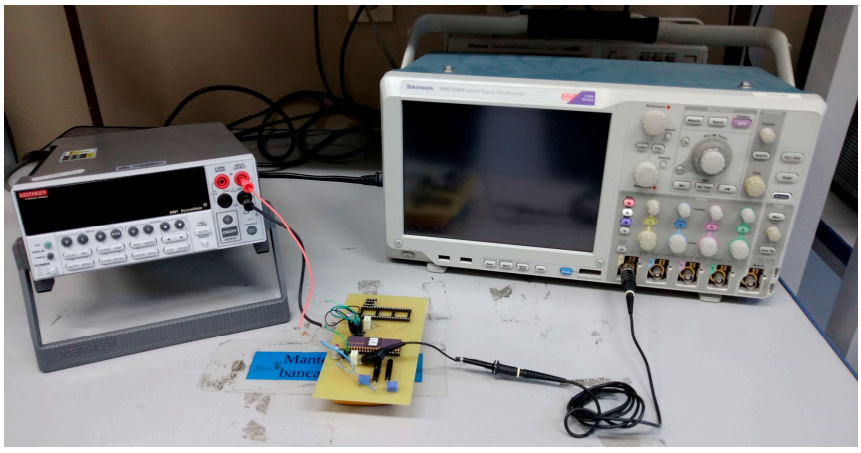


Figure 62 - Test bench setup used for the measurements.

6.1 STARTUP

The startup of the converter was achieved with either off-chip or on-chip ESRO inductors. Due to the low Q of integrated inductors, the minimum startup voltage achieved in measurements was 90 mV for the on-chip design, which is higher than the simulation results of 70 mV. Although the signal V_{A1} was externalized in one specific pin, the oscillation frequency of the on-chip ESRO was not measured due to the loading effect, but the post-layout simulations have shown it to be in the range of 400 MHz. The parasitic capacitance of the metal tracks, pad, pin and bondwire connected to V_{A1} contribute to the deterioration of the on-chip startup.

For the ESRO using off-the-shelf inductors, several combinations of inductors L_1 and L_2 were tested in order to find the values which start up the converter at the lowest input voltage, as shown in Table 11. The startup voltage is defined as the minimum input voltage which allows the boost converter to reach steady-state operation (phase C).

Table 11 - Startup voltages for several ESRO inductor combinations.

L_1 (μH)	L_2 (μH)	Startup Voltage (mV)
4.7	33	28
4.7	1000	26
10	100	20
4.7	220	20
4.7	330	20
4.7	470	19
4.7	100	15
1	100	11

According to (4.2), the minimum value achievable for the startup of the oscillator is a function of not only the ratio L_1/L_2 but also the losses in the inductors and the rectifier input conductance (G_O). The combination of inductor values that led to the minimum supply voltage to start up the boost converter was L_1=1 μH (Q=40 @1MHz) and L_2=100 μH (Q=100 @1MHz). For these values of L_1 and L_2, the ESRO started to oscillate for an input voltage of 3.3 mV, which provided a voltage of 63.4 mV at node V_{DDCS}. However, this is not high enough

to power the clock circuit. As the input voltage increases, V_{DDCS} also increases, making it possible to start up the boost converter.

Figure 63 shows the voltage at node V_{DDCS} against the input voltage level. The boost converter can fully start up at V_{IN}=11 mV for chips 1 and 2 and at V_{IN}=10.9 mV for chip 3, achieving steady-state operation (phase C). It should be noted that the oscilloscope probe imposes a significant load (10 MΩ) at node V_{DDCS}. Another cold starter test, in which nodes V_{A1}, V_{A2} and V_{DDCS} were simultaneously measured against V_{IN}, is also shown in Figure 63. The effect of loading the ESRO output nodes using the probes (10 MΩ - 3.8 pF) clearly impairs the startup performance, as can be noted by the difference in V_{DDCS} when V_{A1} and V_{A2} are not being measured.

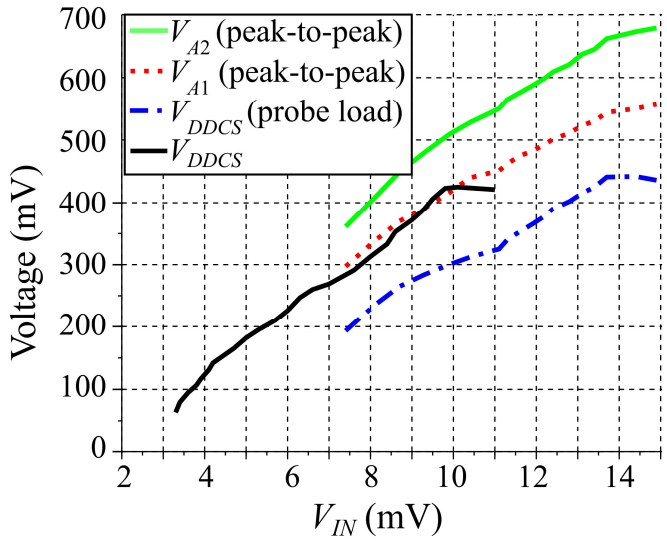


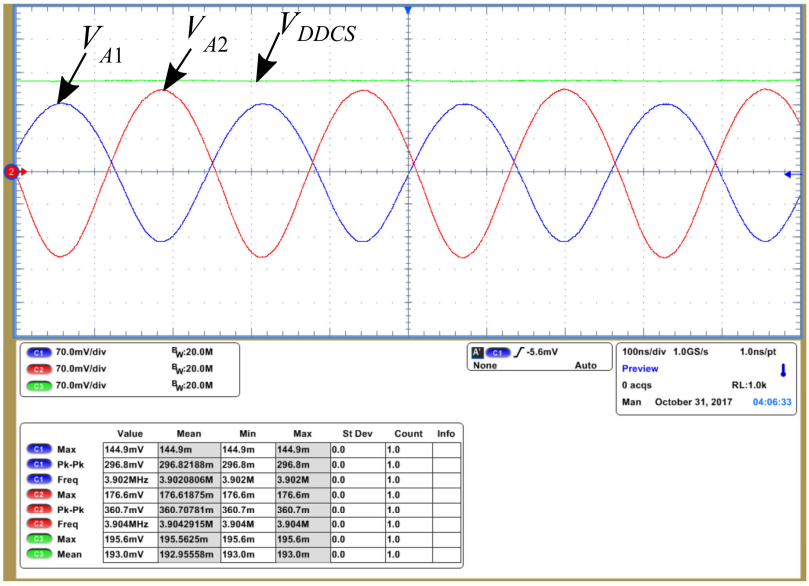
Figure 63 - V_{DDCS}, V_{A1} and V_{A2} vs V_{IN} for R_{TEG}=6Ω.

In Figure 64, V_{A1}, V_{A2} and V_{DDCS} are plotted against time for input voltages of 7.4 and 14.9 mV, which are the minimum V_{IN} required to startup the ESRO and the minimum V_{IN} to start up the boost converter, respectively, when nodes V_{A1} and V_{A2} are loaded by the oscilloscope probes. The measured oscillation frequency is around 3.9 MHz for the values of L_1=1 µH and L_2=100 µH.

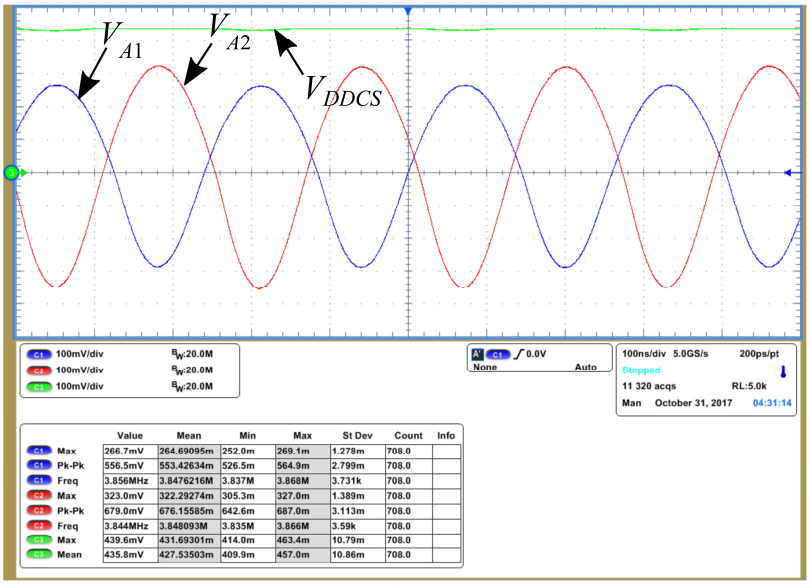
Since the ESRO implemented with off-chip inductors provided startup at lower V_{IN} levels, the following tests described in the thesis were performed using off-chip inductors for the ESRO implementation.

6.2 V_{DD} BUILDUP

Figure 65 shows V_{DDCS} and CLK_{AB} during startup. As can be seen, after the cold starter has established the voltage V_{DDCS}, the CSRO starts to oscillate. Every time the CSRO switches the transistor NM_{1AB}, V_{DDCS} drops, showing that the amount of energy needed to



(a)



(b)

Figure 64 - V_{DDCS}, V_{A1} and V_{A2} for (a) V_{IN}=7.4 mV and (b) 14.9 mV (R_{TEG}=6 Ω).

switch the LSS affects the loading of the cold starter. A larger area switch would lead to a higher voltage drop at the V_{DDCS} node, thus increasing the V_{IN} required for a given V_{DDCS} level. Hence, the dual switching scheme using a specific switch with smaller dimensions during startup is an important strategy in reducing the minimum startup voltage of the converter.

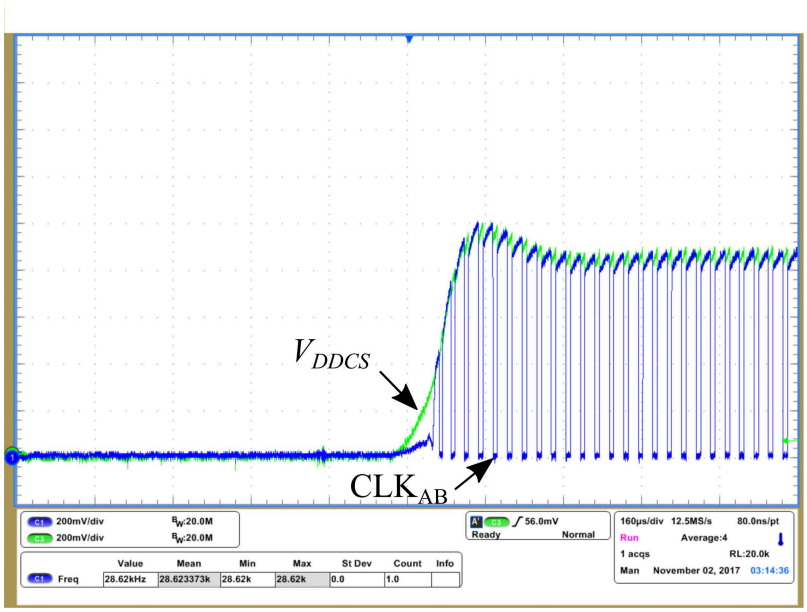


Figure 65 - V_{DDCS} and CLK_{AB} during startup.

After CLK_{AB} has been established, node V_{DD} starts to build up. In Figure 66, the complete buildup of V_{DD}, V_{DDCS} and V_{OUT} is shown for V_{IN}=30 mV. As can be noted, V_{DD} starts to increase once V_{DDCS} is established. When V_{DD} reaches approximately 420 mV, the circuit enters phase B, where nodes V_{DDCS} and V_{DD} are connected to each other through PM_2 and the load is connected to V_{DD} through PM_3. At this point, charge redistribution between C_{OUT} and C_{OCS} occurs. Once V_{DD} reaches approximately 600 mV, the ESRO is disabled, switch NM_{1C} replaces switch NM_{1AB} and the zero-current switching (ZCS) scheme starts to operate. At this point, V_{DD} (or V_{DDCS}) starts to increase at a faster rate due to the gain in the efficiency delivered by the ZCS scheme, subsequently reaching steady state at close to 1 V. The transition between phases occurred at voltage levels lower than those designed in Chapter 3, but no significant effect was observed in terms of the system performance.

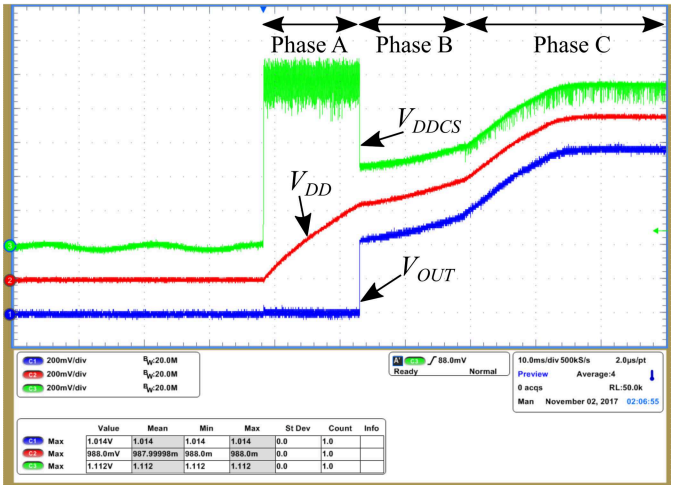


Figure 66 - V_{DDCS} , V_{DD} and V_{OUT} buildup.

6.3 ZERO-CURRENT SWITCHING

In order to evaluate the performance of the ZCS scheme, v_M and v_{GPM1} were measured. Since the capacitance of the oscilloscope is of the same order of magnitude as the capacitance of both nodes, some degradation is introduced by the measurement equipment. Figure 67 shows the steady-state waveform of v_{GPM1}, where the pulse used for switching PM_1 is observed. Figure 68 shows the waveform of v_M, where it is possible to see the alternation between early and late openings of switch PM_1. As can be noted, the early opening of PM_1 generates a glitch in the waveform of v_M, whereas late opening does not. Figure 69 shows the v_M waveform in detail for early and late openings.

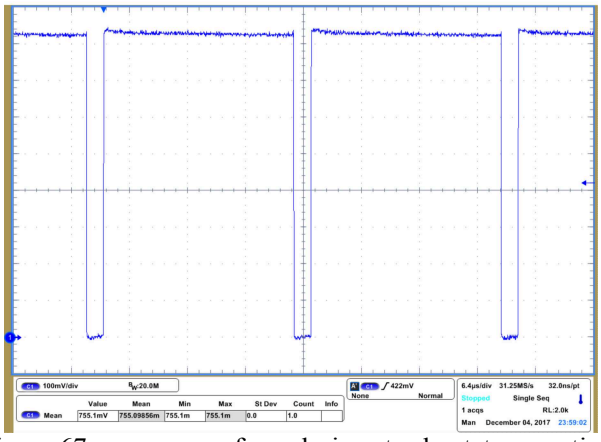


Figure 67 - v_{GPM1} waveform during steady-state operation.

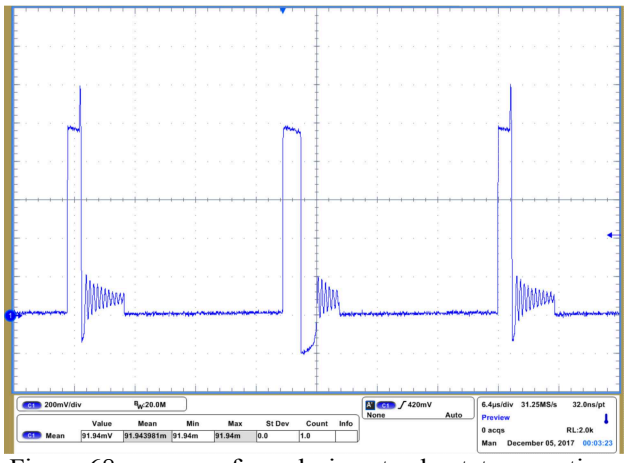
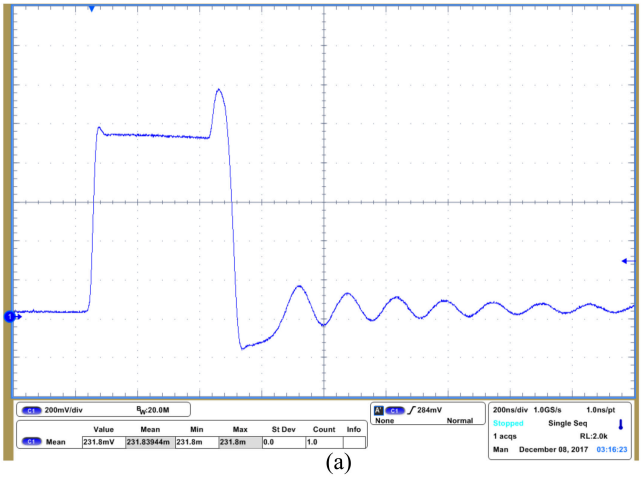
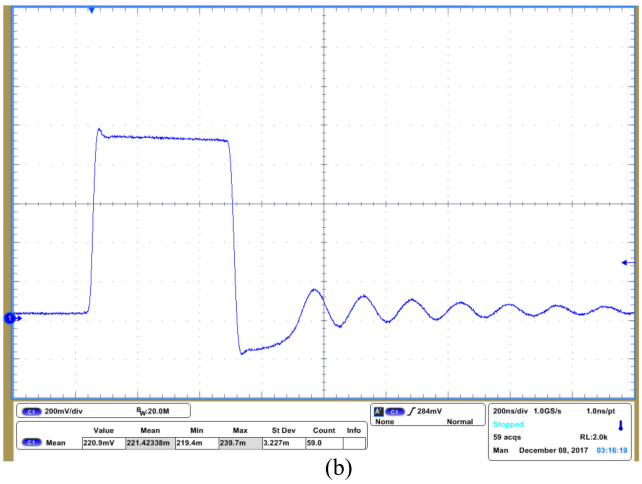


Figure 68 - v_M waveform during steady-state operation.



(a)

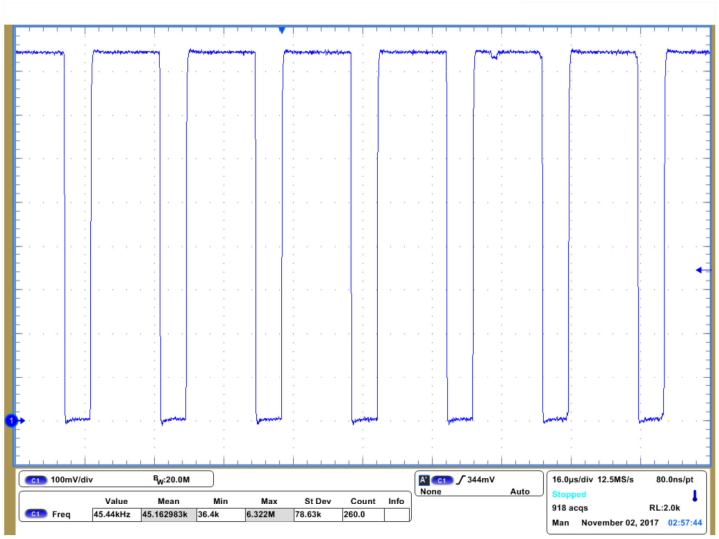


(b)

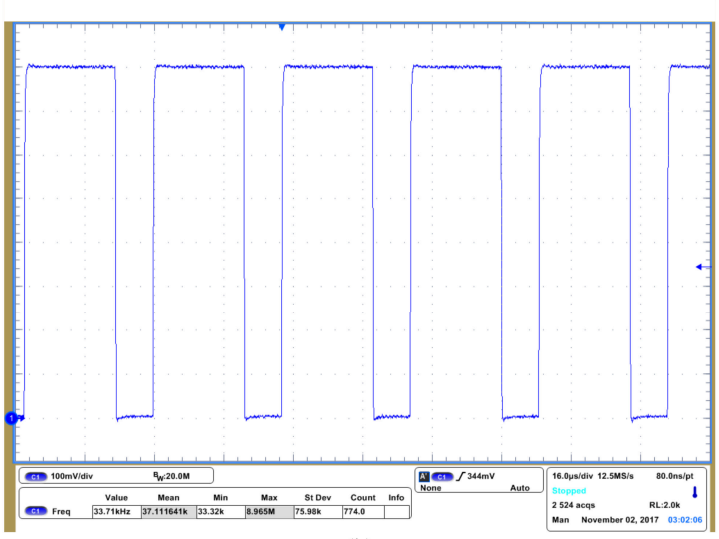
Figure 69 - v_M waveform for (a) early opening and (b) late opening of PM_1.

6.4 CLOCK FREQUENCY

As explained in Chapter 3, four external bits are used to control f_{SW} in order to maximize the harvesting efficiency. In Figure 70 and Figure 71, the measured waveform of signal CLK_C is shown for maximum (word 1111) and minimum (word 0000) settings.



(a)



(b)

Figure 70 - CLK_C signal for (a) maximum (45.44 kHz) and (b) minimum (33.71 kHz) frequency settings.

6.5 EFFICIENCY

The end-to-end and extraction efficiencies were measured for different R_{TEG} and input voltages, as shown in Figure 71. A resistive load was varied at the output to perform the measurements, allowing the maximum end-to-end and extraction efficiencies to be measured

for each value of input voltage. The minimum measured input voltage capable of sustaining steady-state operation in phase C was 7.3 mV for chip 1, 7.6 mV for chip 2 and 7.5 mV for chip 3, for a 10 MΩ load (oscilloscope load) connected at the output. For this condition, the output voltage is 690 mV and $\eta_{end\text{-}to\text{-}end}$ is 2.4% for chip 1.

The system delivers better efficiencies for R_{TEG}=40 Ω as compared to R_{TEG}=6 Ω. For V_{IN} > 42 mV, $\eta_{end\text{-}to\text{-}end}$ reaches a plateau with a value of the order of 83%. The minimum input voltage required to achieve a 50% end-to-end efficiency is approximately 10.5 mV. The extraction efficiency is higher than 95% for the whole V_{IN} range, showing that the technique of matching the TEG resistance with the input resistance of the converter ensures the MPPT. The maximum measured output power was 2.8 mW for V_{IN} of 132 mV and R_{TEG} of 6 Ω.

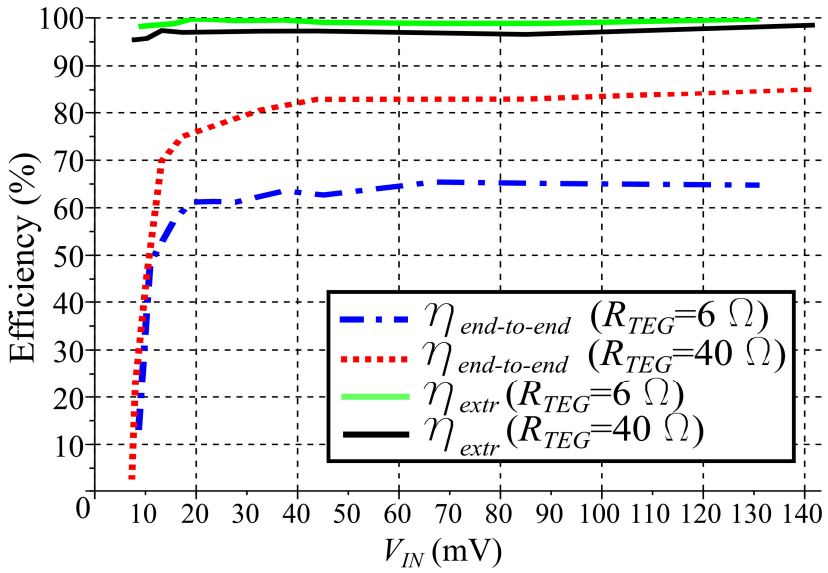


Figure 71 - Maximum end-to-end and extraction efficiencies vs V_{IN} for different R_{TEG}.

Keeping V_{TEG} fixed and varying the load, the efficiency was measured for different load conditions. Since for light load conditions V_{OUT} is kept constant, at around 1 V, a decrease in both end-to-end and extraction efficiencies is expected when the load current decreases. Figure 72 shows the variation in the end-to-end efficiency with the load current for different V_{TEG} for R_{TEG}=40 Ω. One can observe two specific regions. In one region, V_{OUT} is limited to 1 V and the efficiency is proportional to the load current. In the other region V_{OUT} is not limited and thus the system maximizes the extraction efficiency. The threshold between the two regions is indicated for V_{TEG}=20mV

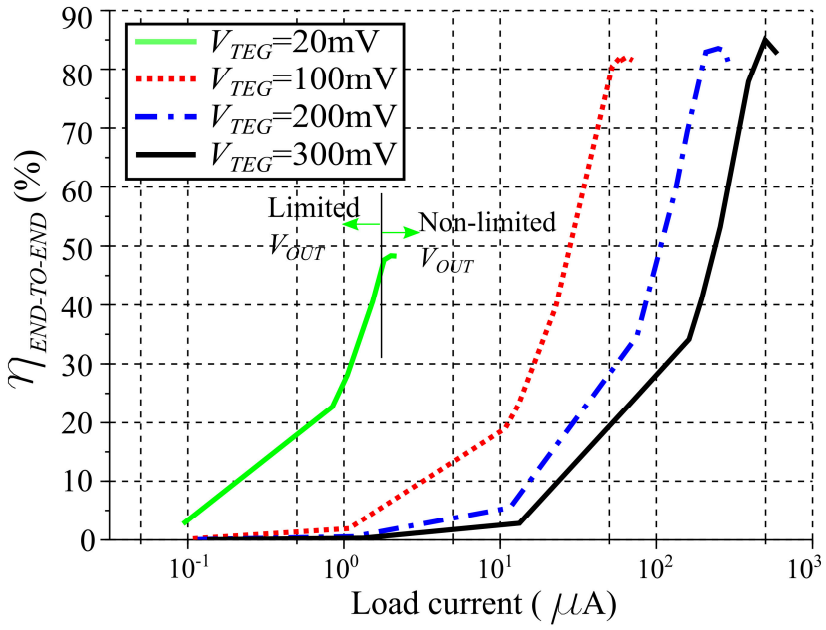


Figure 72 - End-to-end efficiency vs load current for different V_{TEG} values (R_{TEG}=40 Ω).

7 DISCUSSION AND CONCLUSIONS

7.1 COMPARISION WITH RELATED STATE-OF-THE-ART CONVERTERS

Table 12 shows a comparison of the specs for similar state-of-the-art harvesters, with regard to the main figures of merit for thermal energy harvesting converters.

Table 12 - Comparison with other state-of-the-art boost converters for energy harvesting.

Work	Technology	Year	Minimum V_{IN}	Startup Voltage	Max. P_{OUT}	Off-chip comp.	Peak $\eta_{end\text{-}to\text{-}end}$	V_{IN} for 50% Eff
[42]	130 nm	2010	20 mV	-	100 µW	3	52%	-
[43]	0.35 µm	2011	25 mV	-	300 µW	3	58%	-
[29]	65 nm	2012	80 mV	80 mV	-	2	72%	-
[33]	130 nm	2012	40 mV *	40 mV	2.7 mW	9	61%	175 mV *
[38]	65 nm	2013	28 mV	50 mV *	1.2 mW	6	73%	32 mV
[34]	130 nm	2014	21 mV	21 mV	2 mW	5	74%	430 mV
[44]	180 nm	2015	70 mV	-	-	3	79%	-
[25]	130 nm	2015	10 mV	220 mV	22 mW	3	83%	20 mV
[39]	130 nm	2016	50 mV *	50 mV *	1.3 mW	9	65%	50 mV *
[41]	65 nm	2018	40 mV*	40 mV *	3.5 mW	6	75%	70 mV *
[22]	65 nm	2018	7 mV	210 mV	1.8 mW	3	71.5%	-
[21]	180 nm	2018	12 mV*	260 mV	6.48 mW	3	90.8%	18 mV*
[31]	180 nm	2018	60 mV	60 mV	-	3	47%	-
[28]	180 nm	2019	25 mV	57 mV	-	2	-	-
[23]	180 nm	2019	50 mV *	190 mV *	400 µW	4	60%	80 mV *
[37]	180 nm	2020	20 mV *	38 mV	8 mW	7	81.5%	25 mV *
This work	130 nm		7.3 mV	11 mV ** 90 mV ***	2.8 mW	7 ** 3 ***	85%	10.5 mV

* Value expressed in terms of the TEG open-circuit voltage.

** ESRO implemented with off-the shelf inductors.

*** ESRO implemented with integrated inductors.

The startup voltage obtained in this research is the lowest reported to date with the cost of four external inductors. Other designs in which the startup voltage is low [33], [34], [37], [41] also have a high number of off-chip components. The converters reported in [38], [25] and [21] achieved similar efficiency values at the low-voltage limit, but do not provide startup at low voltage.

The combination of high efficiency at low V_{IN} and low startup voltage enables efficient and autonomous thermal energy harvesting. With regard to these two characteristics, the work in [37] is the only referenced work which has obtained similar values for both figures of merit when compared to the converter reported herein.

7.2 CONCLUSIONS

An efficient converter topology with self-startup for ULV thermal energy harvesting applications was developed and implemented in 130 nm technology. The developed topology is capable self-startup and operation at ultra-low input voltages, providing high end-to-end efficiency from the μW to the mW range, in a wide range of input voltages and for different types of TEGs, meeting the requirements specified for the converter.

The model developed for the boost converter for thermal energy harvesting allows the designer to define the most important design variables in order to achieve high conversion and extraction efficiencies, as well as to provide system operation at ultra-low input voltages. The proposed oscillator and rectifier co-design methodology enables the design of a cold starter which is able to startup at ULV. The proposed zero-current swicthing (ZCS) circuit maximizes the conversion efficiency of the boost converter operating in DCM, while maintaining the low consumption of the ZCS scheme.

The experimental results of this thesis show a peak end-to-end efficiency of 85% for a 140 mV input voltage and 50% efficiency for input voltages as low as 10.5 mV. The circuit achieved ULV startup from an input voltage of 11 mV when using off-chip inductors for the ESRO implementation. To the best of our knowledge, this is the lowest startup voltage reported in the literature for this type of converter. For the fully-integrated ESRO, the startup was achieved from an input voltage of 90 mV.

The results show the circuit feasibility for startup and efficient steady-state operation from TEGs at ULV, enabling harvesting even when the temperature gradient is of the order of

1 ^{o}C, making possible the autonomous and continuous operation of IoT devices powered from the thermal energy provided by the human body.

APPENDIX A – INPUT RIPPLE AND INPUT CAPACITOR

In order to define the value of the input ripple and capacitance, the Kirchhoff's current law is applied at the input node, leading to

$$i_{CIN}(t) = i_L(t) - I_{TEG}\,. \tag{A.1}$$

The time constants used in Figure 6 (b) are further divided according to Figure 73. The new time constants can be calculated by the graph

$$\frac{\frac{V_{IN}t_{ON}}{L} - I_{TEG}}{t_{ONy}} = \frac{I_{TEG}}{t_{ONx}} = \frac{I_{TEG}}{t_{ON} - t_{ONy}}, \tag{A.2}$$

$$\frac{\frac{V_{IN}t_{ON}}{L} - I_{TEG}}{t_{OFFx}} = \frac{I_{TEG}}{t_{OFFy}} = \frac{I_{TEG}}{t_{OFF} - t_{OFFx}}; \tag{A.3}$$

thus

$$t_{ONy} = t_{ON}\left(1 - \frac{LI_{OUT}}{V_{IN}t_{ON}}\right), \tag{A.4}$$

$$t_{OFFx} = t_{OFF}\left(1 - \frac{LI_{OUT}}{V_{IN}t_{ON}}\right). \tag{A.5}$$

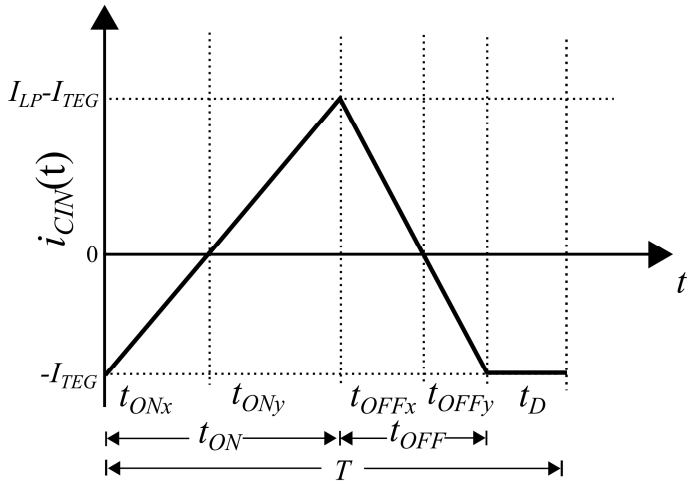


Figure 73 - Input capacitor current and time constants.

It is then possible to calculate the input ripple using the current–voltage relation at the input capacitor, given by

$$\Delta V_{IN} = \frac{1}{C_{IN}}\left[\int_{t_{ONx}}^{t_{ON}} i_{CIN}dt + \int_{t_{ON}}^{t_{ON}+t_{OFFx}} i_{CIN}dt\right] \quad (A.6)$$

$$= \frac{1}{C_{IN}}\left[\frac{1}{2}\left(\frac{V_{IN}t_{ON}}{L} - MI_{OUT}\right)\left(t_{ONy} + t_{OFFx}\right)\right]. \quad (A.7)$$

Replacing (A.4), (A.5), (2.17) and (2.20) in (A.7), we have an expression for the input ripple

$$\Delta V_{IN} = \frac{V_{IN}}{2C_{IN}Lf_{SW}{}^2}\left[D\left(D+D'\right)\left(1-\frac{D+D'}{2}\right)\left(1-\frac{D'}{2}\right)\right]. \quad (A.8)$$

Assuming the converter operating under high gain, (A.8) can be rewritten as

$$\Delta V_{IN} = \frac{V_{IN}D^2}{2C_{IN}Lf_{SW}{}^2}\left(1-\frac{D}{2}\right). \quad (A.9)$$

Thus, the proportional input ripple under high gain operation and the input capacitor, respectively, are given by

$$\frac{\Delta V_{IN}}{V_{IN}} = \frac{D^2}{2C_{IN}Lf_{SW}{}^2}\left(1-\frac{D}{2}\right). \quad (A.10)$$

$$C_{IN} = \frac{D^2}{2Lf_{SW}{}^2\dfrac{\Delta V_{IN}}{V_{IN}}}\left(1-\frac{D}{2}\right). \quad (A.11)$$

Using (A.11), it is possible to define the value of C_{IN} for a specified input ripple.

APPENDIX B – OUTPUT RIPPLE AND OUTPUT CAPACITOR

In order to define the value of the output ripple and capacitance, the Kirchhoff's current law is applied at the output node, leading to

$$i_{COUT}(t) = i_{HSS}(t) - I_{OUT}. \tag{B.1}$$

The time constants used in Figure 6 (b) are further divided according to Figure 74. The new time constants can be calculated by the graph, assuming the constant slope of i_{COUT} during t_{OFF}, leading to

$$\frac{\frac{V_{IN}t_{ON}}{L} - I_{OUT}}{t_{OFFa}} = \frac{I_{OUT}}{t_{OFFb}} = \frac{I_{OUT}}{t_{OFF} - t_{OFFa}}; \tag{B.2}$$

hence

$$t_{OFFa} = t_{OFF}\left(1 - \frac{LI_{OUT}}{V_{IN}t_{ON}}\right). \tag{B.3}$$

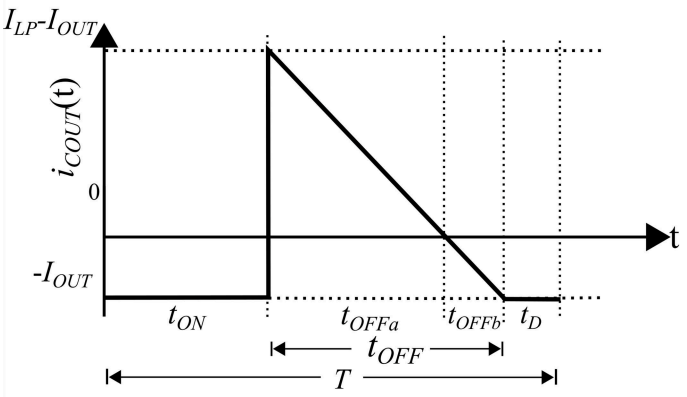


Figure 74 - Output capacitor current and time constants.

It is then possible to calculate the output ripple using the current–voltage relation at the output capacitor, given by

$$\Delta V_{OUT} = \frac{1}{C_{OUT}}\left[\int_{t_{ON}}^{t_{ON}+t_{OFFa}} i_{COUT}\,dt\right] = \frac{1}{C_{OUT}}\left[\frac{1}{2}\left(\frac{V_{IN}t_{ON}}{L} - I_{OUT}\right)t_{OFFa}\right]. \tag{B.4}$$

Replacing (B.3) and (2.17) in (B.4), we have

$$\Delta V_{OUT} = \frac{V_{IN}}{2LC_{OUT}f_{SW}^{\,2}}\left[DD'\left(1 - \frac{D'}{2}\right)^2\right]. \tag{B.5}$$

Under high gain operation, this expression reduces to

$$\Delta V_{OUT} = \frac{V_{IN}}{2C_{OUT}Lf_{SW}{}^2}\frac{D^2}{M}. \tag{B.6}$$

The proportional output ripple under high-gain operation and the output capacitor, respectively, are given by

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{1}{2C_{OUT}Lf_{SW}{}^2}\left(\frac{D}{M}\right)^2, \tag{B.7}$$

$$C_{OUT} = \frac{1}{2Lf_{SW}{}^2}\frac{\Delta V_{OUT}}{V_{OUT}}\left(\frac{D}{M}\right)^2. \tag{B.8}$$

Using (B.8), it is possible to define the value of C_{OUT} for a specified output ripple, where M is set for the worst case scenario (lower M, or maximum V_{IN}).

APPENDIX C – MOSFET SHEET RESISTANCE (ON STATE)

When the LSS is conducting, the transistor operates in strong inversion; hence, the drain current can be expressed as [54]

$$I_D = \mu_{n(p)} n C_{OX} \frac{W_{n(p)}}{2.L_{n(p)}} \left[\left(V_P - V_S \right)^2 - \left(V_P - V_D \right)^2 \right]. \tag{C.1}$$

where V_P is the pinch-off voltage. Since V_{DS} is low, the LSS sheet resistance can be given by

$$R_{S,LSS} = \left(\frac{dI_D}{dV_D} \right)^{-1} . \frac{W_{LSS}}{L_{LSS}} \approx \frac{1}{\mu_n C_{OX} \left(V_{GN} - V_{TON} - nV_D \right)}. \tag{C.2}$$

Since V_{GN}-V_{TON}>>nV_D, we approximate (C.2) by

$$R_{S,LSS} \approx \frac{1}{\mu_n C_{OX} \left(V_{GN} - V_{TON} \right)}. \tag{C.3}$$

An equivalent procedure is used for the HSS, leading to

$$R_{S,HSS} \approx \frac{1}{\mu_p C_{OX} \left(V_{OUT} - \left| V_{TOP} \right| - V_{GP} \right)}. \tag{C.4}$$

APPENDIX D – ANALYTICAL EXPRESSION FOR t_{SP0}

The time response after the opening of PM_1 is analyzed using the equivalent circuit shown in Figure 53 for $i_L(0)=0$. Applying the Kirchhoff's current law at node M yields

$$i_L(t) - i_C(t) - i_{RNM1C}(t) - i_{RPM1}(t) = 0\,. \tag{D.1}$$

$$\frac{d^2 v_M(t)}{dt^2} + \frac{dv_M(t)}{dt}\left[\frac{1}{C\left(R_{LSS}\,//\,R_{HSS}\right)}\right] + \frac{1}{LC_{MPAR}}\left(v_M(t)\right) = \frac{V_{IN}}{LC_{MPAR}}\,. \tag{D.2}$$

To evaluate the type of damping that occurs after the opening of PM_1 [65], we measure the values of the switches resistance and C_{MPAR}. Using the test bench shown in Figure 75, the DC transfer simulation was performed to measure the switches resistance versus v_M, which was swept from -0.3 to 1.3 V, as shown in Figure 76. When v_M shifts from V_{OUT} to $V_{OUT}/2$, the resistance of the three switches, which are in parallel in this analysis, ranges from 55 to 100 kΩ, as can be seen in Figure 76.

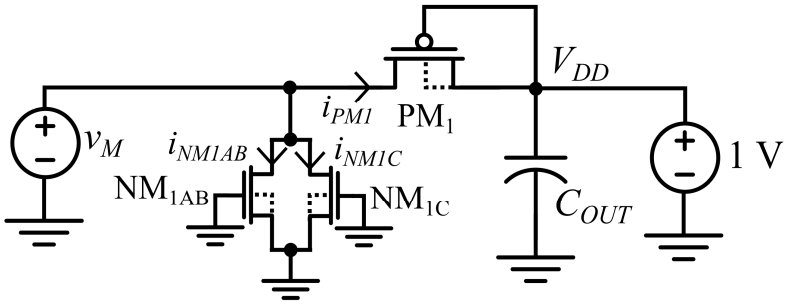


Figure 75 - Test bench used for measuring the switches resistance with regard to v_M.

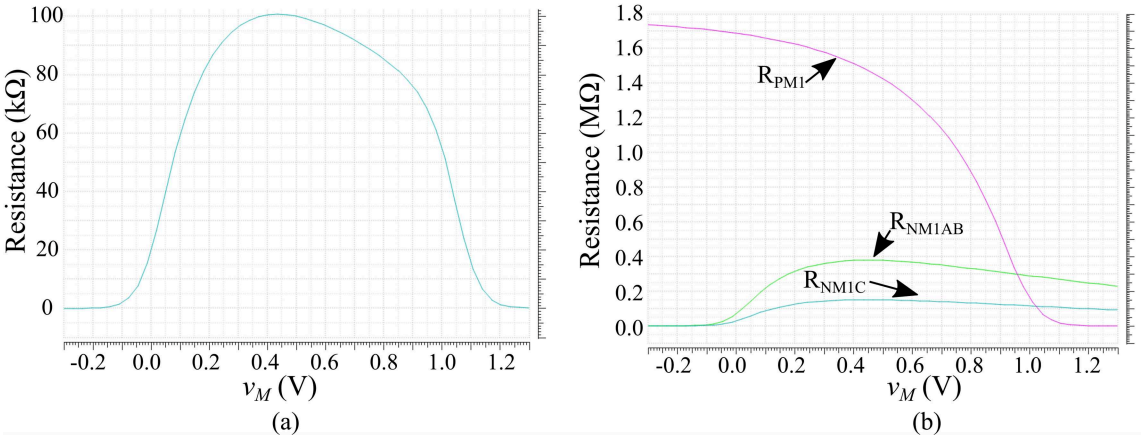


Figure 76 - (a) The total parallel resistance and (b) the individual switches resistance.

To evaluate C_{MPAR}, the post-layout circuit of Figure 77 was simulated. A pulse signal was applied to node M with a known series resistance R_M=1 kΩ, and the v_M rising waveform was measured, as shown in Figure 78. Thus, C_{MPAR} can be evaluated knowing that

$$C_{MPAR} = \frac{\Delta t_R}{R_M}, \tag{D.3}$$

where Δt_R is the time needed for v_M to shift from 0 V to 0.632xV_{DD}. Using Figure 78, the measured C_{MPAR} of the post-layout simulation is 4.6 pF.

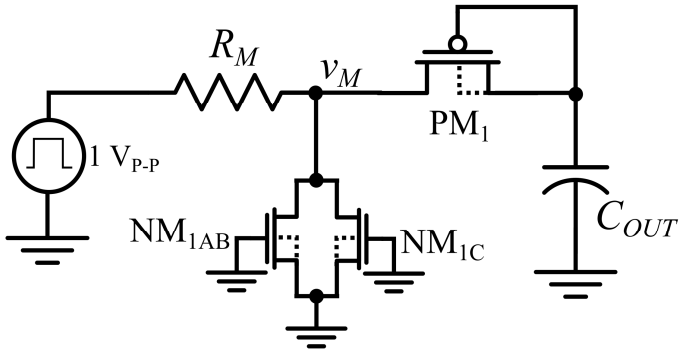


Figure 77 - Test bench used for measuring C_{MPAR}.

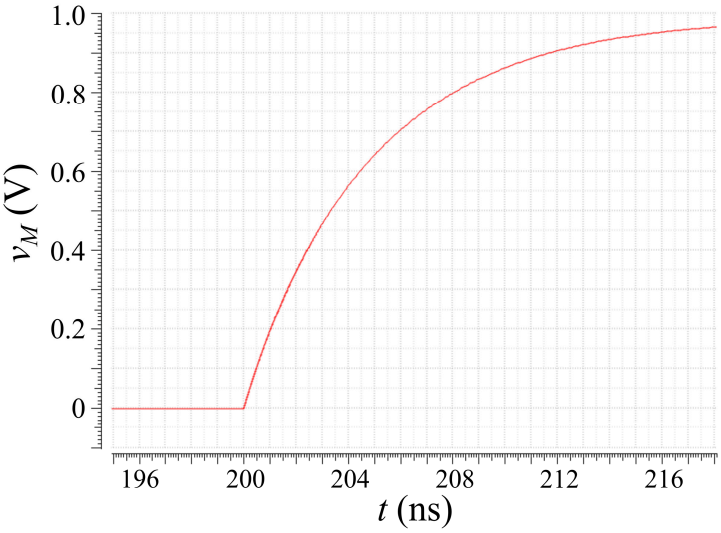


Figure 78 - Signal measured at node M.

For the highest value of boost inductance considered in this research (L=220 uH for R_{TEG}=40 Ω), the measured values of C_{MPAR}=4.6 pF and R_{LSS} //R_{HSS} ranging from 55 to 100 kΩ, when v_M ranges from V_{OUT} to V_{OUT}/2, we have

$$\omega_0 = \frac{1}{\sqrt{LC_{MPAR}}} = 3.14x10^7 , \tag{D.4}$$

$$\alpha = \frac{1}{2RC} \rightarrow 1.09x10^6 \le \alpha \le 1.97x10^6 . \tag{D.5}$$

Hence, for the whole range of switches resistance and boost inductance, we have a highly underdamped system, since $\omega_0 >> \alpha$, thus

$$\omega_D = \sqrt{\omega_0^2 - \alpha^2} \approx \omega_0 . \tag{D.6}$$

For the underdamped system, the time response follows the expression

$$v_M(t) = V_{IN} + \left(B_1 \cos(\omega_D t) + B_2 \sin(\omega_D t)\right) e^{-\alpha t} . \tag{D.7}$$

Since for t=0, v_M=V_{OUT}, then

$$B_1 = V_{OUT} - V_{IN} . \tag{D.8}$$

To find the value of B_2, we use the derivative

$$\frac{i_C(t)}{C_{MPAR}} = \frac{dv_M(t)}{dt} \tag{D.9}$$

$$= e^{-\alpha t} \left\{ \left[-B_1 \sin(\omega_D t) + B_2 \cos(\omega_D t) \right] \omega_D - \alpha \left[B_1 \cos(\omega_D t) + B_2 \sin(\omega_D t) \right] \right\} . \tag{D.10}$$

Therefore, for t=0 we have

$$B_2 \approx \frac{V_{OUT}\left[\alpha R_{LSS} C_{MPAR} - 1\right] + i_L(0) R_{LSS}}{\omega_D R_{LSS} C_{MPAR}} . \tag{D.11}$$

Since $V_{IN} << V_{OUT}$, $\omega_D >> \alpha$, and $B_2 << B_1$ for $i_L(0)$=0 , we approximate (D.7) as

$$v_M(t) = B_1 \cos(\omega_D t) . \tag{D.12}$$

Thus, assuming that at the switching point (t=t_{SP0}), v_M is equal to V_{OUT}/2, using (D.12) we have

$$t_{SP0} = \sqrt{LC_{MPAR}} \arccos 0.5 \approx 1.05\sqrt{LC_{MPAR}} . \tag{D.13}$$

APPENDIX E – DERIVATION OF THE OUTPUT VOLTAGE AND INPUT RESISTANCE OF THE CROSS-COUPLED RECTIFIER

Figure 79 shows a single stage of the cross-coupled rectifier, where M_1=M_2 and M_3=M_4.

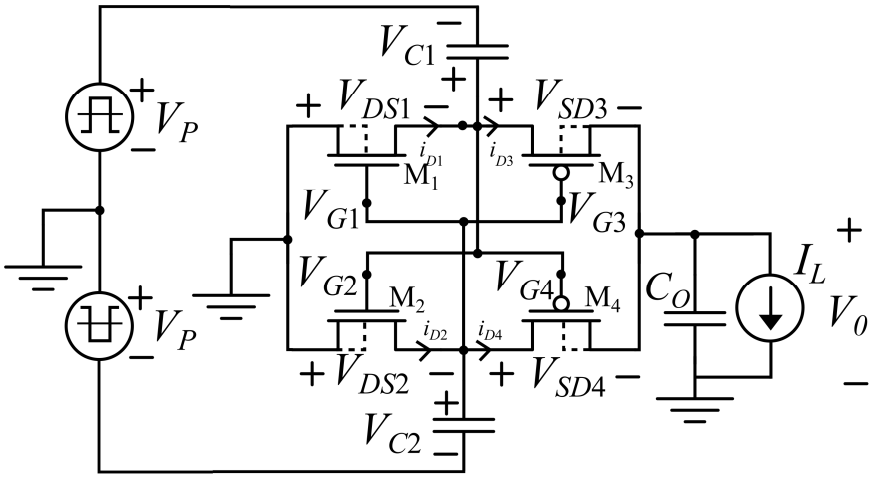


Figure 79 - A single stage of the cross-coupled rectifier

In steady state, the mean current on the capacitors is zero and the sum of the mean drain current on both transistors is I_L, thus

$$\overline{i_{D1}} = \overline{i_{D2}} = \overline{i_{D3}} = \overline{i_{D4}} = \frac{I_L}{2}. \tag{E.1}$$

Assuming the device operation in weak inversion and n≈1, the drain current of the NMOS and PMOS transistors can be approximated by [54]

$$I_{D,N(P)} \approx \mu_{n(p)} \frac{W_{N(P)}}{L_{N(P)}} nC_{OX}\phi_t^2 e^1 e^{\frac{-V_{TON(P)}}{n\phi_t}} e^{\frac{V_{GS(SG)}}{n\phi_t}} \left(1 - e^{-\left(\frac{V_{DS(SD)}}{\phi_t}\right)}\right) \tag{E.2}$$

In order to simplify the analysis, we assume that the n-channel and p-channel transistors are sized in such way that

$$\mu_n \frac{W_N}{L_N} nC_{OX}\phi_t^2 e^1 e^{\frac{-V_{TON}}{n\phi_t}} = \mu_p \frac{W_P}{L_P} nC_{OX}\phi_t^2 e^1 e^{\frac{V_{TOP}}{n\phi_t}} = I_{SEQ}. \tag{E.3}$$

We assume the transistors are on for positive V_{GS} (V_{SG}) and off for negative V_{GS} (V_{SG}), for n(p)-channel transistors. Hence, when the transistors are on and off, respectively, we have the following conditions

$$V_{DS1,ON} = V_{DS2,ON} = V_{SD3,ON} = V_{SD4,ON}, \tag{E.4}$$

$$V_{DS1,OFF} = V_{DS2,OFF} = V_{SD3,OFF} = V_{SD4,OFF}. \tag{E.5}$$

Assuming that the input capacitors are sized so that V_{C1} and V_{C2} have a negligible AC component, we apply the Kirchhoff's voltage law at the rectifier circuit, yielding

$$-2V_P - V_{DS1,OFF} + V_{DS1,ON} = 0 \tag{E.6}$$

$$V_{DS1,OFF} + V_{SD3,ON} + V_0 = 0 \tag{E.7}$$

Hence, using (E.4) through (E.7), we have

$$V_{DS1,OFF} = -V_P - \frac{V_0}{2}, \tag{E.8}$$

$$V_{DS1,ON} = V_P - \frac{V_0}{2}. \tag{E.9}$$

Using (E.1), (E.2), (E.8) and (E.9), we now have

$$i_L = i_{D1,ON} + i_{D1,OFF} = I_{SEQ}\left(e^{\left(\frac{2V_P}{n\phi_t}\right)} + e^{\left(\frac{-2V_P}{n\phi_t}\right)} - e^{\left(\frac{2V_P}{n\phi_t}\right)} e^{\frac{-V_{DS1ON}}{\phi_t}} - e^{\left(\frac{-2V_P}{n\phi_t}\right)} e^{\frac{-V_{DS1OFF}}{\phi_t}} \right) \tag{E.10}$$

$$= I_{SEQ}\left(2\cosh\left(\frac{2V_P}{n\phi_t}\right) - e^{\frac{V_0}{2\phi_t}} 2\cosh\left(\frac{(2-n)V_P}{n\phi_t}\right)\right); \tag{E.11}$$

thus

$$e^{\frac{V_0}{2\phi_t}} = \frac{\cosh\left(\frac{2V_P}{n\phi_t}\right) - \frac{i_L}{2I_{SEQ}}}{\left(\cosh\left(\frac{(2-n)V_P}{n\phi_t}\right)\right)}. \tag{E.12}$$

Hence, the output voltage of a single stage rectifier can be written as

$$V_0 = 2\phi_t \ln \frac{\cosh\left(\frac{2V_P}{n\phi_t}\right) - \frac{i_L}{2I_{SEQ}}}{\cosh\left(\frac{(2-n)V_P}{n\phi_t}\right)}, \tag{E.13}$$

and the output of an N-stage rectifier can be given by

$$V_0 = 2N\phi_t \ln \frac{\cosh\left(\frac{2V_P}{n\phi_t}\right) - \frac{i_L}{2I_{SEQ}}}{\cosh\left(\frac{(2-n)V_P}{n\phi_t}\right)}. \tag{E.14}$$

The static losses in a single stage can be reduced to

$$P_{SLOSS} = 2\left(V_{DS1,ON} i_{D1,ON} + V_{DS1,OFF} i_{D1,OFF}\right). \tag{E.15}$$

$$= 2I_{SEQ}\left(\begin{array}{l} e^{\left(\frac{V_0}{2\phi_t}\right)}\left[V_0 \cosh\left(\frac{(2-n)V_P}{n\phi_t}\right) - 2V_P \sinh\left(\frac{(2-n)V_P}{n\phi_t}\right)\right] \\ +\left[2V_P \sinh\left(\frac{2V_P}{n\phi_t}\right) - V_0 \cosh\left(\frac{2V_P}{n\phi_t}\right)\right] \end{array} \right). \tag{E.16}$$

Using (E.12), we write (E.16) as

$$P_{SLOSS} = \left[i_L - 2I_{SEQ}\cosh\left(\frac{2V_P}{n\phi_t}\right)\right] 2V_P \tanh\left(\frac{(2-n)V_P}{n\phi_t}\right) + 4I_{SEQ}V_P \sinh\left(\frac{2V_P}{n\phi_t}\right) - V_0 i_L. \tag{E.17}$$

For an N-stage rectifier, we have

$$P_{SLOSS} = N\left[i_L - 2I_{SEQ}\cosh\left(\frac{2V_P}{n\phi_t}\right)\right]2V_P\tanh\left(\frac{(2-n)V_P}{n\phi_t}\right) + 4NI_{SEQ}V_P\sinh\left(\frac{2V_P}{n\phi_t}\right) - V_0 i_L \qquad \text{(E.18)}$$

The input resistance seen from each of the input nodes to the ground, for a N-stage rectifier can be given by

$$R_{IN} = \frac{V_P^2}{P_{IN}} = \frac{V_P^2}{\frac{P_{OUT} + P_{LOSS}}{2}} \qquad \text{(E.19)}$$

$$= \frac{V_P}{N\left\{\left(i_L - 2I_{SEQ}\cosh\left(\frac{2V_P}{n\phi_t}\right)\right)\tanh\left(\frac{(2-n)V_P}{n\phi_t}\right) + 2I_{SEQ}\sinh\left(\frac{2V_P}{n\phi_t}\right)\right\}}. \qquad \text{(E.20)}$$

Using the equivalence between sinusoidal and square-wave signals described in [58], for sinusoidal signals, we have

$$V_0 = 2N\varphi_t \ln\frac{I_0\left(\frac{2V_A}{n\phi_t}\right) - \frac{i_L}{2I_{SEQ}}}{I_0\left(\frac{(2-n)V_A}{n\phi_t}\right)}, \qquad \text{(E.21)}$$

$$R_{IN} = \frac{V_A}{2N\left\{\left(i_L - 2I_{SEQ}I_0\left(\frac{2V_A}{n\phi_t}\right)\right)\frac{I_1\left(\frac{(2-n)V_A}{n\phi_t}\right)}{I_0\left(\frac{(2-n)V_A}{n\phi_t}\right)} + 2I_{SEQ}I_1\left(\frac{2V_A}{n\phi_t}\right)\right\}}. \qquad \text{(E.22)}$$

where $I_0(z)$ and $I_1(z)$ are the modified Bessel functions of the first kind of order zero and one, respectively.

APPENDIX F – PUBLICATIONS

The following papers were published during the doctoral research period:

Journal paper:

R. L. Radin, M. Sawan, C. Galup-Montoro and M. C. Schneider, "A 7.5 mV-Input Boost Converter for Thermal Energy Harvesting with 11 mV Self-Startup," in IEEE Transactions on Circuits and Systems II: Express Briefs. [66]

International conference papers:

A. K. Sinha, R. L. Radin, D. D. Caviglia, C. G. Montoro and M. C. Schneider, “An energy harvesting chip designed to extract maximum power from a TEG,” IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS), Florianopolis, 2016, pp. 367-37. [67]

S. M. Noghabaei, R. L. Radin, Y. Savaria and M. Sawan, "A High-Efficiency Ultra-Low-Power CMOS Rectifier for RF Energy Harvesting Applications," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-4. [62]

S. M. Noghabaei, R. L. Radin and M. Sawan, "Efficient Dual-band Ultra-Low-Power RF Energy Harvesting Front-End for Wearable Devices," 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), Windsor, ON, Canada, 2018, pp. 444-447. [68]

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