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Deni Germano Alves Neto

Ultra-Low-Voltage Minimalist Standard Cell Library

Florianópolis
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O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Prof. Cesar Ramos Rodrigues, Dr.
Universidade Federal de Santa Catarina

Profa. Cristina Meinhardt, Dra.
Universidade Federal de Santa Catarina

Eng. William Prodanov, Dr.
Chipus Microelectronics

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Prof. Carlos Galup-Montoro, Dr.
Orientador

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Este trabalho é dedicado aos meus queridos avós.

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“What I cannot create,
I do not understand."
(Feynman, 1988)

RESUMO

A operação de ultrabaixa tensão é uma abordagem atraente para aplicações com restrição de energia, onde a frequência de operação é uma preocupação secundária. No entanto, o aumento da variabilidade dos parâmetros do processo deve ser mitigado neste domínio. Esta dissertação propõe abordagens para melhorar a robustez de circuitos integrados digitais em operação sublimiar por meio de dimensionamento de dispositivos e topologias alternativas de circuito. A fim de transcender os limites anteriores de bibliotecas de células padrão de baixa tensão, esta dissertação apresenta uma metodologia para projetar uma biblioteca de células padrão minimalista de ultra baixa tensão de 100 mV; a biblioteca consiste em células combinacionais e sequenciais. Foram utilizadas duas topologias de circuitos lógicos, o CMOS *sliced* e o *Schmitt trigger*. A biblioteca de células padrão foi validada através do projeto e teste de circuitos divisores de frequência fabricados nas tecnologias de 130 nm e 180 nm. Resultados experimentais na tecnologia de 130 nm de um divisor de frequência com 15 estágios cascateados utilizando a lógica *Schmitt trigger* demonstram a operação em 32 kHz com uma tensão de alimentação de 76 mV. Os resultados em silício da tecnologia 180 nm operam em uma tensão ainda mais baixa, um divisor de frequência baseado na topologia *sliced* opera com uma tensão de alimentação de 72 mV, com 32 kHz de frequência de entrada. Todas as dez amostras dos divisores de frequência de 180 nm são totalmente funcionais em V_{DD} =100 mV, mostrando a robustez da biblioteca de ultra baixa tensão projetada nesta dissertação.

Palavras-chave: Ultra-baixa-tensão. Sublimiar. CMOS. Schmitt Trigger. Standard cells

RESUMO EXPANDIDO

INTRODUÇÃO

Os dispositivos semicondutores são os blocos de construção essenciais da economia moderna. Todos os produtos e serviços atuais dependem fortemente de chips, desde smartphones, computadores e carros até automação industrial.

Nas últimas décadas, a computação de alto desempenho permaneceu o domínio principal da tecnologia CMOS. No entanto, outra via de pesquisa e desenvolvimento é estimulada por eletrônicos vestíveis consumíveis em massa e a já estabelecida internet das coisas. No entanto, o desafio a ser enfrentado é fornecer energia elétrica a esses dispositivos eletrônicos. Sistemas sempre ativos, como nós de sensores sem fio, dispositivos biomédicos implantáveis e redes IoT, devem fornecer funcionalidade, mantendo uma quantidade de energia limitada. Em tais aplicações, os circuitos estão espalhados por diferentes ambientes e espera-se que sejam autossuficientes em energia. A rede elétrica e baterias não são mais uma solução viável para sustentar esses sistemas devido ao custo de manutenção e substituição de componentes no esgotamento da energia. Por outro lado, a captação de energia fornece energia termoelétrica, fotovoltaica e vibracional nas proximidades do nó sensor. A operação de ultrabaixa tensão é uma abordagem atraente para aplicações com restrição de energia, onde a frequência de operação é uma preocupação secundária. No entanto, o aumento da variabilidade dos parâmetros do transistor MOS no processo de fabricação deve ser mitigado neste domínio.

OBJETIVOS

Esta dissertação propõe abordagens para melhorar a robustez de circuitos integrados digitais em operação sublimiar por meio de dimensionamento de dispositivos e topologias alternativas de circuito.

METODOLOGIA

A fim de transcender os limites anteriores de bibliotecas de células padrão de baixa tensão, esta dissertação apresenta uma metodologia para projetar uma biblioteca de células padrão minimalista de ultra baixa tensão de 100 mV; a biblioteca consiste em células combinacionais e sequenciais. Foram utilizadas duas topologias de circuitos lógicos, o CMOS *sliced* e o *Schmitt trigger*. A biblioteca de células padrão foi validada através do projeto e teste de circuitos divisores de frequência fabricados nas tecnologias de 130 nm e 180 nm.

RESULTADOS E DISCUSSÃO

Resultados experimentais na tecnologia de 130 nm de um divisor de frequência com 15 estágios cascateados utilizando a lógica *Schmitt trigger* demonstram a operação em 32 kHz com uma tensão de alimentação de 76 mV. Os resultados em silício da tecnologia 180 nm operam em uma tensão ainda mais baixa, um divisor de frequência baseado na topologia *sliced* opera com uma tensão de alimentação de 72 mV, com 32 kHz de frequência de entrada. Todas as dez amostras dos divisores de frequência de 180 nm são totalmente funcionais em V_{DD} =100 mV, mostrando a robustez da biblioteca de ultra baixa tensão projetada nesta dissertação.

CONSIDERAÇÕES FINAIS

Abordar a variabilidade na região sublimiar foi o principal desafio deste trabalho. No projeto a nível do transistor, técnicas de dimensionamento e associação de transistores foram usadas para melhorar a robustez das portas lógicas.

Duas topologias de portas lógicas foram comparadas neste trabalho, a baseada na topologia *sliced* e a baseada no inversor *Schmitt trigger*. A simulações pós-layout da biblioteca de células padrão mostrou que as células baseadas em *sliced* têm uma melhoria significativa na dissipação de potência, tempo de propagação e área.

A biblioteca de células padrão foi verificada através do projeto de divisores de frequência. O divisor de frequência foi simulado e fabricado em duas tecnologias CMOS diferentes; este circuito foi escolhido devido à vasta aplicação em relógios de tempo real. O divisor de frequência baseado na topologia *sliced* chegou a uma tensão de alimentação de 72 mV, a mais baixa para um circuito sequencial CMOS. Este resultado prova que mesmo em um campo maduro como o projeto de circuitos operando na região sublimiar, há espaço para melhorias.

Palavras-chave: Ultra-baixa-tensão. Sublimiar. CMOS. Schmitt Trigger. Células lógicas

ABSTRACT

Ultra-low-voltage operation is a compelling approach for power-constrained applications where the frequency of operation is a secondary concern. However, the increased variability of the process parameters must be mitigated in this domain. This dissertation proposes approaches to improve the robustness of digital integrated circuits in subthreshold operation through device sizing and improved circuit topologies. In order to transcend the previous limits of low voltage standard cells libraries, this dissertation presents a methodology to design an ultra-low-voltage minimalist standard cell library to operate with a supply voltage of 100 mV; the library consists of combinational and sequential cells. Two topologies of logic circuits were used, the CMOS sliced-based and the Schmitt trigger-based cells. The standard cell library was validated through the design and test of frequency dividers circuits fabricated in 130 nm and 180 nm technologies. Experimental results on the 130 nm tech of a 15-stage Schmitt trigger-based frequency divider chain demonstrate the operation at 32 kHz with a supply voltage of 76 mV. The 180 nm silicon results operate in an even more extreme low voltage, a 72 mV CMOS sliced-based frequency divider operate at 32 kHz. All ten samples of the 180 nm frequency dividers are fully functional at V_{DD} =100 mV, resulting in a 100% yield.

Keywords: Ultra-Low-Voltage. CMOS. Subthreshold. Schmitt trigger. Standard cells

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND ACRONYMS

AOI	AND-OR-INVERTER
BSIM	Berkeley Short-Channel IGFET Model
CMOS	Complementary Metal-Oxide Semiconductor
CS	Common-Source
CSIG	Common-Source Intrinsic Gain
DC	Direct Current
DFF	D-Flip-Flop
DIBL	Drain-Induced Barrier Lowering
DRC	Design Rule Check
FD	Frequency Divider
MEP	Minimum Energy Point
LVS	Layout Versus Schematic
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MVT	Medium Threshold Voltage Transistor
N	Number of Stages
NMOS	N-Channel MOS
NVT	Native Transistor
OAI	OR-AND-INVERTER
PDK	Process Design Kit
PDN	Pull-down Network
PDP	Power-Delay-Product
PMOS	P-Channel MOS
PUN	Pull-up Network
RSCE	Reverse Short-Channel Effect

ROSC	Ring Oscillator
SCL	Standard Cell Library
SVT	Standard Threshold Voltage Transistor
ST	Schmitt-Trigger
ULV	Ultra-Low-Voltage
VTC	Voltage Transfer Characteristic

LIST OF SYMBOLS

α	Activity factor
μ	Mean value
μ_n	Electron mobility
ϕ_t	Thermal voltage
σ_x	Standard deviation of x
σ	DIBL coefficient
A_V	Voltage gain
A_{V_T}	Pelgrom coefficient of the threshold voltage
C_L	Load capacitance
C_{ox}	Oxide capacitance per unit area
f_{in}	Input frequency
f_{osc}	Frequency of oscillation
f_{out}	Output frequency
f_{switch}	Switching frequency
f_T	Unity gain frequency
g_{mb}	Bulk transconductance
g_{md}	Drain transconductance
g_{ms}	Source transconductance
g_m	Gate transconductance
I_{SC}	Short-circuit current
I_D	Drain current
i_d	Normalizes drain current
I_F	Forward current
i_f	Normalized forward current (inversion level)
I_{LK}	Leakage current

$I_{N(P)}$	Transistor scale factor/transistor strength
I_R	Reverse current
i_r	Normalized reverse current
I_S	Specific current
I_2/I_1	Design factor
I_1/I_0	Design factor
L	Transistor channel length
n	Slope factor
P_{dyn}	Dynamic power
P_{stat}	Static power
P_{sc}	Short-circuit power
P_{tot}	Total power
T	Temperature
T_{sc}	Period of conduction of I_{SC}
t_p	Propagation delay
t_{pHL}	High-to-low propagation delay
t_{pLH}	Low-to-high propagation delay
V_B	Bulk voltage
$V_{DD_{min}}$	Minimum voltage supply
V_{DD}	Supply voltage
V_D	Drain voltage
V_G	Gate voltage
V_{IN}	Input voltage
V_M	Inverter threshold voltage
V_{OUT}	Output voltage
V_P	Pinch-off voltage

V_S	Source voltage
V_{T0}	Threshold voltage
W	Transistor channel width

CONTENTS

1 INTRODUCTION

Semiconductor devices are the essential building blocks of the modern economy. All current products and services rely heavily on chips, from smartphones, computers, and cars to industrial automation and defense. The global chip market was approximately $500 billion in 2021 and is expected to grow to $1 trillion by 2030 [1] as data volumes, computing power, and connectivity increase.

Over the past decades, high-performance computing remained the primary domain of complementary metal-oxide-semiconductor (CMOS) technology. Nevertheless, another avenue of research and development is stimulated by mass-consumable electronic wearables and the already established Internet-of-Things (IoT). However, the challenge to be addressed is supplying those electronic devices with electrical power. Always-on systems, such as wireless sensor nodes, implantable biomedical devices, and IoT networks, must provide functionality while maintaining a limited power budget [2]. In such applications, circuits are scattered across different environments and expected to be energy self-sufficient. Power grids and batteries are no longer a viable solution to sustain these systems due to the cost of maintenance and replacement of components upon energy depletion. On the other hand, energy harvesting provides power from thermometric, photovoltaic, and vibration in the vicinity of the sensor node, as presented in [3].

In the early years of the metal-oxide-semiconductor field-effect transistor (MOSFET), integrated circuit designers used the well-known quadratic relationship between drain current (I_D) and gate-source voltage (V_{GS}) in a saturated transistor [4], presented in Equation (1), also known as the strong inversion (SI) drain current, to determine the transistor gate geometry.

$$I_{D,SI} = \frac{\beta}{2n}(V_{GS} - V_{T0})^2 \tag{1}$$

In this simplified model of I_D, the transistor is represented by 3 parameters, the threshold voltage (V_{T0}), the slope factor n and the transconductance parameter β given by

$$\beta = \mu C_{ox}\frac{W}{L} \tag{2}$$

where μ is the carrier mobility, C_{ox} is the oxide capacitance, W the channel width and L the channel length.

The MOS transistor has increased performance and decreased power consumption over the years through the scaling down of its dimensions. Dennard's constant field scaling [5] was the predominant device scaling method used in the last four decades of Moore's Law [6]. Dennard proposed that performance improvement could be observed by scaling the minimum channel length. To mitigate the inevitable reliability problems and reduction in functional lifetime, the length of the channel and the operating voltage must also be scaled by the same factor to maintain the same electric field.

Reducing the gate-source voltage (V_{GS}) below the threshold of conduction, also known as the threshold voltage (V_{T0}), leads to an exponential relationship between the drain current and the gate-source voltage, as shown in Equation (3). The regime of operation of the MOS when $V_{GS} \leq V_{T0}$ is called the subthreshold region, also known as weak inversion (WI), studied by Swanson and Meindl in [7].

$$I_{D,WI} = I_0 e^{\frac{V_{GS}-V_{T0}}{n\phi_t}} \tag{3}$$

where ϕ_t is the thermal voltage and I_0 is the specific saturation current.

One can compare a mature MOS process of the '80s with a 00's technology node and a low voltage advanced technology 10's by taking the ratio of a transistor in strong inversion (1) operating at the supply voltage (V_{DD}), i.e., $V_{GS} = V_{DD}$ over the subthreshold current of a transistor operating at the threshold of conduction, i.e., $V_{GS} = V_{TO}$. Equation (4) shows the ratio between the strong and weak inversion drain currents.

$$\frac{I_{D,SI_{@V_{DD}}}}{I_{D,WI@V_{T0}}} = \frac{1}{2e}\left(\frac{V_{DD}-V_{T0}}{n\phi_t}\right)^2 \tag{4}$$

Table 1 shows the supply voltage, threshold voltage, and current ratio of some representative technology nodes: n $= 1$, $\phi_t = 26$ mV, the values of V_{DD} and V_{T0} were based on the work of CMOS scaling trends in [8].

Table 1 – The ratio between the strong and weak maximum currents in some representative technology nodes.

Technology decade	V_{DD} [V]	V_{T0} [V]	$\frac{I_{D,SI}}{I_{D,WI}}$
'80s	15	1	53331
00's	1.5	0.5	272
10's	0.5	0.25	17

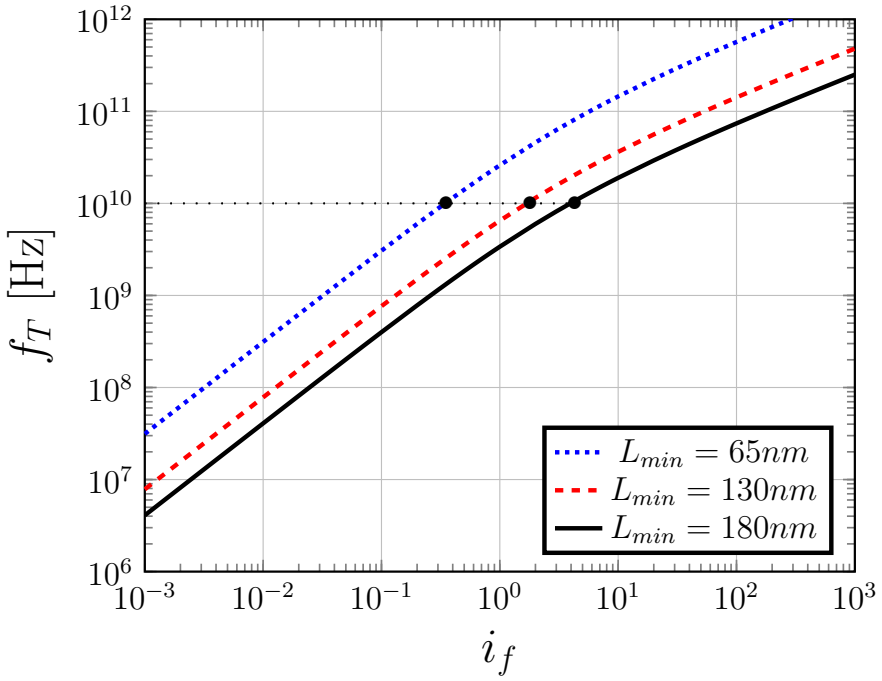
Source – The Author.

Table 1 presents a simple but effective way to observe that with the scaling process, the values of V_{DD} and V_{TO} are getting closer at each new technology; thus, the subthreshold current is becoming more relevant on the design of integrated circuits. Another way to deal with the importance of subthreshold design is to introduce the concept of inversion levels (i_f), presented in chapter 2 of [9]. For design purposes, $i_f < 1$ characterizes operation in weak inversion, while for $i_f > 100$, it is assumed operation in strong inversion. For inversion levels between 1 and 100, it is said that the transistors operate in moderate inversion (MI). Equation (5) shows the unity gain frequency (f_T) of a single transistor, i.e., the frequency at which the short-circuit current gain drops to 1 in the common-source (CS) configuration. The first-order

approximation of the unity-gain frequency is plotted for three different technology nodes in Figure 1. The schematic and formal analysis of the circuit are shown in Chapter 2 of [9].

$$f_T \approx \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right) \tag{5}$$

Figure 1 – Unity-gain frequency of an CS amplifier versus inversion level at three different technology nodes.



Source – The Author.

Figure 1 shows the impact of MOS scaling on the unity-gain frequency of the MOSFET. In the 180 nm technology, a given frequency, e.g., $f_T = 10$ GHz requires the transistor to operate in moderate inversion ($i_f \approx 6$), while for a more advanced node such as the 65 nm, the same frequency is obtained for a transistor operating in weak inversion ($i_f \approx 0.4$), which strengthens the importance of the subthreshold design as the semiconductor industry evolves. Although it was used a first-order approximation without the specific technology parameters of each node to calculate the frequency, one can observe that the frequency range (from MHz to GHz) of the subthreshold regime is appropriate for designing analog, radio-frequency and digital integrated circuits.

Up to this point, the importance of subthreshold design was discussed based on the MOS scaling. Another well-known technique, called voltage scaling also benefits from subthreshold design, this technique has been used to reduce power consumption over the last twenty years without the necessity to use an advanced technology node to design a circuit

under severe power constraints, as extensively reviewed in [10]. The critical parameter in the design space of the voltage scaling technique is the supply voltage.

Considering digital CMOS circuit design, the supply voltage has a quadratic relationship with the dynamic power. i.e., $P_{dyn} \propto V_{DD}^2$ and a linear dependency with the idle power, i.e., $P_{idle} \propto V_{DD}$. Therefore, to achieve the minimum power consumption (P_{min}), a circuit must operate at the minimum supply voltage (V_{DDmin}). As it was investigated by Calhoun et al. [11], there is a minimum energy point (MEP) of operation, near $V_{DD} \approx$ 200 mV - 300 mV, that depends on both the application and the technology. This optimal point of energy occurs for an optimum balance between dynamic and leakage energy.

Systems operating at the MEP may satisfy the demands of power constraint applications; however, depending on the circuit switching activity, power consumption in the idle state can be a significant or even the dominant part of the entire power consumption, as pointed out in [2]. Thus, a digital system being operational near the supply voltages given by energy harvesting sources, e.g., of the order of 100 mV or even lower, as showed in [12] - [13], will be vital to the wireless sensor nodes and implantable devices [13].

The region of operation for $V_{DD} \leq$ 200 mV will be called the ultra-low-voltage (ULV) domain in this work. Although the applications of ULV circuits are recent [14] - [15], we can go back to 1972 when the study of an inverter operating in the subthreshold region was pioneered by Swanson and Meindl [7]. Due to the limitations of the technology of the early 1970s, they estimate that the minimum supply voltage was around $8\phi_t$ or 200 mV at 300K. Later in 2000, Meindl and Davis [16] derived the fundamental limit of operation of an inverter in CMOS technology, which is 36 mV at 300K. One year later, in 2001, Bryant et al. designed a CMOS inverter operating at $V_{DD}=$ 100 mV in [17]. In 2018 Melek et al. [18] derived the fundamental limit of operation of an Schmitt trigger inverter, which is 31.5 mV at 300K. The interest in the ULV domain keeps on, as demonstrated in recent papers [19] - [20], which can be applied to the design of the fundamental blocks of digital integrated systems: the standard cells, as shown in [21].

A standard cell is a network of transistors and interconnections arranged in a particular pattern to yield a Boolean logic function, e.g., NOT, AND, OR, NAND, NOR. The synthesis of the desired digital circuit is done by translating the behavioral language into the netlist created with the standard cell. A minimalist number of cells (NOT, NAND or NOR) can implement any digital system due to the universal propriety of these gates. A standard cell library (SCL) is a collection of cells designed in a standard way, e.g., with one of its dimensions fixed, specific supply voltage (V_{DD}), and process technology, such as a brick in civil engineering.

Until now, the necessity and advantage of ULV design are mentioned for the feasibility of batteryless systems with extremely low power consumption. However, there is a significant problem in the subthreshold design: the impact of process variations in the ULV design [22]. The drain current of the metal-oxide-semiconductor field-effect transistor (MOSFET) in the subthreshold region has an exponential dependence on the threshold voltage V_{TO} [9]. V_{TO}

depends on technology, aspect ratio, temperature, and process. Due to the exponential behavior, any minor shift in the threshold voltage significantly impacts the drain current; thus, increases the variability in the delay and power consumption of the digital circuit, as presented by Vittoz in chapter 16 of [23].

This work proposes designing and implementing an ultra-low-voltage minimalist standard cell library using a commercial 180 nm CMOS technology while addressing the process variation issue with transistor-level design.

1.1 OBJECTIVES

Driven by the opportunities and challenges in the ULV domain, this research aims to investigate a minimalist SCL, which consists of a basic set of combinational logic gates: NOT, NAND, NOR, AOI, OAI, and a sequential logic gate: a D-Flip-flop, operating in the subthreshold region.

The specific objectives of this work are:

- Design and implementation of a minimalist standard cell library operating at the supply voltage V_{DD}= 100 mV while maintaining the robustness of the logic circuits.
- Investigate the minimum supply voltage of a frequency divider designed with the custom SCL.
- Investigate the yield and the maximum frequency of a frequency divider operating at 100 mV.

1.2 WORK ORGANIZATION

The overall structure of this dissertation takes the form of five chapters, including this introductory chapter. Chapter 2 briefly introduces the basis of transistor-level design. The third chapter presents a methodology to develop the standard cell library. Chapter 4 evaluates the ultra-low-voltage minimalist standard cell library using frequency dividers as a testbench. Finally, chapter 5 concludes with a brief state-of-the-art summary, findings, and future research.

2 TRANSISTOR LEVEL DESIGN

An intuitive, easy-to-use MOSFET model is essential for designing integrated circuits. In this work, we are confined to the subthreshold region of the MOS transistor; thus, in this chapter, we will briefly overview the behavior of the MOSFET in the ULV domain and the significant parameters of the model. Also, this chapter will briefly review the traditional CMOS inverter and the Schmitt trigger, which are the essential components of the standard cell library.

2.1 MOSFET MODELING

Although BSIM [24] -[25] has been vastly used as the primary MOSFET model to simulate MOS circuits in EDA tools, the complexity of its calculations and numerous parameters opens a gap between circuit simulation and hand-design [26] - [27], complicating the understanding of how the main MOSFET parameters relate to the simulation results. Therefore, incorporating inversion charge-based models based on physics in the simulators simplifies the action of design

In the fast-expanding ultra-low-voltage domain [20], some short-channel effects, such as velocity saturation, are not relevant; thus, a simplified MOSFET model can be satisfactory for circuit design. Targeting the ultra-low-voltage designs, this work uses a 4-parameter model (4PM) [28] - [29] based on the all-region Advanced Compact MOSFET model (ACM) [30]-[31].

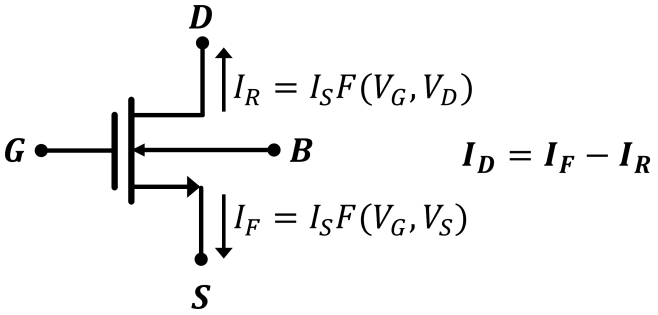
2.1.1 The 4-parameter model

The Advanced Compact MOSFET model describes the electrical behavior of MOS transistors in all regions of operation.

The three main parameters of the ACM model are the specific current I_S, the threshold voltage V_{T0}, and the slope factor n. Though these three parameters are usually enough to design a large set of circuits, a secondary effect called the drain-induced barrier lowering (DIBL) [32] completes the 4-parameter model. Despite being a very pronounced effect for short-channel transistors, the DIBL is also relevant for long-channel transistors in weak inversion. For long channel transistors in strong inversion (out of the scope of this work), DIBL is overshadowed by channel length modulation.

Figure 2 presents the symbol of an N-channel MOSFET (NMOS) transistor and its four terminals: gate (G), source (S), drain (D), and bulk (B). In this work, the bulk terminal is always grounded for the NMOS transistor and tied to V_{DD} for the PMOS transistor. For this reason, the bulk terminal will be omitted in the main text of this dissertation.

Figure 2 – Symbol of the NMOS transistor.



Source – The Author.

In the ACM model, the drain current I_D can be written as the difference between the forward (I_F) and reverse (I_R) currents, both dependent on the voltage V_{GB}, as illustrated in Figure 2. I_F is also dependent on V_{SB} , while I_R is dependent on V_{DB}. Equation (6) shows the MOS source-drain symmetry.

$$I_D = I_F - I_R = I_S\ (i_f - i_r\ ) \tag{6}$$

The specific (or normalization) current I_S is dependent on both geometry and technological parameters as given by (7), where μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage, n is the slope factor, W is the width and L is the length of the transistor channel.

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{7}$$

The normalized form of the unified current-control model (UICM), expressed in Equation (8), establishes the relationship between the terminal voltages and the forward (reverse) inversion levels $i_{f(r)}$. As a rule of thumb [9], the transistor operates in weak inversion (WI) up to $i_f = 1$ and in strong inversion (SI) for $i_f > 100$. The intermediate values of i_f, from 1 to 100, characterize moderate inversion (MI).

$$I_{F(R)} = I_S F\left[\frac{V_P - V_{S(D)}}{\phi_t}\right] \tag{8a}$$

$$F^{-1} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{8b}$$

An useful approximation of the pinch-off voltage V_P is given by Equation (9), where V_{T0} is the equilibrium threshold voltage that corresponds to the gate voltage for which $V_P = 0$

and σ is the magnitude of the DIBL coefficient. In the 4PM model, the DIBL effect comply with the MOSFET symmetry.

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \tag{9}$$

2.1.2 Subthreshold operation

In the ULV domain, the MOSFET operates in the subthreshold regime only ($i_{f(r)} \ll 1$). Thus, Equation (8) simplifies to Equation (10), which has an exponential relationship between the control voltages and the forward (reverse) inversion levels.

$$i_{f(r)} = 2e^{\frac{V_P - V_{S(D)}}{\phi_t} + 1} \tag{10}$$

Using Equations (6) and (10), one can express the well-known drain current of the MOS in the subthreshold region (11).

$$I_{DN(P)} = I_{N(P)} e^{\frac{V_{GB(BG)} + \sigma\left(V_{DB(BD)} + V_{SB(BS)}\right)}{n_{N(P)}\phi_t}} \left(e^{\frac{-V_{SB(BS)}}{\phi_t}} - e^{\frac{-V_{DB(BD)}}{\phi_t}} \right) \tag{11a}$$

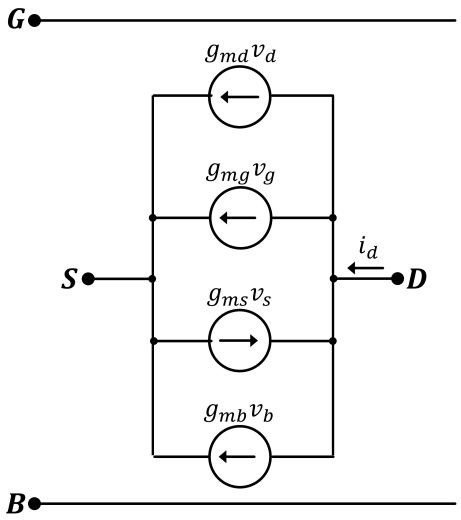
$$I_{N(P)} = 2I_{SN(P)} e^{\frac{-\left|V_{TON(P)}\right|}{n_{N(P)}\phi_t} + 1} = I_{ON(P)} e^{\frac{-\left|V_{TON(P)}\right|}{n_{N(P)}\phi_t}} \tag{11b}$$

The current scaling factor $I_{N(P)}$ represents the strength of the device, which depends on the main technological parameters and the dimensions of the transistors.

2.1.3 Small-Signal Transconductances

The small-signal transconductances are essential for both the design of integrated circuits and the extraction of the four transistor parameters [29]. As the MOSFET transistor is a 4-terminal device, Figure 3 presents the low-frequency small-signal model for the MOSFET, in which the voltage variation in each of its terminals will contribute to the variation of the drain current (I_D).

Figure 3 – Low-frequency small-signal model of the MOSFET.



Source – The Author.

The differentiation of the drain current I_D with respect to V_G, V_S, and V_D gives us the small-signal transconductances g_{mg}, g_{ms}, and g_{md} respectively, as shown in (12).

$$g_{mg} = \frac{\partial I_D}{\partial V_G}; g_{ms} = -\frac{\partial I_D}{\partial V_S}; g_{md} = \frac{\partial I_D}{\partial V_D}; g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{12}$$

If we take the particular case where all the terminals of a MOSFET increase the voltage by the same amount, the change in I_D would be 0, as shown in (13).

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0 \tag{13}$$

The vital relationships to design integrated circuits are the transconductance-to-current ratios. Applying the partial derivatives of (12) to the 4-parameter UICM (8), we have the relationship between the transconductances and the inversion levels. The thorough expressions of the transconductances and transconductance-to-current ratios are investigated in [29]. In this work, we will use two fundamental relationships to extract the four parameters of the model, the gate transconductance-to-current ratio (14) and the ratio of the gate to the drain transconductance in saturation (15). Annex A presents the parameter extraction method.

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t(\sqrt{1+i_f} + \sqrt{1+i_r})} \tag{14}$$

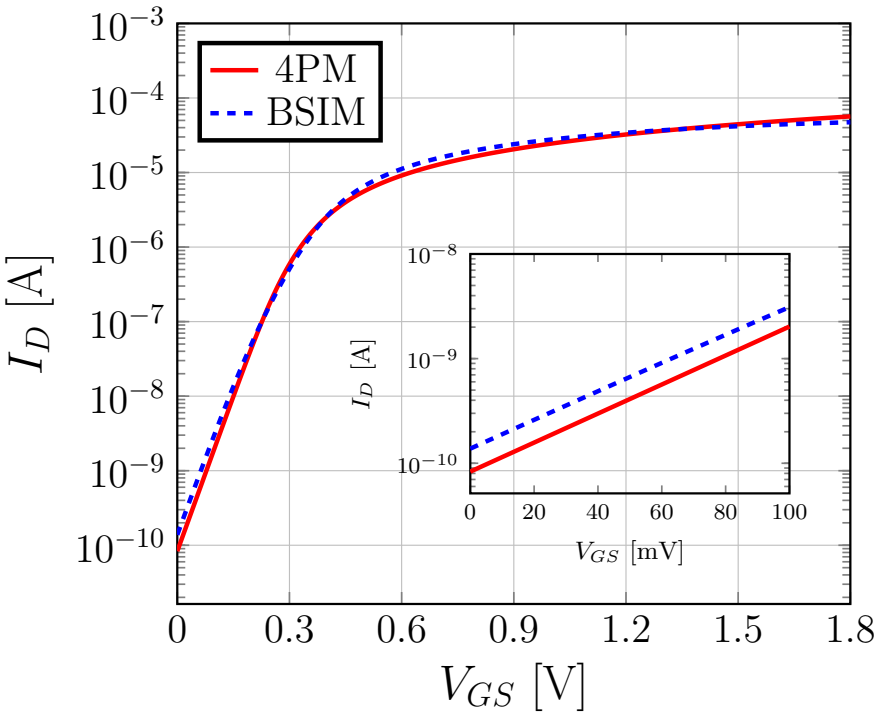
$$\frac{g_m}{g_{md}} = \frac{1}{\sigma} \tag{15}$$

2.1.4 4PM vs BSIM

This section will present a brief overview of the two most significant IV curves of the MOS transistor with a comparison of the 4PM and the BSIM model. The fully detailed implementation and comparison between the models have been carried out in [29].

Figure 4 presents the I_D vs V_{GS} at V_{DS} = 100 mV. Overall, this IV characteristic resulted in a 4PM curve close to BSIM's curve throughout the V_{GS} range. In the zoom from 0 to 100 mV, one can see the difference in the drain current between the models.

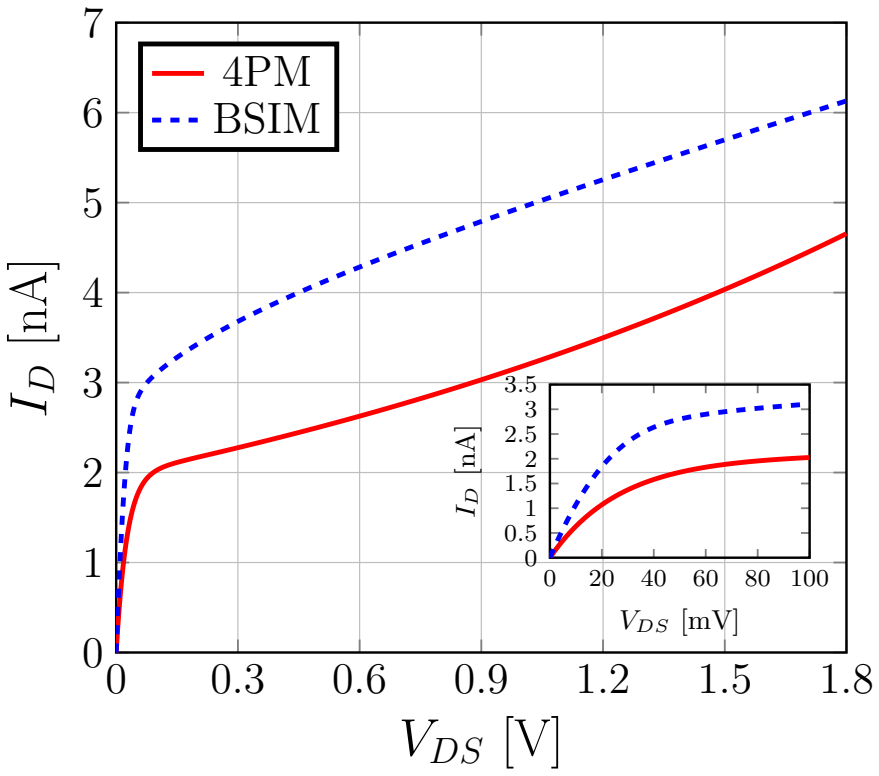
Figure 4 – I_D x V_{GS} @ V_{DS}= 100 mV of an NMOS transistor, BSIM vs 4PM.



Source – The Author.

The I_D vs V_{DS} at V_{GS} = 100 mV characteristic was also simulated, as shown in Figure 5. One can see difference between the model's curves, mainly because only one short-channel effect (DIBL) is included in the 4-parameter model.

Figure 5 – I_D x V_{DS} @ V_{GS}= 100 mV of an NMOS transistor, BSIM vs 4PM.



Source – The Author.

Indeed, the 4PM model is far less complicated than the BSIM4.5 model [33],with only four parameters (n,V_{TO}, I_S and σ) as shown in (8). In this work, we will use the 4PM model implemented in [29] and compare some simulations on Cadence Virtuoso© with those obtained with the BSIM 4.5 model available on the process design kit (PDK) of the 180 nm technology node.

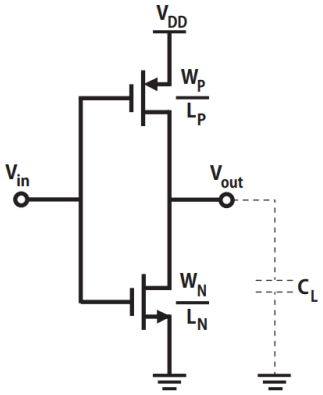
2.2 THE ULV INVERTER

The CMOS inverter, shown in Figure 6, is the fundamental building block of any digital system [34], the analysis of CMOS inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, AOI, or OAI. Despite being well-known, we will briefly overview in this section the characteristics of the classical CMOS inverter in the ULV domain.

2.2.1 Voltage transfer characteristic

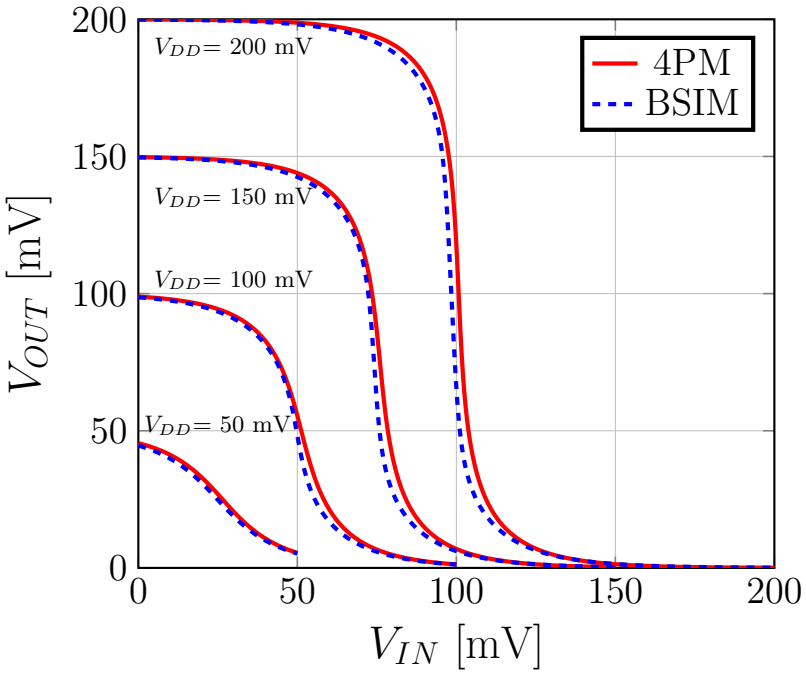
The essential characteristic of the CMOS inverter is its regenerative property that leads to well-defined logic levels, even in the ULV domain [16], operating at a supply voltage of 100 mV, as shown in Figure 7.

Figure 6 – CMOS Inverter with a equivalent load capacitance C_L.



Source – The Author.

Figure 7 – Voltage transfer characteristic of the CMOS inverter for different values of supply voltages.



Source – The Author.

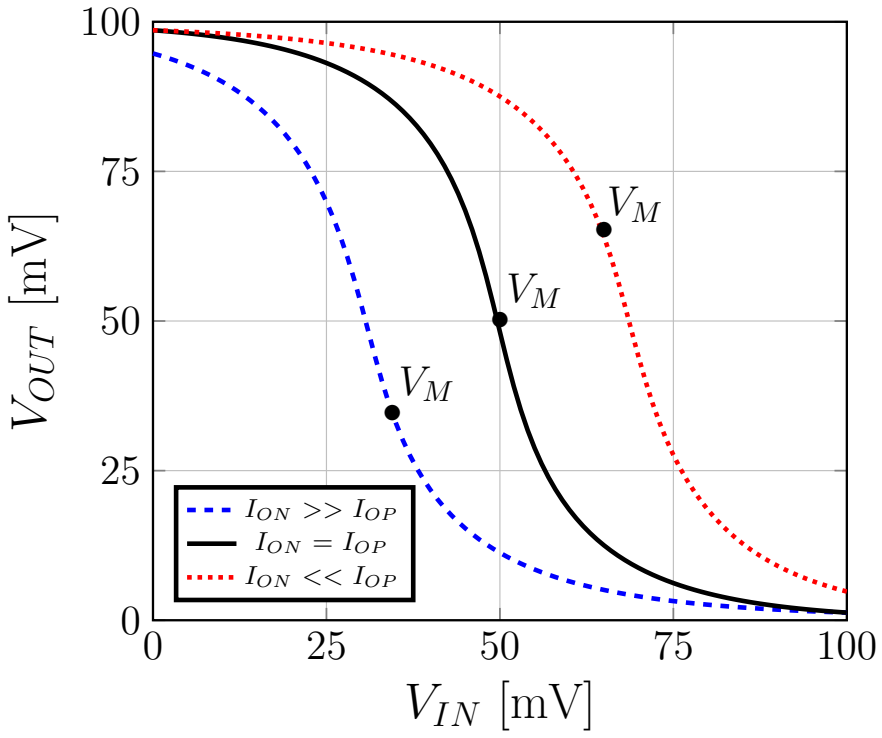
The analysis of the voltage transfer characteristic (VTC) of the CMOS inverter conducted in [35] points out that the inverter threshold voltage (V_M), defined as the voltage such that $V_{IN} = V_{OUT}$, shows dependence on the supply voltage, on technological parameters,

and on transistors strength ratios, as shown in Equation (16).

$$V_M \approx \frac{V_{DD}}{2} + \frac{\frac{V_{TON}-V_{TOP}}{2} + \frac{n\phi_t}{2} ln\left(\frac{I_{OP}}{I_{ON}}\right)}{1 + \frac{e^{\frac{V_{DD}}{2\phi_t}}-1}{n}} \tag{16}$$

If the PMOS transistor is stronger than the NMOS transistor, then $V_M > \frac{V_{DD}}{2}$ and, if the NMOS transistor is stronger than the PMOS transistor, then $V_M < \frac{V_{DD}}{2}$. From (16), it can be noted that the imbalance between the PMOS-NMOS transistors can be compensated with proper sizing. The imbalance of the networks can be also evaluated by the imbalance factor (IF), which is defined as the transistor current strength ratio I_{OP}/I_{ON}, as illustrated in Figure 8.

Figure 8 – VTC dependence on the imbalance factor.



Source – The Author.

2.2.2 Power dissipation

Melek et al. conducted a deep analysis of the CMOS inverter in [35]; the static and dynamic characteristics, as well as power dissipation, were analyzed.

The total power dissipation P_{tot} of the CMOS inverter consists of 3 components:

dynamic power, short-circuit power, and static power, as shown in Equation (17).

$$P_{tot} = P_{dyn} + P_{sc} + P_{stat} \tag{17}$$

The dynamic power P_{dyn} is dependent on the switching frequency (f_{switch}), activity factor (α), load capacitance (C_L) and quadratic dependent of the supply voltage, as shown in (18).

$$P_{dyn} = \alpha C_L V_{DD}^2 f_{switch} \tag{18}$$

The short-circuit power P_{sc} given in (19), is due to the simultaneous conduction of the PMOS and NMOS transistors. P_{sc} is linearly dependent on V_{DD}.

$$P_{sc} = V_{DD} \left(\frac{1}{T_{sc}} \right) \int_0^{T_{sc}} I_{SC} \, dt \tag{19}$$

where I_{SC} is the short circuit current and T_{sc} is the period of conduction of I_{SC} .

The static power P_{stat}, in (20), is independent of the frequency. However, it is dependent on the leakage current $I_{LK_{N(P)}}$, which has the same magnitude as $I_{N(P)}$, and is also dependent on the supply voltage.

$$P_{statN(P)} = I_{LKN(P)} V_{DD} \tag{20}$$

Static power is the dominant power in low-frequency applications, such as ULV domain systems [2]. In this work, the static power at $V_{DD} = 100$ mV can be further reduced by properly balancing the inverter, i.e., $I_N = I_P$, and by selecting appropriate transistors in the available CMOS technology, which will be discussed in detail in chapter 3.

2.2.3 Delay

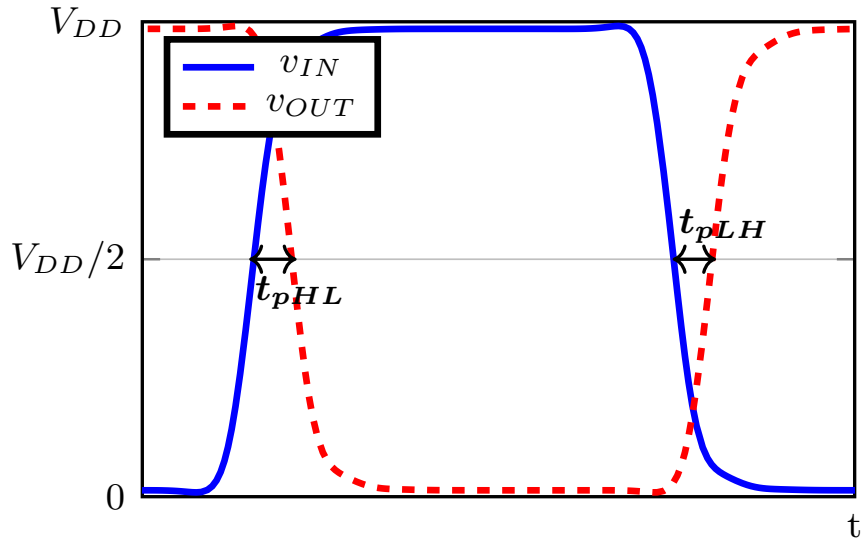
Indeed, the power dissipation in the subthreshold region is reduced by a lower supply voltage. However, the propagation delay t_p of the CMOS inverter increases exponentially [35], as shown in Equation (22). The inverter delay is defined as the maximum of the low-to-high $t_{p_{LH}}$ and high-to-low $t_{p_{HL}}$ delays, i.e., the worst-case scenario, as shown below.

$$t_p = \max \left(t_{p_{LH}}, t_{p_{HL}} \right) \tag{21}$$

The delay $t_{p_{LH(HL)}}$ is defined as the time it takes for the output voltage to switch from low-to-high (high-to-low), reaching the midpoint between the low and high logic levels,

i.e., 50% of V_{DD} in our CMOS logic case, after the input voltage switches from high-to-low (low-to-high). Figure 9 illustrates the definition of the delays.

Figure 9 – Definition of $t_{p_{HL(LH)}}$ and $t_{p_{HL(LH)}}$ of the CMOS inverter.



Source – The Author.

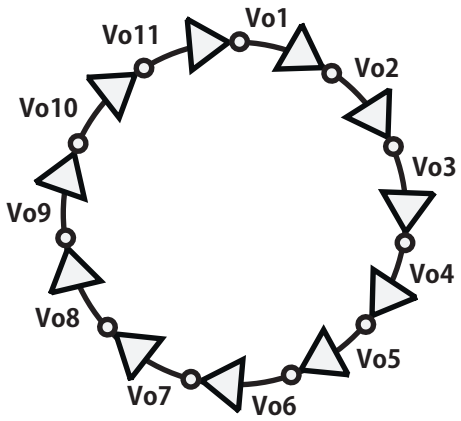
$$t_{pHL(LH)} = \frac{V_{DD}\left(0.5 + ln\left(\frac{1-e^{-\frac{V_{DD}}{2\phi_t}}}{1-e^{-\frac{V_{DD}}{\phi_t}}}\right)\right)}{2e^1 \frac{I_{S_{N(P)}}}{C_L} e^{\frac{V_{DD}-V_{TO_{N(P)}}}{n_{N(P)}\phi_t}}} \tag{22}$$

The delay of a CMOS inverter can also be calculated by measuring the oscillation frequency f_{osc} of a ring oscillator (ROSC). Equation (23) presents t_p in terms of the number of stages (N) and the f_{osc} of a ROSC.

$$t_p = \frac{1}{2N f_{osc}} \tag{23}$$

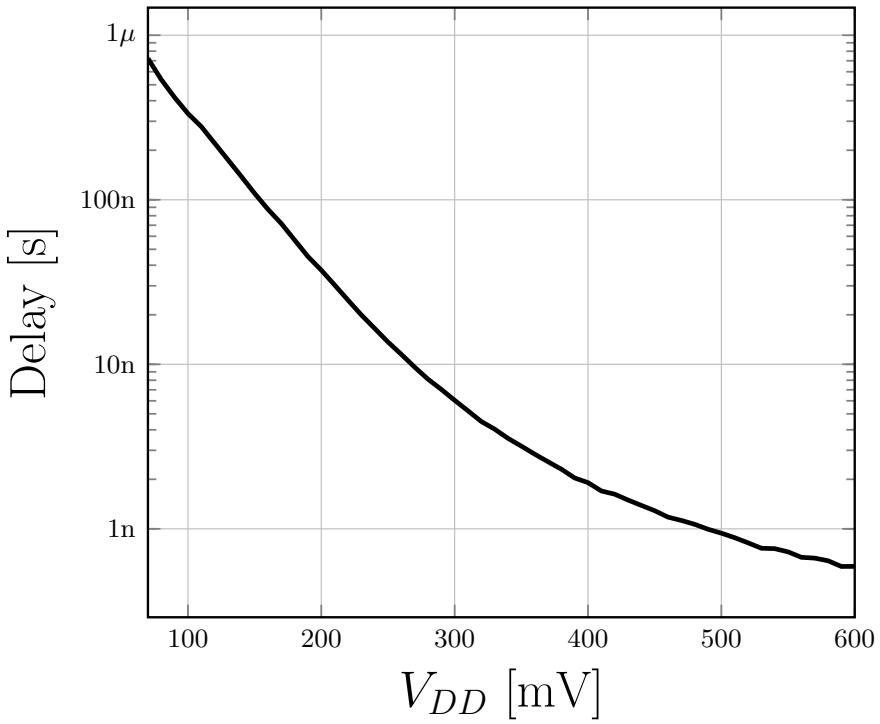
The ring oscillator shown in Figure 10 consists of an odd number of inverters in a loop. Following the guidelines for ULV ring oscillators discussed in [36], we chose the number of stages N=11. Figure 11 shows the delay of an inverter as a function of V_{DD}. One can observe that the subthreshold delay increases exponentially as the supply voltage decreases, in agreement with Equation (22).

Figure 10 – Ring Oscillator schematic



Source – The Author.

Figure 11 – Delay of an inverter vs V_{DD} in the 180 nm technology, with $\frac{W_N}{L_N} = \frac{420\ nm}{300\ nm}$ and $\frac{W_P}{L_P} = \frac{530\ nm}{300\ nm}$



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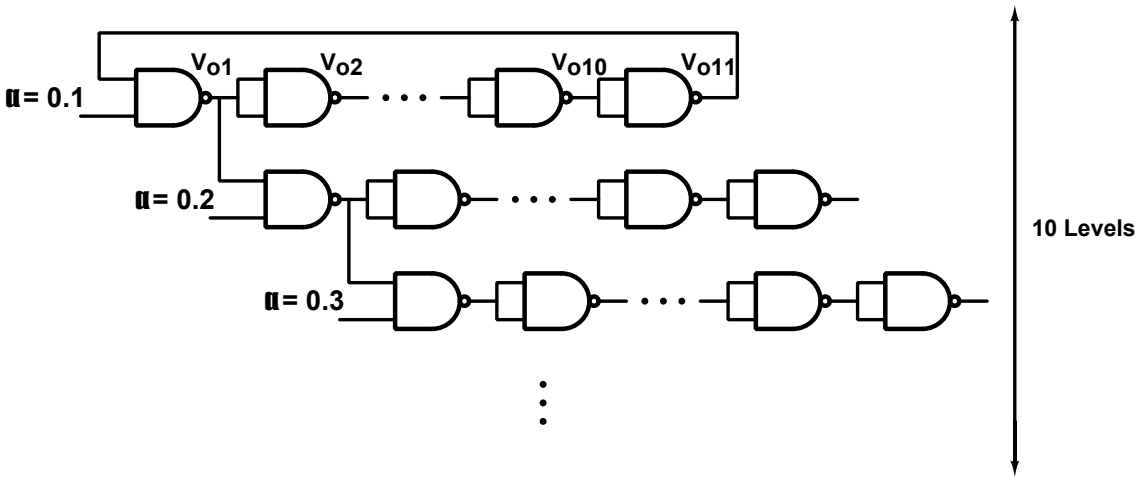
2.2.4 Power-delay-product

Another figure of merit evaluated in digital circuits is the power-delay-product (PDP). As the name implies, the PDP is the product of the total power dissipation (P_{tot}) and the propagation delay (t_p), as shown in Equation (24). It indicates the energy consumed per switching event by the CMOS circuit [23].

$$PDP = P_{tot}t_p \tag{24}$$

The design of subthreshold digital circuits with minimal energy consumption has been studied in detail by Wang et al. in [37], as well as the advantages of voltage scaling in CMOS logic and the dependence of the energy per switching event on the activity factor (α). In this work, the variable activity factor circuit presented in Chapter 4 of [37] was implemented using only NAND gates in the 180 nm technology. The circuit consists of 10 levels of 11 cascaded NAND gates, with the first level being a ring oscillator that drives the other branches when activated, as shown in Figure 12. The logic depth increases when one more branch is enabled, which is similar to the behavior of a processor pipeline. Also, by allowing one more level to operate, the activity factor increases 10%. The circuit is simulated through V_{DD} sweeps to determine the relationship between the PDP and the activity factor.

Figure 12 – Schematic of the variable activity factor circuit

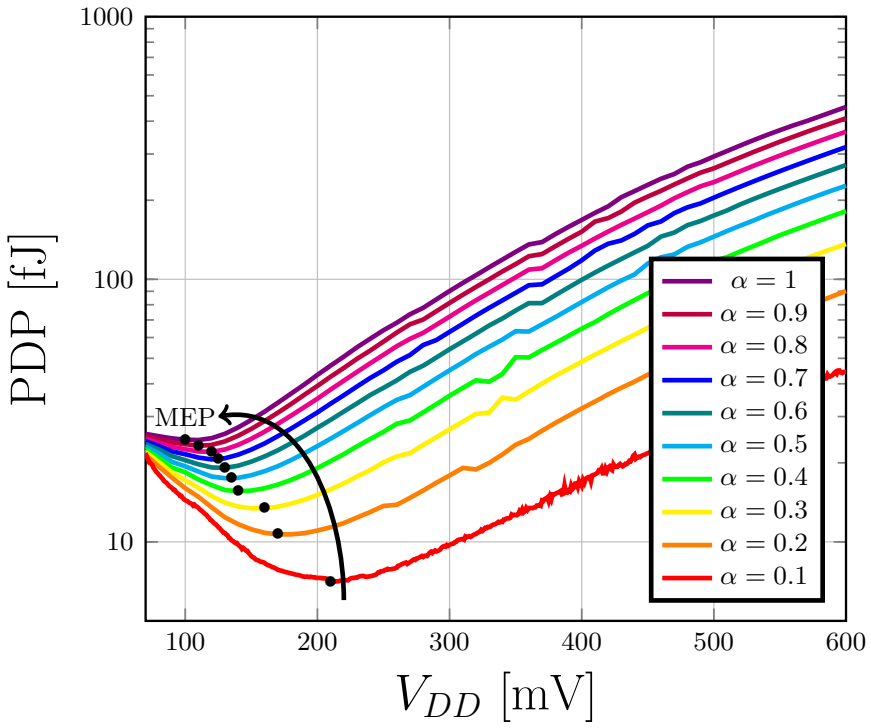


Source – The Author.

Figure 13 shows the energy per switching event (PDP) of the variable activity factor circuit as a function of the supply voltage. As mentioned earlier, lowering V_{DD} reduces the total power of a CMOS logic circuit, mainly due to the dynamic power component. However, lowering V_{DD} also exponentially increases the propagation delay, according to Equation (22), which leads to a minimum energy point in the PDP, even in the ULV domain.

Therefore, it is possible to control the V_{DD} to which the MEP occurs by simply increasing the activity factor which increases the dynamic power. For instance, the results in Figure 12 show the MEP shifts from $V_{DD} \approx 200$ mV to 100 mV as α increases from 0.1 to 1. This circuit is just one example of the relationship between the activity factor and the minimum energy point for CMOS logic, and it demonstrates the importance of determining the logic depth to design ULV systems with minimum energy consumption.

Figure 13 – PDP vs V_{DD} with variable activity factor.



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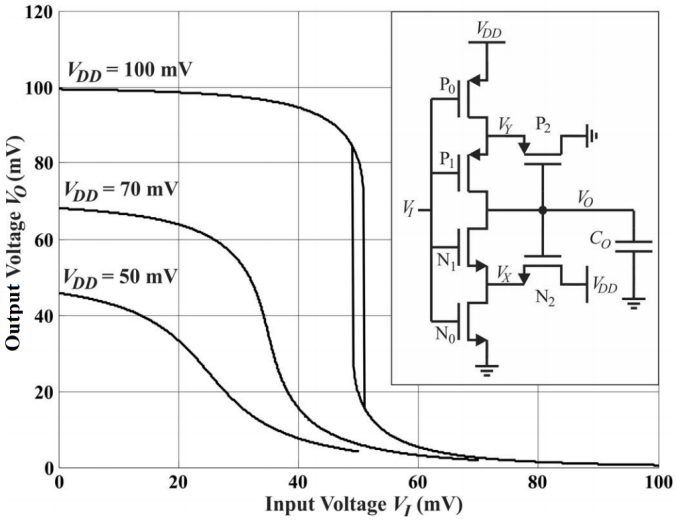
2.3 THE ULV SCHMITT TRIGGER

This section presents a brief overview of the design of a ULV Schmitt-trigger (ST), which was extensively investigated in [38] - [18]. Figure 14 shows the voltage transfer characteristic (VTC) of a CMOS Schmitt trigger with balanced PMOS and NMOS subcircuits under ULV operation [18]. The voltage transfer characteristic shows hysteresis for $V_{DD} = 100$ mV but not for $V_{DD} = 70$ mV and $V_{DD} = 50$ mV. As demonstrated in [38], the ST of Figure 14 cannot theoretically present hysteresis for supply voltages below 75 mV due to the lack of voltage gain. In practice, due to the non-perfect balance between the NMOS and PMOS networks and slope factors larger than unity, hysteresis can only appear for over 100 mV of supply. As mentioned in Subsection 2.1.2, the transistor current scaling factor, $I_{N(P)}$, in Equation (11b), represents the transistor strength, is dependent on both the technology parameters and dimen-

sions. For a balanced (symmetrical) ST, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$ and $n_N = n_P = n$.

Figure 14 – Voltage transfer characteristics of the symmetrical CMOS Schmitt trigger

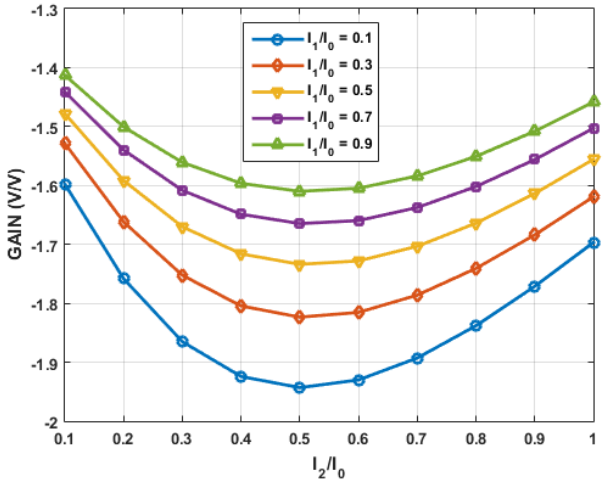


Source – [38]

The voltage gain of the ST circuit around $V_{DD}/2$, given by (25) [38], is a function of the supply voltage V_{DD} and ratios I_1/I_0 and I_2/I_0. Figure 15 shows the gain calculated using Equation (25) for $V_{DD} = 60$ mV. This low voltage was selected in order to explore the limits of the design space. The value of $I_1/I_0 = I_2/I_0 = 0.5$ was chosen for layout convenience.

$$\frac{v_o}{v_i} = \frac{\left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} - \frac{I_2}{I_0} e^{\frac{-V_{DD}}{\phi_t}}\right)\left(1 - e^{-\frac{V_{DD}}{2\phi_t}}\right)}{1 - \left(2 + \frac{I_0}{I_2} + \frac{I_1}{I_2} + \frac{I_2}{I_0}\right) e^{\frac{-V_{DD}}{2\phi_t}} - \left(1 + \frac{I_1}{I_0}\right) e^{\frac{-V_{DD}}{\phi_t}}} \tag{25}$$

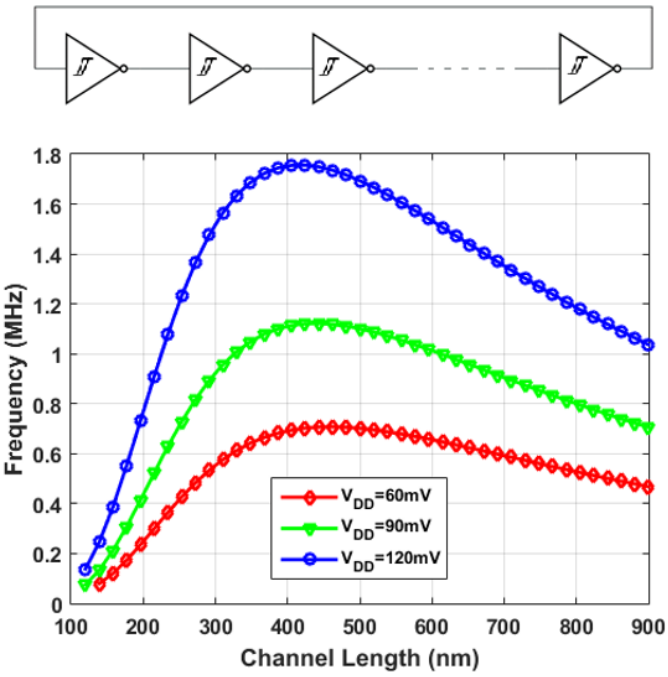
Figure 15 – Voltage gain of the ST inverter as a function of I_2/I_0.



Source – The Author.

The channel length is determined through the simulation results for the operating frequency of an ST-based 11-stage ring oscillator [36]. Due to the reverse short-channel effect (RSCE), in WI, the maximum operating frequency does not occur for the minimum channel length [36], [39], as shown in Figure 16 .

Figure 16 – Oscillation frequency as a function of the channel length.



Source – The Author.

For the 130 nm technology, the ratio of the widths of the corresponding p- and n-channel transistors is 5 to 1 to balance their current strengths for a supply voltage of 90 mV. The 180 nm technology did not present the RSCE, thus the minimum length will be used in the design.

Another significant characteristic of the ST inverter is that it is less sensitive to technology parameter variations than the conventional inverter since both the pull-up and pull-down circuits are composed of both nMOS and pMOS [38] transistors. Consequently, the robustness of the ST logic can be much higher than that of the conventional logic in ULV operation.

In [40], the design of an 8x8 multiplier based on the ST standard cell library was investigated with different cell strengths and additional layout area, with one sample operating at the extremely low voltage of 62 mV. Also, in [40], Lotze et al. investigate the static noise margin, on-to-off current ratio, temperature dependence, and operation frequency of the Schmitt Trigger. The ST was superior to the traditional CMOS inverter in almost all of those design spaces. However, the ST is slower than the CMOS inverter at the same supply voltage.

In this work, the ST will be used as a comparison to the CMOS inverter as a fundamental building block of a SCL to operate in the ULV domain.

3 STANDARD CELL DESIGN IMPLEMENTATION

Robustness is fundamental in any digital system [34]. It is well known that ultra-low-voltage design has a degraded performance [2] compared with the drift-dominant strong inversion design. Yet, while digital logic may function at extremely low voltages, another problem arises: the variability of the process fabrication [2]. This chapter will discuss the design of standard cells driven by variability awareness in subthreshold operation.

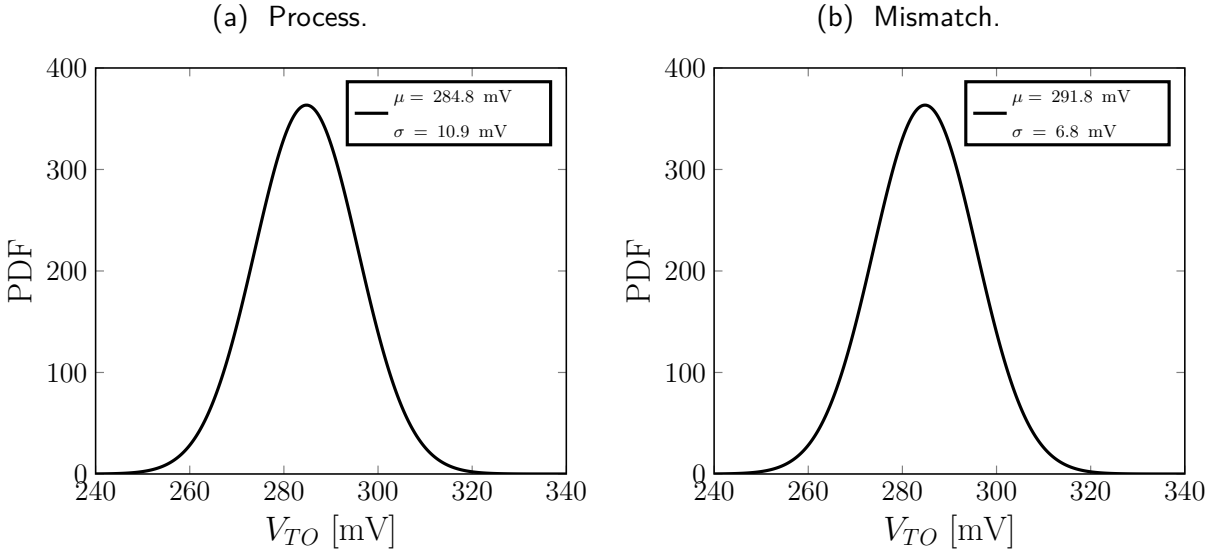
3.1 ADDRESSING VARIABILITY

The MOS parameters (V_{TO}, I_S, n, σ) are affected by the fabrication process due to variations in the device geometry, and random dopant fluctuations [9]. The MOSFET operating in the subthreshold regime is very sensitive to the threshold voltage due to the exponential relationship between the V_{TO} and the drain current, as shown in Equation (11).

The fabrication process variations can be classified into two major categories: mismatch and process. The mismatch variation is due to individual (local) device variations, and the process variations occur as a group (die-to-die, wafer-to-wafer) [9].

With the parameter extractor circuit from Figure 42a in Annex A, Monte Carlo simulations of an NMOS transistor using the BSIM4 MOS model were conducted to observe the V_{TO} variability due to mismatch and process. Figure 17 shows the result of 2000 samples Monte Carlo simulations. The dimensions of the NMOS were W = 420 nm and L = 300 nm. Figure 17a and 17b shows the variability of V_{TO} with respect to the process and mismatch, respectively.

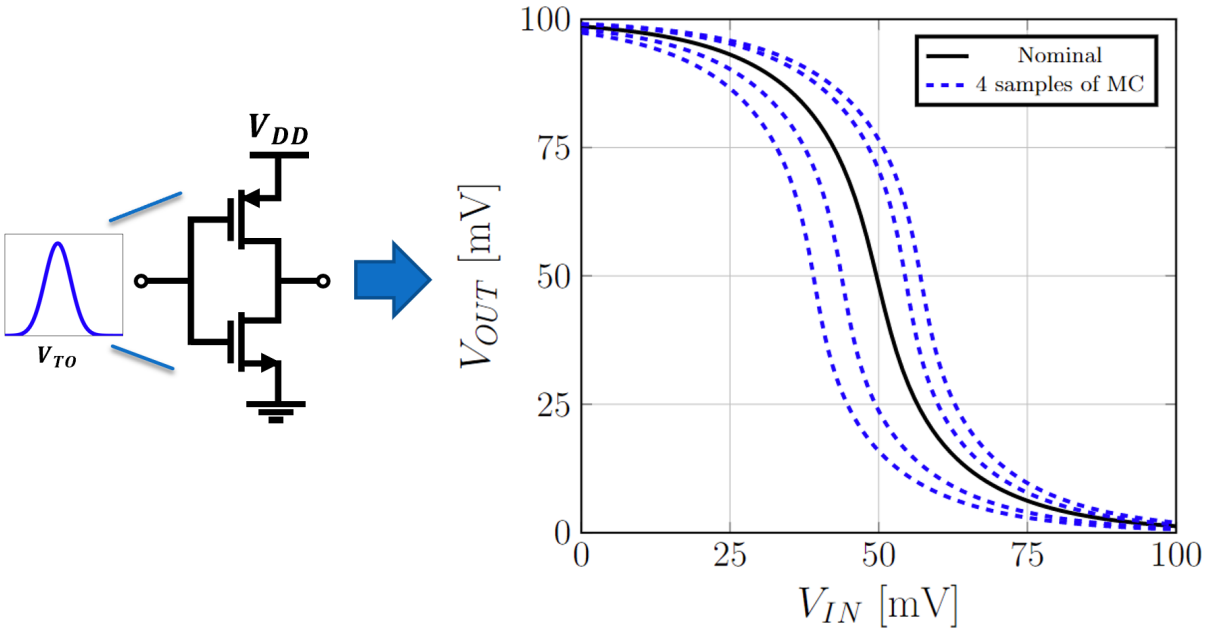
Figure 17 – Distributions of the threshold voltage of an NMOS transistor.



Source – The Author.

The standard deviations of V_{TO} in mismatch and process will have a considerate impact on the device drain current. Variations of the drain current of NMOS and PMOS transistors in a CMOS inverter will result in shifts in the VTC, as shown in Figure 18. Consequently, VTC shifts increase the logic cell's delay and total power variability.

Figure 18 – Impact of mismatch and process variation on VTC of the CMOS inverter at V_{DD} = 100 mV.



Source – The Author.

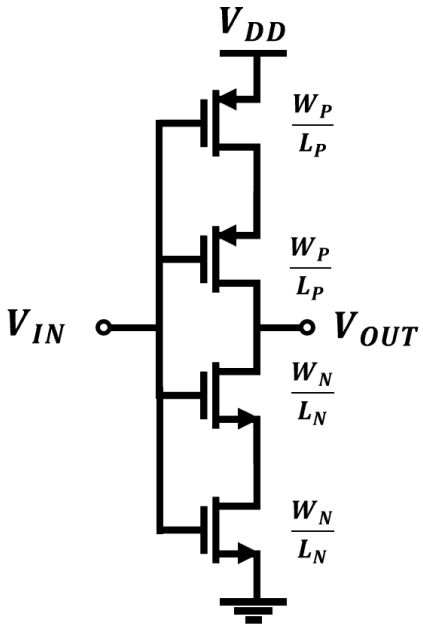
3.1.1 Techniques to Improve Robustness

To address this variability (σ/μ) problem of the threshold voltage, the design of the ULV standard cells will combine already known techniques to improve the robustness, i.e., minimize the shift in the VTC of the logic cell. Presented by Pelgrom et al. in [41], the first technique consists of increasing the area of a MOS transistor which will decrease the standard deviation of the threshold voltage due to mismatch, as shown in Equation (26).

$$\sigma_{V_{TO}} = \frac{A_{V_{TO}}}{\sqrt{WL}} \tag{26}$$

The second technique was introduced by Bjerkedok et al. in [42]; which instead of increasing only the W or L of the MOS transistor in a logic gate, they use a series association of MOS transistors called "slices".

Figure 19 – Schematic of a Slice.

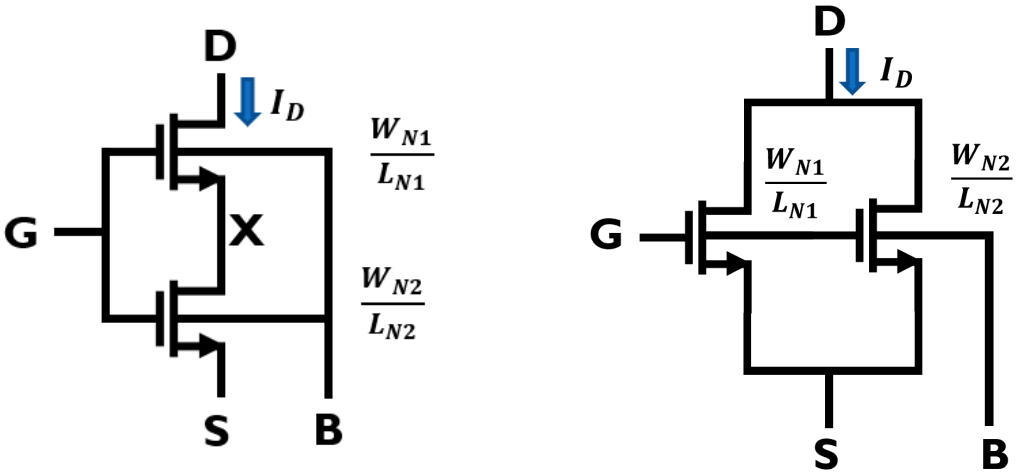


Source – The Author.

The symmetry of the MOS transistor is suitable for making associations equivalent to a single device. Such associations can be series or parallel, as shown in Figure 20.

Figure 20 – MOS associations.

(a) Series association of 2 MOS transistors. (b) Parallel association of 2 MOS transistors.



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The associations of transistors with the same channel width and terminals connected in series allow the construction of a device equivalent to a single transistor. The length L of this device is the result of the sum of the unit channel lengths and a width W. On the other

hand, in parallel associations of transistors with the same channel length, we obtain a device with a width equivalent to the sum of the unit widths and a length L.

To model the series associations in the triode region, we consider the schematic shown in Figure 20a. The composition presented here consists of two NMOS transistors connected from node "X" connecting drain and source of N1 and N2, respectively, with the gate and substrate terminals common to both devices. The formal analysis presented in [43] using the gradual channel approximation allows us to write the drain current as a function of the applied potentials at the gate,source (V_G, V_S) and gate,drain (V_G V_S) terminals, as expressed in the equation (27).

$$I\left(V_G, V_X\right) = \frac{\left(\frac{W}{L}\right)_{N1} I\left(V_G, V_D\right) + \left(\frac{W}{L}\right)_{N2} I\left(V_G, V_S\right)}{\left(\frac{W}{L}\right)_{N1} + \left(\frac{W}{L}\right)_{N2}} \tag{27}$$

From Equation (27) and using the ACM model we have that the drain current for a series composition of two transistors is

$$I_D = \left(\frac{W}{L}\right)_{eq} \left[I\left(V_G, V_S\right) - I\left(V_G, V_D\right)\right] \tag{28a}$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_{N1}\left(\frac{W}{L}\right)_{N2}}{\left(\frac{W}{L}\right)_{N1} + \left(\frac{W}{L}\right)_{N2}} \tag{28b}$$

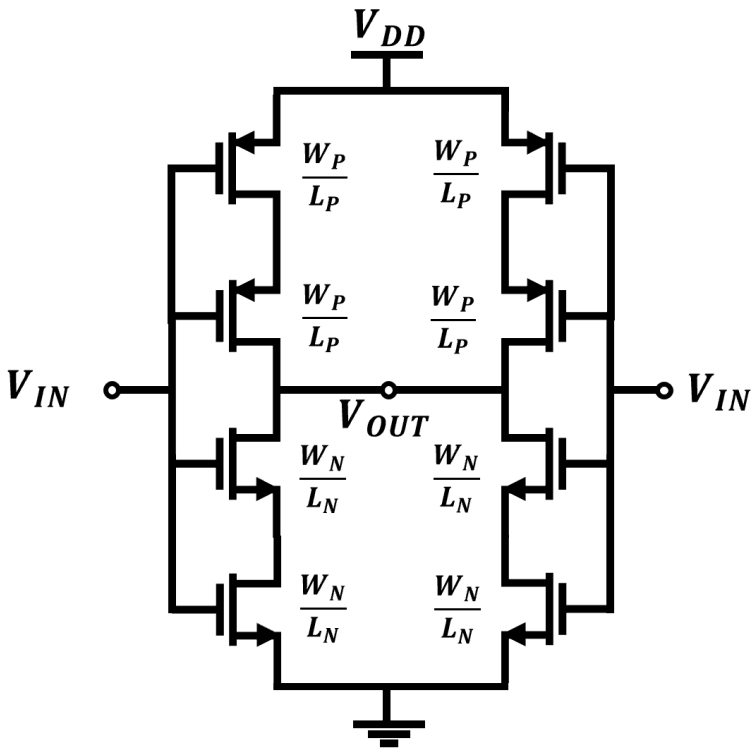
Equation (28) shows that the current obtained through the series association for transistors in linear region is similar to that obtained with a unitary transistor whose aspect ratio is equivalent. For example, in a series association of two unitary transistors (N1 = N2) the equivalent aspect ratio is

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_{N1}}{2} \tag{29}$$

For the parallel association of 2 unitary MOS transistors of identical lengths, the equivalent width is $W_{eq} = 2W_N$. The methodology presented in this section can be used for the association of PMOS transistors.

MOS association modeling can be used for the slice shown in Figure 19, which results in the transistor strength in each network being half of the strength of the CMOS inverter. Therefore, a single slice is equivalent to a CMOS inverter with half of the current strength. Using two slices connected, as seen in Figure 21, results in implementing the CMOS inverter-sliced, which has the same current strength as the conventional CMOS inverter.

Figure 21 – Schematic of two Slices.



Source – The Author.

The two slices topology is extremelly versatile. In principle, one can implement any combinational logic function, which includes the traditional Boolean logic gates: NAND, NOR, XOR, XNOR, INV, AOI, OAI and so on.

For example with the truth table of the NAND gate, given in Table 2, the NAND with slices implementation is straighfoward by only changing the inputs of the two slices topology. The same method can implement the others Boolean gates.

Table 2 – Truth table of the 2-input NAND gate.

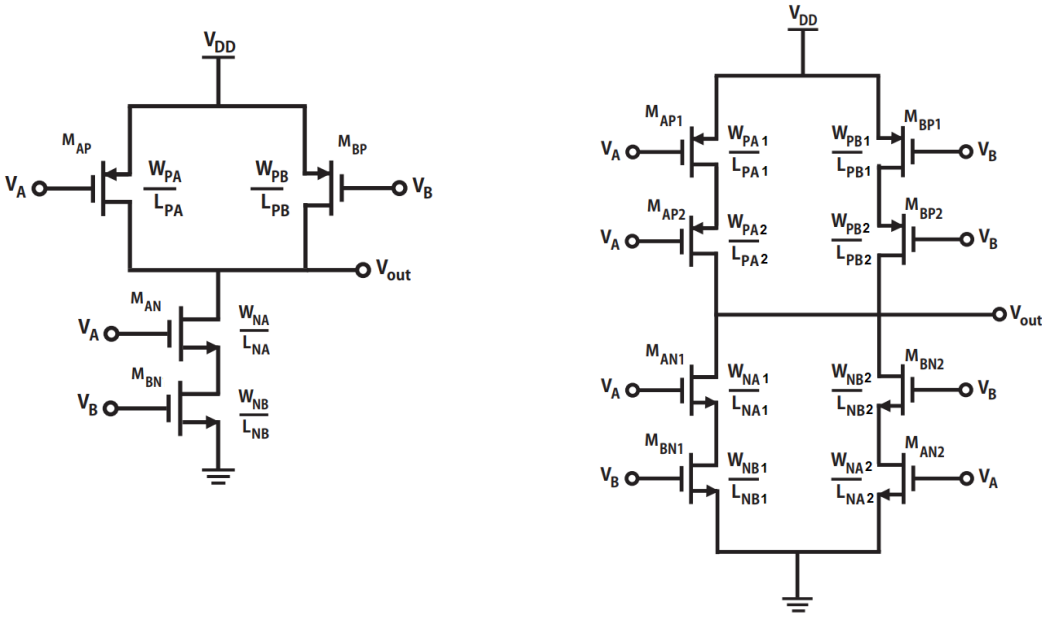
A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Source – The Author.

Figure 22a shows the conventional NAND CMOS and Figure 22b shows the application of the sliced technique in a NAND gate, called NAND-Sliced from now on.

Figure 22 – Schematic of the NAND logic gates.

(a) Conventional NAND. (b) NAND-Sliced.

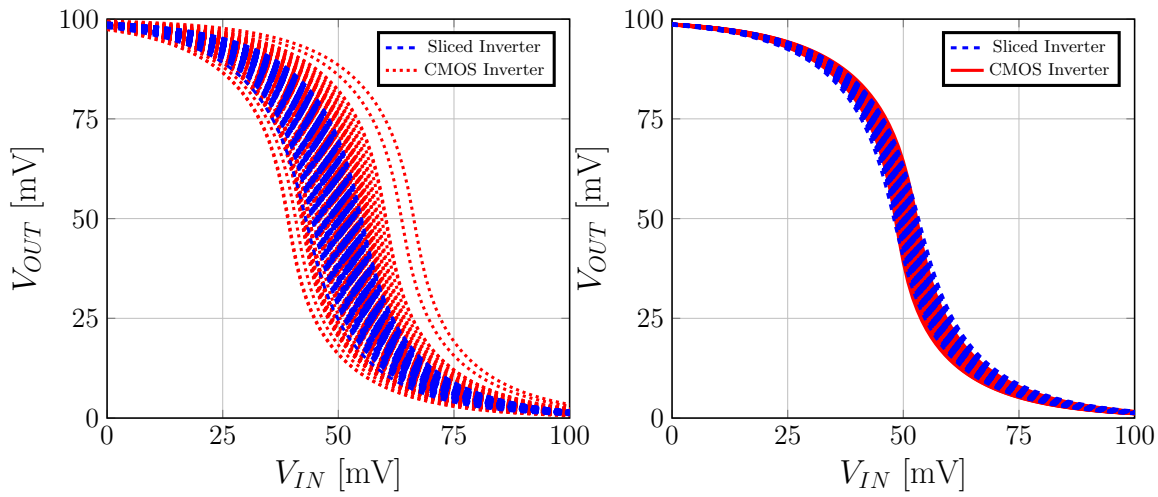


Source – The Author.

Figure 23 shows the result of 200 samples of Monte Carlo simulations with mismatch and process variations. Visibly, the sliced inverter topology decreases variability due to device mismatch.

Figure 23 – Comparison of VTCs of sliced and traditional CMOS inverter, from 200 samples of Monte Carlo: mismatch and process variations. Sliced from Figure 21. The dimensions of the transistors are : $\frac{W_P}{L_P} = \frac{530\,nm}{300\,nm}$ and $\frac{W_N}{L_N} = \frac{420\,nm}{300\,nm}$.

(a) Mismatch. (b) Process.



Source – The Author.

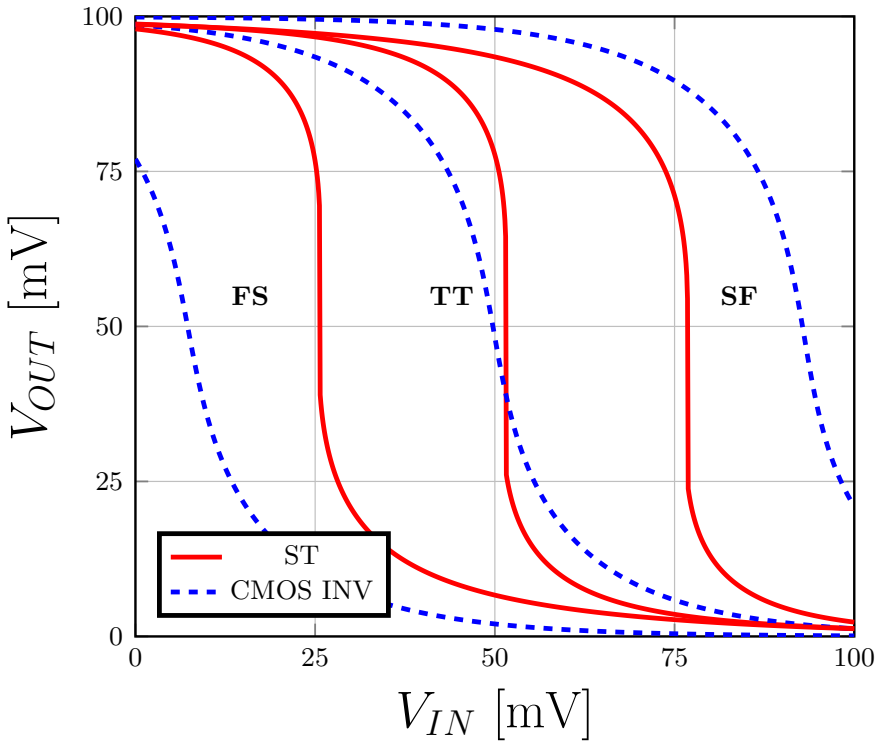
Despite the increased robustness of the logic circuit, the use of the sliced technique has disadvantages regarding the total power dissipation and the delay of the cell; as it was explained in [42], the metrics of the sliced-based cells will be evaluated in section 3.4.

3.1.2 Schmitt trigger vs process corners

Another way to analyze process variations is by simulating the circuit at the extremes of the manufacturing process (corners). The first letter in the corner refers to the NMOS transistor, and the second refers to the PMOS transistor. The typical-typical (TT) corner of the process uses the nominal parameters of the transistor; the slow-fast (fast-slow) corners SF(FS) is related to the threshold voltage of the MOS transistor, i.e., in a slow transistor, the threshold voltage has a higher value compared to the typical transistor; in a fast transistor, the opposite occurs.

Figure 24 shows the lower susceptibility of the ST to the fabrication process due to the configuration of its pull-down network (PDN) and pull-up network (PUN). The ST pull-up network is composed of transistors P0, P1, and N2; at the corner SF, for example, transistor N2 is slow, but is compensated by the network configuration, as P0 and P1 are fast.

Figure 24 – Comparison of VTCs of ST and traditional CMOS inverter, from simulation, for FS,TT, and SF corners at $V_{DD} = 100$ mV.



Source – The Author.

3.2 SIZING STRATEGIES IN ULV STANDARD CELLS

In the ultra-low-voltage cell libraries, the design's main objective is to minimize the imbalance factor between the pull-up and pull-down networks of the standard cells to ensure functionality and enhance performance in the ULV domain [2]. The performance in the subthreshold region can be increased by choosing an appropriate transistor in the available process design kit (PDK).

The key MOS parameter to increase performance in the subthreshold region is the threshold voltage due to the exponential relationship between V_{TO} and the drain current, already presented in Equation (11). There are three types of transistors in the available 180 nm technology: standard threshold voltage (STD), medium threshold voltage (MVT), and native threshold voltage (NVT). The NVT is not adequate to design logic cells because there is no PMOS transistor in the available PDK. The STD and MVT transistors can be used to design standard cells, but for the ULV domain, the MVT is more appropriate due to the lower value of V_{TO}, which increases the drain current for the target supply voltage ($V_{DD} = 100$ mV), thus improving the cell performance.

The starting point for designing a CMOS inverter is to choose the supply voltage and the NMOS geometry. In this work, the target V_{DD} is 100 mV, and the NMOS aspect ratio will be $W_N/L_N = 300$ nm/300 nm, which are the minimum width and length of the MVT transistor. With the supply voltage and aspect ratio defined, the next step is to run a simulation on Cadence Virtuoso© simulator to determine the width of the MVT PMOS transistor; the simulator uses BSIM 4.5 to model the MOSFET [33]. For a simple CMOS inverter, the perfect balance between PDN and PUN happens when $V_M \approx \frac{V_{DD}}{2}$ which is obtained by sizing the PMOS-NMOS transistors properly, as mentioned in Section 2.2.1. The balanced PDN and PUN will result in $t_{p_{HL}} = t_{p_{LH}}$ and lower power dissipation.

With the PMOS-NMOS aspected ratios, one can extract (Annex A) the four parameters of the MOS presented in Section 2.1.1. The sizes of the transistors, as well as their parameters, are indicated in Table 3.

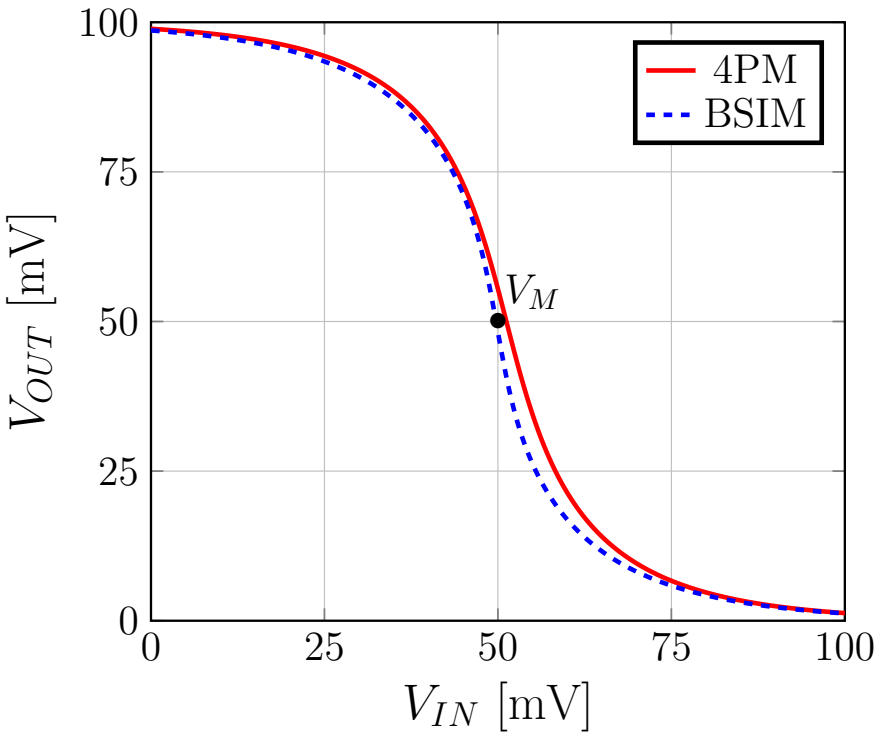
Table 3 – Dimensions and parameters of the balanced CMOS inverter in 180 nm technology.

Parameters	**NMOS**	**PMOS**
W/L [nm/nm]	300/300	490/300
I_S [nA]	74	80
V_{T0} [mV]	258	-279
n	1.12	1.27
σ [mV/V]	14	23

Source – The Author.

The design was validated using the four-parameter model and BSIM in the Cadence© simulator. Figure 25 shows the VTC of the CMOS inverter for $V_{DD} = 100$ mV.

Figure 25 – CMOS inverter VTC at $V_{DD} = 100$ mV. The dimensions of the transistors are given in Table 3.



Source – The Author.

In more complex gates, the perfect balance of PUN/PDN is in general not possible since the imbalance factor varies for multi-input standard cells.

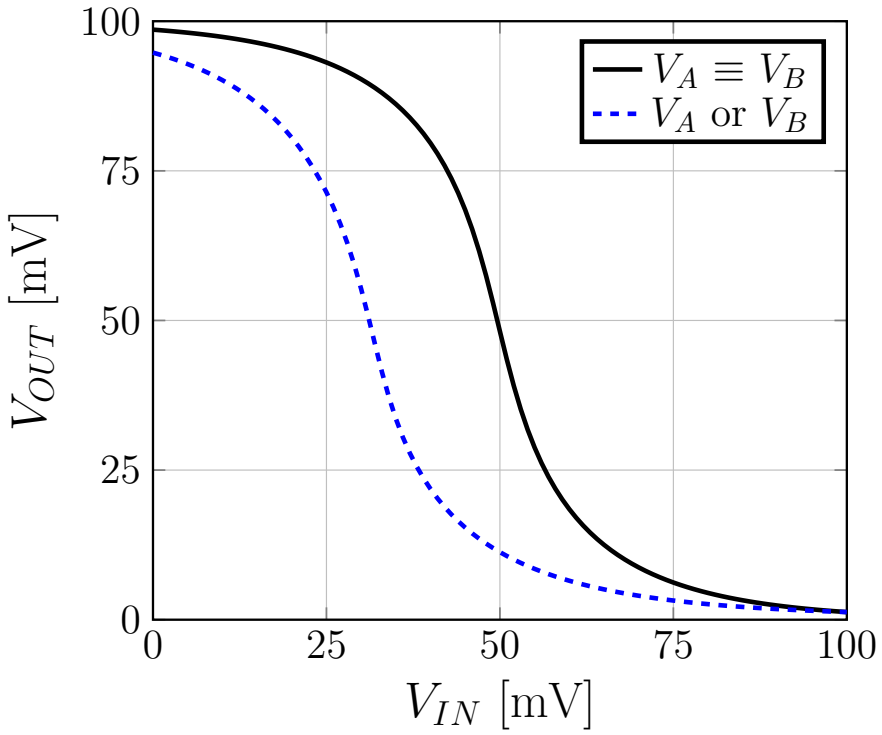
Equation (30) presents the equivalent strength (I_{EQ}) of the series/parallel associations of the NAND-Sliced. In (30a), one of the inputs (V_A) changes while the other input (V_B) is held constant at V_{DD}. In (30b), both inputs (V_A and V_B) vary simultaneously, i.e., $V_A \equiv V_B$. In this case, the NAND-Sliced gate is equivalent to an inverter with a PMOS transistor equivalent to the series/parallel associations of MAP1, MAP2, MBP1, and MPB2, and an NMOS transistor equivalent to the series/parallel associations of MAN1, MAN2, MBN1, and MNB2. Therefore, the transistors of the NAND-Sliced present the same dimensions of Table 3. Figure 26 shows the VTC of the NAND-Sliced designed with conditions (a) and (b).

$$I_{EQ,P} = \frac{I_P}{2} \qquad and \qquad I_{EQ,N} = I_N \tag{30a}$$

$$I_{EQ,P} = I_P \qquad and \qquad I_{EQ,N} = I_N \tag{30b}$$

The other complex gates of the sliced library (NOR,OAI21,AOI21,AOI22) can be designed using the same methodology.

Figure 26 – NAND-Sliced VTC at $V_{DD} = 100$ mV.



Source – The Author.

The design of the ST-Sliced standard cells combines the strategies mentioned in Section 2.3 with the sliced technique.

3.3 LAYOUT OF A STANDARD CELL

The layout of a standard cell has a vital role in minimizing the threshold voltage variability. All the standard cells are equal in height and with variable width, as shown in Figure 27. The supply rails V_{DD} and ground (GND) are located at the edges of the cell; in between are located the PMOS, NMOS transistors, the polysilicon and metal interconnections [34].

To mitigate the V_{TO} variations, safety margins are maintained from the borders to minimize the impact of the well proximity effect [44].

The width of the NMOS transistor was slightly increased from 300 nm to 420 nm for layout convenience. The same sizing strategies of Section 3.2 were used to balance the pull-up and pull-down networks. Table 4 shows the final geometries and parameters of unitary transistors used in the sliced-based standard cell libraries.

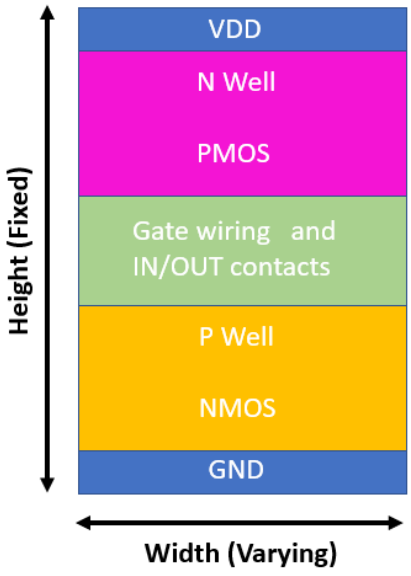
Table 4 – Dimensions and parameters of the transistors used in the SCL in 180 nm technology.

Parameters	**NMOS**	**PMOS**
W/L [nm/nm]	420/300	530/300
I_S [nA]	168	86
V_{T0} [mV]	292	-279
n	1.21	1.26
σ [mV/V]	15	24

Source – The Author.

Appendix I and J show the layout of the NAND-Sliced and the NAND-ST, respectively. Visibly, both the sliced and ST libraries increase the total area of each cell. However, the increase in cell area by the sliced technique will mitigate parameter variations and improve the logic gate's regularity and manufacturability [42].

Figure 27 – Standard cell layout style

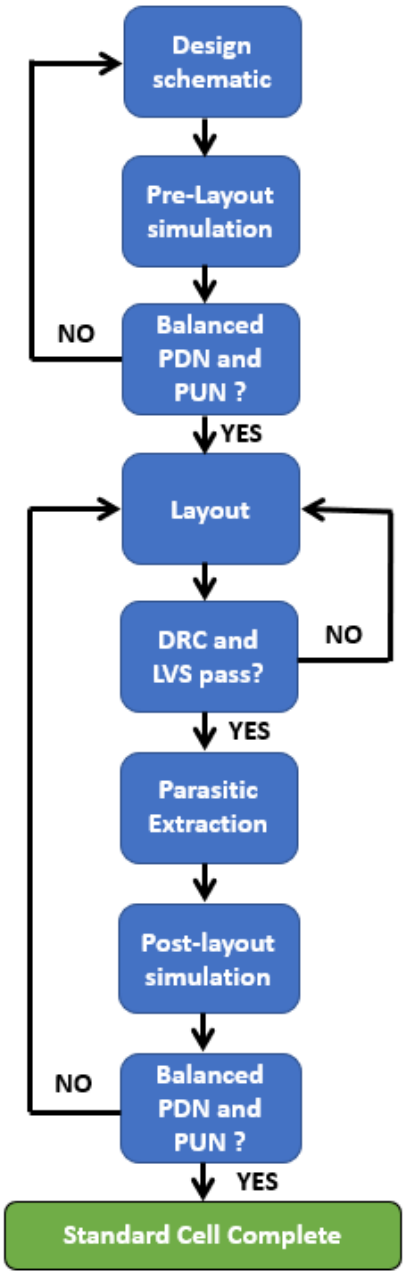


Source – The Author.

All the layouts of the standard cells were verified through the design rule check (DRC) and the layout versus schematic (LVS) tools in Cadence Virtuoso©.

The design of the ULV standard cell library can be summarized by the design flow presented in Figure 28. All the schematics and layouts of the ULV-SCL in 180 nm technology are presented in Appendix D - Appendix X.

Figure 28 – Design flow of the ULV standard cell library



Source – The Author.

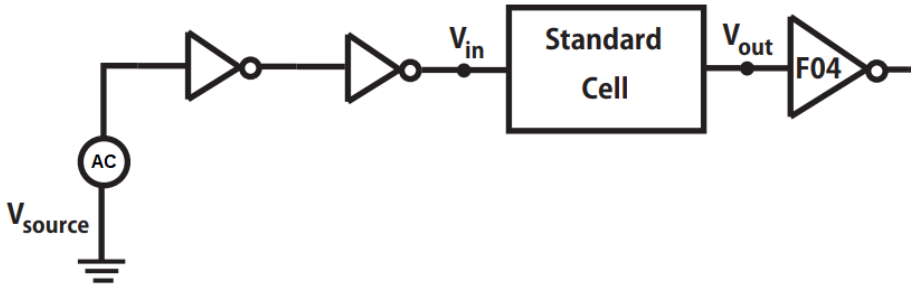
3.4 STANDARD CELL SIMULATIONS

The simulations of the standard cells was performed using the Virtuoso Analog Design Environment tool in Cadence©, for a temperature of 27°C and in the typical-typical (TT) corner. The MOSFET model used in this simulations was the BSIM4.5, which is commonly used in commercial simulators.

The simulations use the testbench in Figure 29, in which the input slew is emulated by two simple CMOS inverters, and the load capacitance is a fan-out of four (FO4), i.e., four

CMOS inverters connected in parallel.

Figure 29 – Testbench used to characterize the standard cells



Source – The Author.

The simulations to evaluate the standard cells are composed of three CMOS logic performance metrics: total power, delay, and PDP [34]. The total power was calculated from the product of each simulated cell's average current and supply voltage. The propagation delay was measured according to the definition introduced in section 2.2.3. The PDP was calculated based on its definition, i.e., the product of total power and propagation delay.

Table 5 presents the results of the time-domain simulations and total area of each Sliced-based cell in the ULV minimalist standard cell library.

Table 5 – Simulation results of the Sliced Library in 180 nm technology.

Standard Cell	Delay [nS]	Total Power [pW]	PDP [aJ]	Area [μm^2]
Inverter	437	22	9.6	9.92
Inverter-Sliced	535	23	12.3	24.61
Inverter-Slicedx2	432	41	17.7	49.21
Inverter-Slicedx4	408	76	31.0	98.42
Inverter-Slicedx16	422	344	145.2	393.76
NAND-Sliced	535	23	12.3	24.61
NAND-Slicedx16	422	344	145.2	393.76
NOR-Sliced	535	23	12.3	24.61
NOR-Slicedx16	422	344	145.2	393.76
OAI21-Sliced	535	23	12.3	28.99
OAI21-Slicedx16	422	344	145.2	463.84
AOI21-Sliced	535	23	12.3	28.99
AOI21-Slicedx16	422	344	145.2	463.84
AOI22-Sliced	535	23	12.3	28.99
AOI22-Slicedx16	422	344	145.2	463.84

Source – The Author.

The standard cell's drive strength is represented by x followed by the number of cells in parallel, i.e., x2 is two cells connected in parallel, with x4 and x16 following the same logic, as shown in Appendix G and H. The sliced technique significantly increases area compared to the traditional CMOS logic. The area of the Inverter-Sliced is 2.48 times larger than the area of the traditional CMOS inverter. Due to the larger area, the sliced logic will have larger capacitances resulting in a more significant delay, according to (22). However, the total power dissipation is almost the same due to the operation in the ULV domain.

The same transient simulations were conducted for the ST-Sliced-based SCL; the results are presented in Table 10, Appendix A. The ST SCL presents a more significant delay and power dissipation than the Sliced-based SCL.

3.5 SEQUENTIAL STANDARD CELLS

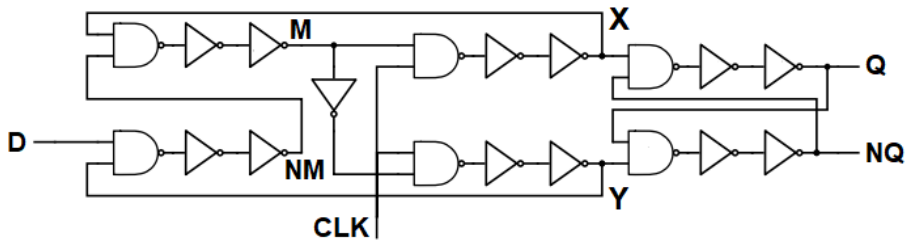
Up to now, the design of the standard cell library was limited to the implementation of combinational logic circuits. Nevertheless, sequential elements are essential to implement synchronous digital systems. Different from combinational logic circuits, where the output state depends on the current input signals, the output of sequential circuits depends not only on the input signal, but also on the previous state of the output [34]. Two D-flip-flop (DFF) were designed using the standard cell library combinational gates.

3.5.1 Flip Flop design

An extensively comparative analysis of Flip-Flop architectures was done in [45]-[46], illustrating the advantages of each architecture regarding performance and power dissipation.

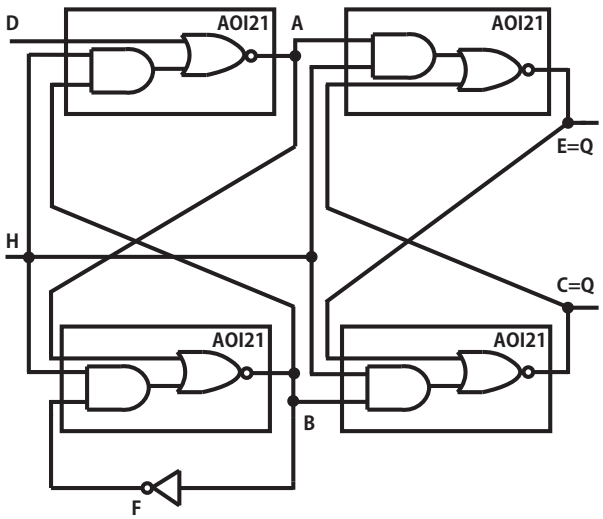
In this dissertation, we prioritize the robustness of the circuit in ultra-low-voltage operation. To ensure the robustness and fault-tolerance of the flip-flop, we chose two race-free flip-flop architectures presented in [47]-[48]. Race conditions in digital circuits occur when two or more binary state variables change value when one input variable changes; due to unequal delay on each path, the circuit cannot compute the future output state. Figure 30 and Figure 31 show the two chosen DFF architectures.

Figure 30 – Race-free D-Flip-Flop architecture 1 (DFF1).



Source – The Author, adapted from [47].

Figure 31 – Race-free D-Flip-Flop architecture 2 (DFF2).



Source – The Author.

In the design of DFF1 [47], Piguet's topology was adapted with the addition of 2

inverters to regenerate the signal of each node, to improve ULV operation at the expense of area. The DFF's were simulated with the same testbench shown in Figure 29, Table 6 shows the delay, power dissipation, and PDP of each DFF. The ST-based SCL FF results are displayed in Table 10, Appendix A. DFF2 [48] is faster, smaller and dissipates less power in Sliced or ST logic.

Table 6 – Simulation results of the Sliced D-Flip-Flops in 180 nm technology.

Standard Cell	**Delay [μS]**	**Total Power [pW]**	**PDP [fJ]**	**Area [μm^2]**
DFF1	5.41	438.7	2.37	467.59
DFF2	1.32	126.7	0.17	18.57

In the next chapter, we validate the design of the standard cell library (combinational and sequential cells) through the design and test in silicon of frequency dividers.

4 DESIGN AND TEST OF FREQUENCY DIVIDERS BASED ON THE ULV-SCL

The ultra-low-voltage minimalist standard cell library was validated through the design of frequency dividers (FD).

4.1 CHIP 1 - FIRST FREQUENCY DIVIDER PROTOTYPE

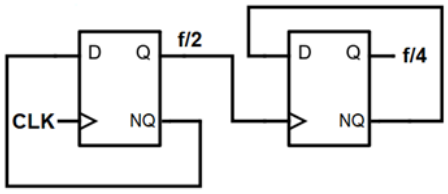
The first is a counter-based frequency divider. Counter-based frequency dividers perform division by operating similarly to digital counters [49]. A digital counter operates by changing the output when a rising or falling edge of a clock signal is detected. A single-bit digital counter can toggle its output between two values and act as a divide-by-two stage. The type of counter determines the sensitivity to either edge, and the reaction of the counter to only one edge-type of the clock means skipping the other edge-type. In other words, only a rising or falling edge will make the counter toggle its output. Because the counter only counts half of the edges, the resulting output waveform has only half the clock signal frequency used for toggling the counter. Equation (31) shows the dependency of output frequency (f_{out}) of the counter-based frequency divider with the number of stages (N) and the input frequency (f_{in}).

$$f_{out} = \frac{f_{in}}{2^N} \tag{31}$$

The first prototype uses a minimalist standard cell library designed in 130 nm technology. The transistor dimensions, logic cells metrics are shown in Appendix B.

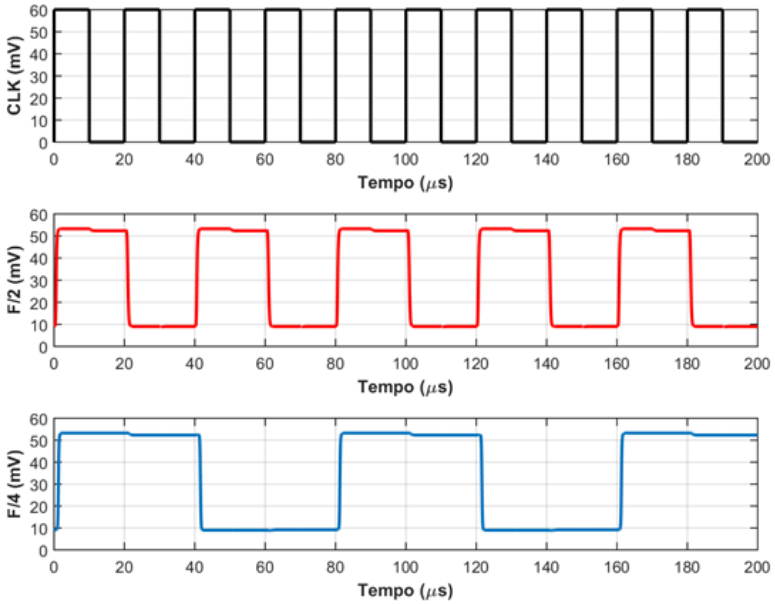
Figure 32 shows the schematic of a counter-based frequency divider by four using the DFF1 topology (FD1). Figure 33 shows the result of a transient simulation of the FD1 operating at a supply voltage of 60 mV and an input frequency of 25 kHz, using the same testbench shown in Figure 29.

Figure 32 – Schematic of a counter-based frequency divider by four using the DFF1 topology.



Source – The Author.

Figure 33 – Counter-based Frequency divider by 4 operating at $V_{DD} = 60$ mV.



Source – The Author.

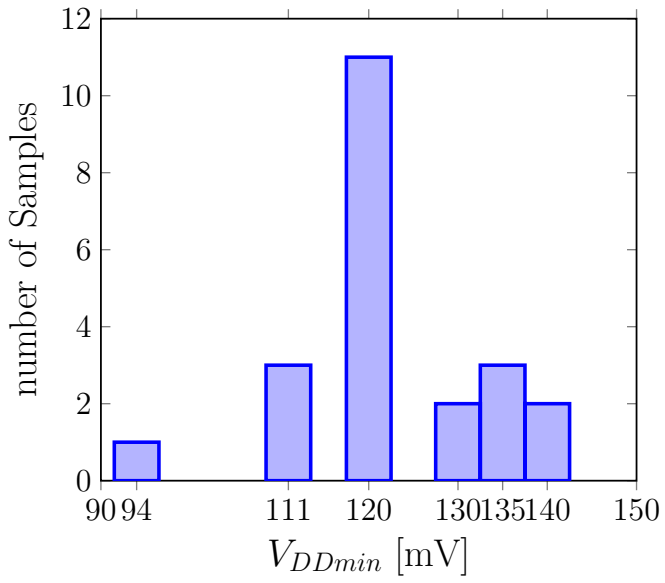
A 15-stage chain frequency divider, using both conventional logic and ST logic, was fabricated in a 130 nm CMOS technology. Figure 34 shows the output signals of both frequency divider chains at 76 mV of the supply voltage. The conventional logic (upper wave) does not operate properly, while the ST logic (lower wave) keeps the signal of 1 Hz at 76 mV. An early study of this prototype was conducted in [50], and a paper [51] was published in the International Symposium on Circuits and Systems 2020.

Figure 34 – Output signals of both frequency divider chains at 76 mV of supply voltage

Source – The Author.

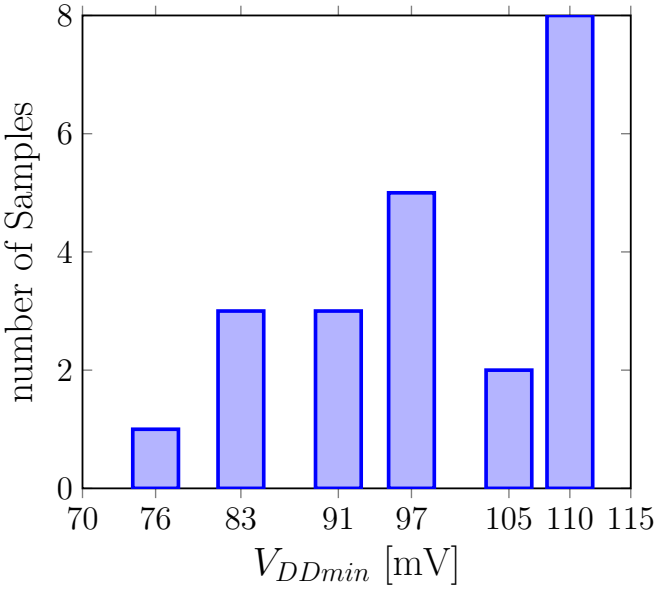
Twenty-two samples were measured, the minimum supply voltages results are presented in Figure 35 and Figure 36. All the ST based samples are fully functional with a $V_{DDmin} =$ 110 mV and a maximum input frequency of 262,144 kHz (or 2^{18} kHz). The conventional logic samples are fully functional with a $V_{DDmin} =$ 140 mV and an input frequency of 1 MHz.

Figure 35 – Minimum supply voltage of the 15-stages frequency divider chain in the tapeout 1 - Conventional logic, with 32 kHz of input frequency.



Source – The Author.

Figure 36 – Minimum supply voltage of the frequency divider by 2^{15} in the tapeout 1 - ST-based logic, with 32 kHz of input frequency.



Source – The Author.

4.2 CHIP 2 - SECOND FREQUENCY DIVIDER PROTOTYPE

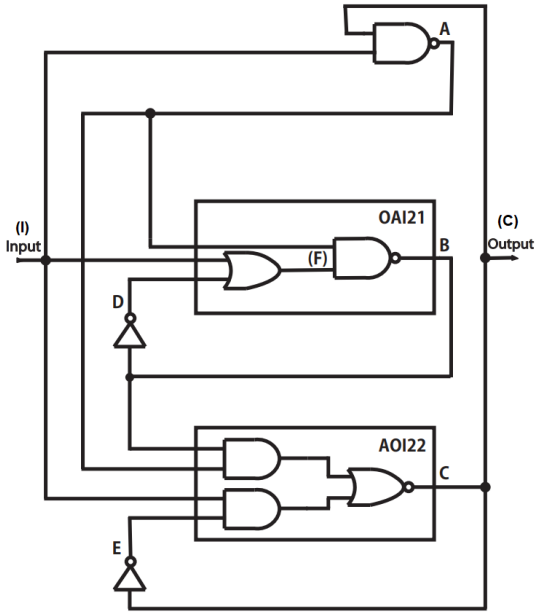
The second implementation of the FD was based on the extensive study of race-free circuits conducted on [48] and [52]. As mentioned before, a race condition in digital circuits occurs when two or more binary state variables change value when one input variable changes; due to unequal delay on each path, the circuit cannot compute the future output state. The schematic of the second frequency divider, presented in Figure 37, was the result of an algorithm that tries to synthesize all possible counters with complex gates (OAI or AOI).

The boolean equations in Equation (32) are the final result of a particular state assignment that removes the intermediate unstable states.

$$\begin{aligned} A &= \overline{IC} \\ B &= \overline{(I+D)A} \\ C &= \overline{IE+AB} \\ D &= \overline{B} \\ E &= \overline{C} \end{aligned} \tag{32}$$

Figure 38 shows the transient simulation of the Vittoz frequency divider with input (I), output(C), and intermediate signals A, B, D, and E. The testbench presented in Figure 29 was used in this simulation. Visibly the output signal has half of the frequency of the input signal.

Figure 37 – Vittoz Frequency divider by 2.



Source – The Author.

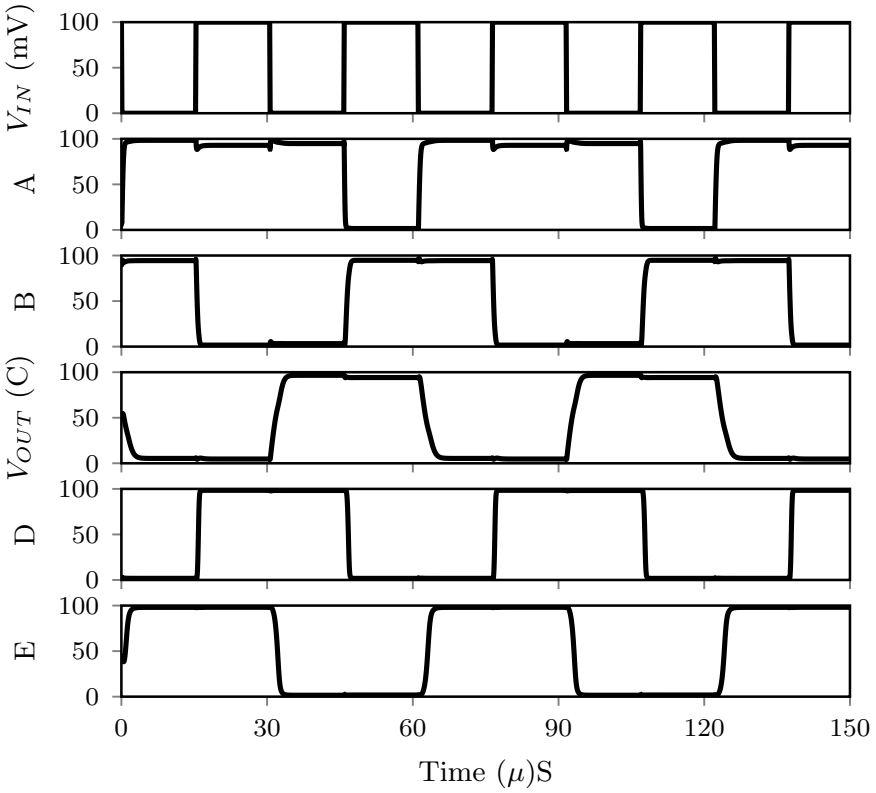
Table 7 shows the simulation results regarding power consumption, delay, and layout area of a divider by 2, by 4, a 15-stage divider, and 15-stage divider x16 (16 parallel 15-stage dividers). The ST-based FD by 2 simulations are presented in Appendix A. As mentioned before, the sliced-based circuits are faster and consume less power with a smaller layout area.

Table 7 – Simulation results of the Sliced frequency dividers, $V_{DD} = 100$ mV and $f_{in} = 32$ kHz.

Standard Cell	**Delay [μS]**	**Total Power [pW]**	**PDP [fJ]**	**Area [μm^2]**
FDby2	1.25	118.3	0.15	131.79
FDby4	2.67	229.95	0.61	263.58
FDchain15	31.95	912.91	29.16	1976.91
FDchain15x16	25.21	14615.56	368.45	31630.49

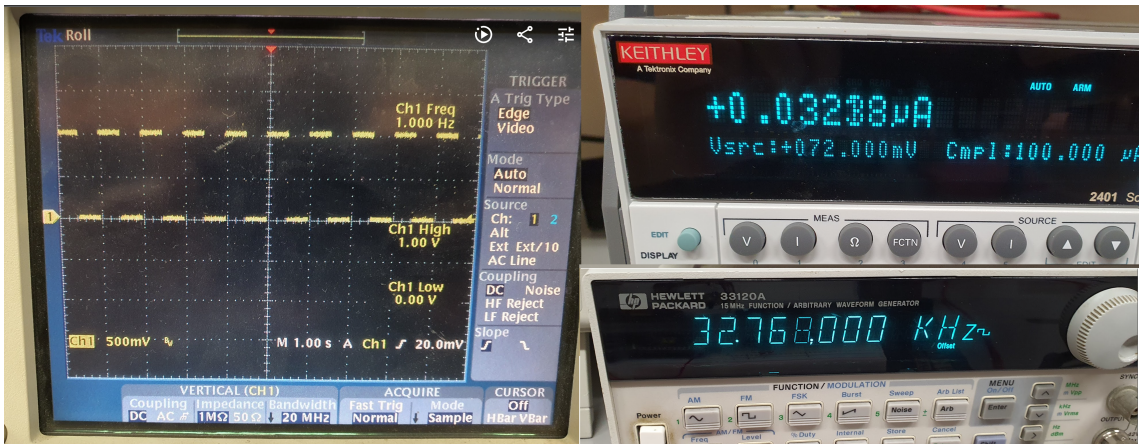
A 15-stage chain frequency divider, using the sliced-based logic, was fabricated in a 180nm CMOS technology. Figure 39 shows the output signal of the sliced frequency divider chain at 72 mV of the supply voltage. As one can see, the output signal has 1 V peak-to-peak in Figure 39, that's because a conventional level-shifter [53] was used as an auxiliary circuit for measurement purposes in this prototype.

Figure 38 – Waveforms of the Vittoz Frequency divider by 2



Source – The Author.

Figure 39 – Minimum supply voltage of the 15-stages frequency divider chain in the tapeout 2 - Sliced based logic, with 32 kHz of input frequency

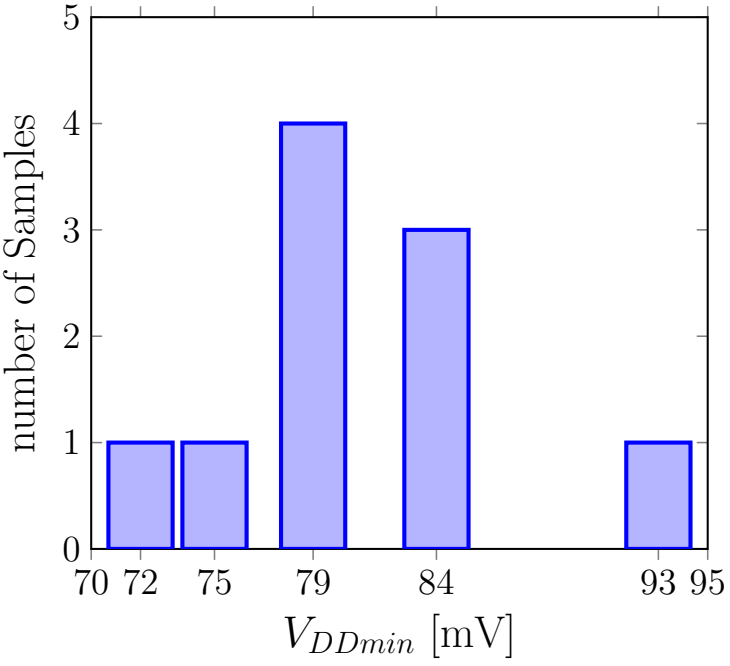


Source – The Author.

The second prototype was sent with only one 15-chain frequency divider composed of slice-based cells because there were only two pads available. Ten samples were measured, the

minimum supply voltages results are presented in Figure 40. All samples are fully functional with a V_{DDmin} = 100 mV and a maximum input frequency of 131.072 kHz (or 2^{17} kHz). All the measurements were conducted at the Integrated Circuits Laboratory of the Federal University of Santa Catarina.

Figure 40 – Minimum supply voltage of the frequency divider by 2^{15} in the tapeout 2, with 32 kHz of input frequency.



Source – The Author.

4.3 CHIP 3 - THIRD FREQUENCY DIVIDER PROTOTYPE

The Vittoz frequency divider topology implemented in the second prototype presented better results than the FD1 topology from the first prototype. Therefore, the Vittoz frequency divider topology was chosen in the third prototype, and the following circuits were implemented: a divider by four, a 15-stages frequency divider chain, and a 15-stages frequency divider chain x16 (16 parallel 15-stage dividers).

Table 8 shows the results of the 2000 samples Monte Carlo simulations with PVT variability to determine the yield of the frequency divider by 4. The definition of yield in this work is the following: if the frequency divider presents the correct output frequency, the yield will increase, thus, a yield of 100% means that all the 2000 samples are functional at the PVT corner specified. The high processing power required in time-domain simulations prevented the yield simulation of the 15 stages dividers.

The yield simulations with PVT variability considered a temperature range from 0 to 65°C and 10% variation of the nominal supply voltage, based on the work [39]. An increase

on the temperature range of the ULV-SCL demands an increase on V_{DD}, within the limits of the available technology. Other techniques that were not explored in this work, such as body biasing, can also increase the robustness of the cells to PVT variations.

The results in Table 8 show a comparison between the Sliced and ST standard cell libraries. Both libraries at nominal conditions present a 100 $\%$ yield. However, while the ST library cells are slower than the sliced cells by default, the ST cells are more appropriate for higher temperatures.

Table 8 – Results of Monte Carlo simulations across process, temperature, and supply voltage variations of a Vittoz frequency divider by four, with an input frequency of 32 kHz

Temperature [$^{\circ}C$]	**V_{DD} [mV]**	**Sliced Divider by 4 [%]**	**ST Divider by 4 [%]**
0	**90**	95	55
	100	100	75
	110	100	85
27	**90**	100	100
	100	100	100
	110	100	100
65	**90**	25	100
	100	95	100
	110	100	100

Source – The Author.

In addition, an inverter and a ROSC with the sliced and ST-based libraries were implemented to characterize the DC and dynamic characteristics of the fundamental cell of each SCL. The third prototype does not have silicon measurements because the chips did not arrive up to the submission of this dissertation.

The tapeout chip's top view, characteristics, and implemented circuits are shown in Appendix Y.

5 CONCLUSIONS AND FUTURE WORK

This dissertation presents a minimalist standard cell library operating in the ultra-low-voltage domain. The focus of the work was the development of robust logic gates through sizing and circuit topology schemes. The primary motivation to design a ULV SCL operating at $V_{DD} = 100$ mV was the reduction of power consumption that comes with the aggressive voltage scaling technique. Despite the notable power savings, the subthreshold operation has some issues regarding parameter process variability and performance.

Addressing the variability in subthreshold was the main challenge of this work. In the transistor level design, sizing and transistor association techniques were used to improve the robustness of the logic gates.

Two logic gate topologies were compared in this work, the sliced-based, and the Schmitt trigger-based cells. The post-layout electrical characterization of the standard cell library shows that the sliced-based cells have a significant improvement in power consumption, delay, and area.

The standard cell library was verified through the design of frequency dividers. The FD was simulated and fabricated in two different CMOS technologies; this circuit was chosen due to the vast application in real-time clocks and phased locked loops systems [49]. Table 9 shows a state-of-the-art comparison of ultra-low-voltage frequency dividers.

As seen in Table 9, the 72 mV sliced-based frequency divider is the lowest supply voltage for a CMOS sequential circuit. This result proves that even in a mature field like the subthreshold design, we can still push the supply voltage limit even further.

A straightforward research path is using the SCL developed in this work in a digital integrated circuit flow. Implement and test well-known circuits testbench (AES-128, ARM Cortex-M0, and a 32-bit RISC processor) [54] with the ultra-low-voltage minimalist standard cell library.

Table 9 – State-of-the-art comparison of ultra-low-voltage frequency dividers.

Standard Cell Library	**ECCTD 2015 [55]**	**NORCAS 2021 [56]**	**First Prototype**	**Second Prototype**	**Third Prototype***
Technology [nm]	65	130	130	180	180
Transistor type	LVT and SVT	HVT	LVT	MVT	MVT
Logic Style	Sliced	CMOS Conventional	Schmitt-Trigger† CMOS Conventional‡	Sliced	ST-Sliced†† Sliced‡‡
FF Topology	Nand-based FF	Nand-based FF	DFF1	Vittoz race-free FD	Vittoz race-free FD
FD architecture	Divide by 3	Divide by 3	divide by 2^{15}	divide by 2^{15}	divide by 4
Cell Height [um]	3.89	6.15	5.14	7.52	7.52
$\boldsymbol{V_{DDmin}[mV]}$	132	135	76	72	60 †† 73‡‡
Maximum frequency	∼40 kHz @ 132 mV	∼1 MHz @ 150mV	262 kHz @ 110 mV† 1 MHz @ 140 mV‡	131 kHz @ 100 mV 800 kHz @ 150 mV	64 kHz @ 100mV†† 350 kHz @ 100mV‡‡ 1 MHz @ 150mV‡‡

* Only simulated: $27°C$, TT corner.
† Schmitt-trigger logic.
‡ Conventional logic.
†† ST-Sliced logic.
‡‡ Sliced logic.

Source – The Author.

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APPENDIX A – SIMULATIONS RESULTS OF THE ST-SLICED BASED SCL IN 180 NM TECHNOLOGY.

Table 10 – Simulation results of the Schmitt trigger-based standard cell library in 180 nm technology.

Standard Cell	Delay [μS]	Total Power [pW]	PDP [fJ]	Area [μm^2]
Inverter	1.66	48.5	0.08	66.8
Inverterx16	2.29	732.6	1.68	1070.5
NAND	1.66	48.5	0.08	66.8
NANDx16	2.29	732.6	1.68	1070.5
NOR	1.66	48.5	0.08	66.8
NORx16	2.29	732.6	1.68	1070.5
OAI21	1.66	48.5	0.08	66.8
OAI21x16	2.29	732.6	1.68	1070.5
AOI21	1.66	48.5	0.08	66.8
AOI21x16	2.29	732.6	1.68	1070.5
AOI22	1.66	48.5	0.08	66.8
AOI22x16	2.29	732.6	1.68	1070.5
DFF1	14.94	1011.4	15.11	9557.07
DFF2	3.43	219.8	0.55	267.1
FD2	2.79	419.9	1.17	333.8
FD4	4.82	514.1	2.51	667.7
FD15	35.9	5134.1	184.8	5007.6
FD15x16	462.9	66039.1	30596.5	80120.9

Source – The Author.

APPENDIX B – 130 NM STANDARD CELL LIBRARY

The 130 nm standard cell library sizing strategies are the same presented in section 2.3 and section 3.2.

The dimensions for a perfect balance VTC of a inverter using low-threshold voltage transistors (LVT) in the 130 nm technology are: W_N/L_N = 300 nm /300 nm and W_P/L_P = 1.5 μm /300 nm. Table 11 presents the ST-based inverter dimensions.

Table 11 – ST inverter dimensions.

PMOS Network	NMOS Network
$W_{P0} = 3\mu m$	$W_{N0} = 600nm$
$L_{P0} = 300nm$	$L_{N0} = 300nm$
$W_{P1} = 1.5\mu m$	$W_{N1} = 300nm$
$L_{P1} = 300nm$	$L_{N1} = 300nm$
$W_{P2} = 1.5\mu m$	$W_{N2} = 300nm$
$L_{P2} = 300nm$	$L_{N2} = 300nm$

As noted in [39], the I_{on}/I_{off} ratio, where I_{on} is the active current and I_{off} is the leakage current, is severely degraded for low supply voltages, with a severe risk to the correct operation of the logic gates. One primary strategy to mitigate the reduction in I_{on}/I_{off} is to avoid gates with more than three inputs. Consequently, to improve the operation at ULV and reduce the design effort, we designed only a small library with two input NAND and NOR gates and a D flip-flop.

Table 12 presents the NAND(NOR) transistors dimensions in 130 nm technology. The transistors sizes of the NAND-ST and NOR-ST gates are indicated in Figure 41 . The transistors were sized to keep the worst-case pull-up and current pull-down strengths of the NAND(NOR) equal to those of the inverter.

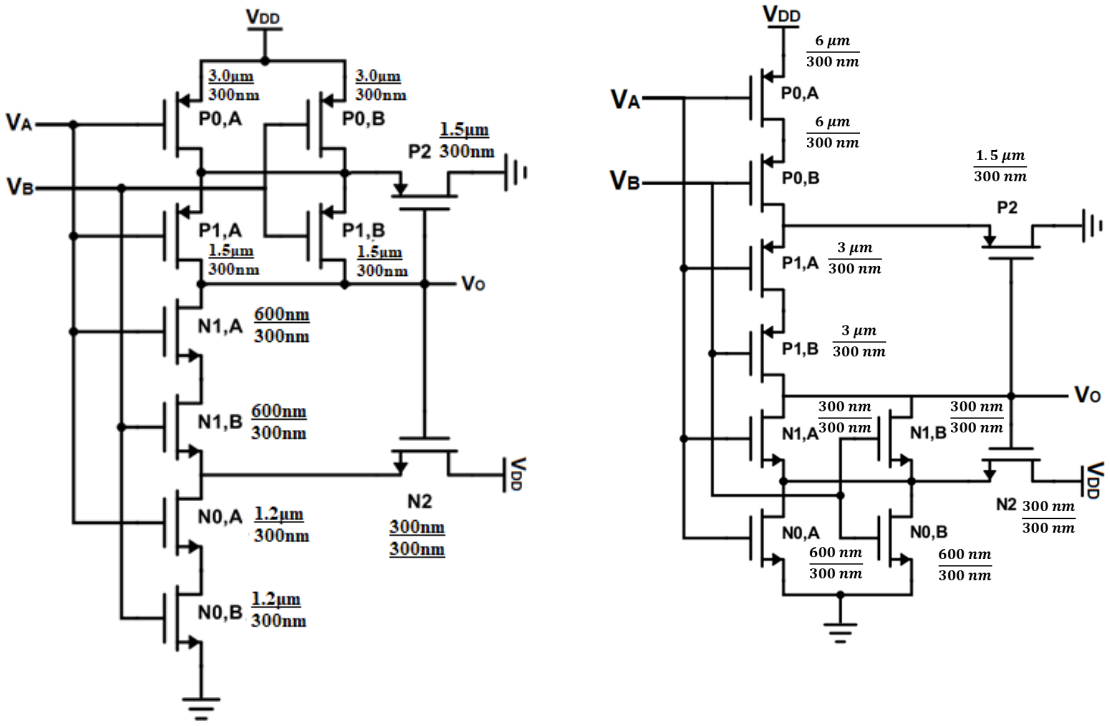
Table 12 – NAND and NOR dimensions in 130 nm technology.

NAND	NOR
$W_P = 1.5\mu m$	$W_P = 3\mu m$
$L_P = 300nm$	$L_P = 300nm$
$W_N = 600\mu m$	$W_N = 300nm$
$L_N = 300nm$	$L_N = 300nm$

Table 13 compares values of delay, power and area of the classical logic and ST logic in 130 nm technology.

Figure 41 – Schematic and dimensions of the ST logic gates in 130 nm technology.

(a) NAND-ST. (b) NOR-ST.

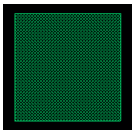
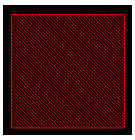
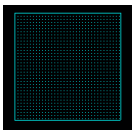
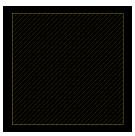
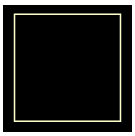
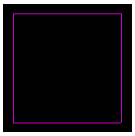
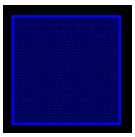
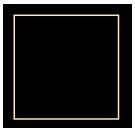
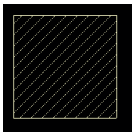


Source – The Author.

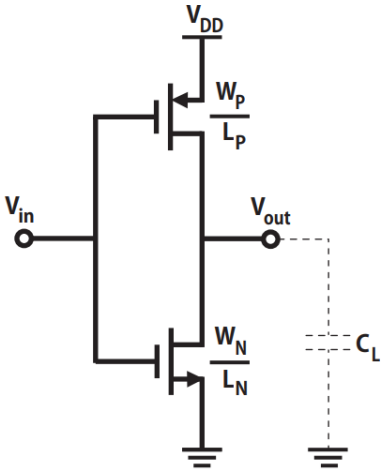
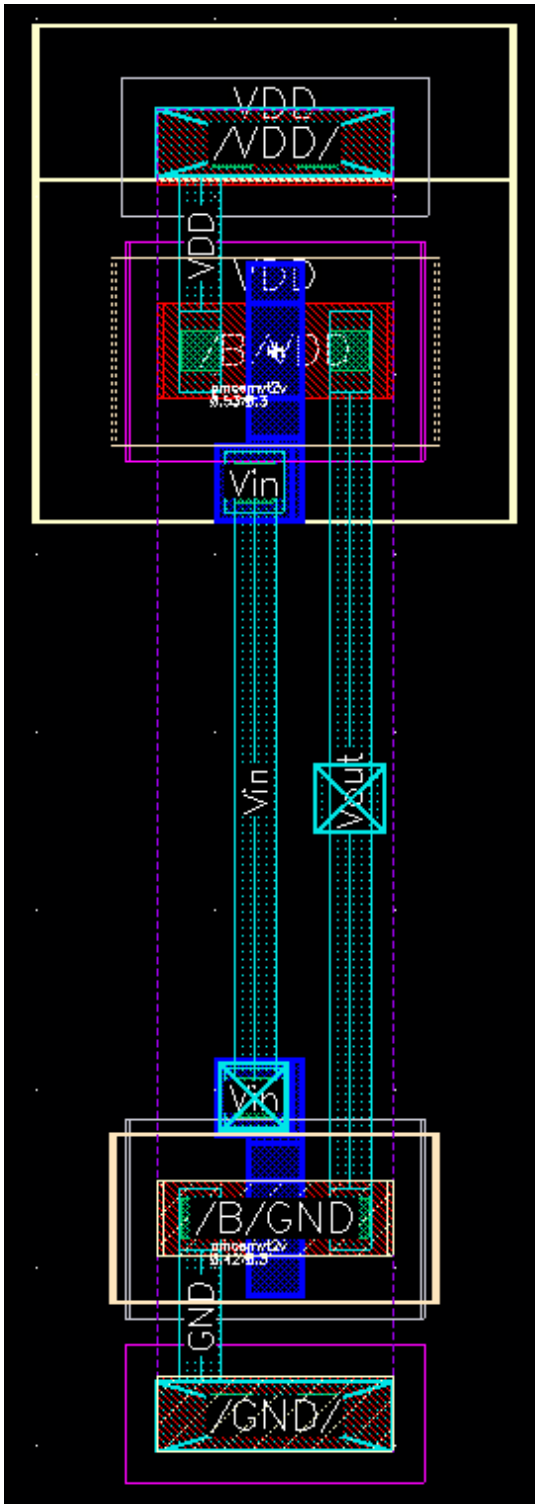
Table 13 – Simulated Comparison of delay, total power and area of the classical and ST logic for $V_{DD} = 90$ mV.

Logic cell	Delay [ns]	Power [nW]	Area [μm^2]
INV	6.76	0.34	14.08
INV-ST	51.34	0.93	36.90
NAND	9.02	0.57	19.61
NAND-ST	54.01	1.57	57.61
NOR	17.9	0.54	25.7
NOR-ST	101.2	1.49	80.19
Divides chain	544.55	98.25	4125.14
Divider chain - ST	6906.44	346.80	12986.31

APPENDIX C – LAYOUT INFORMATION

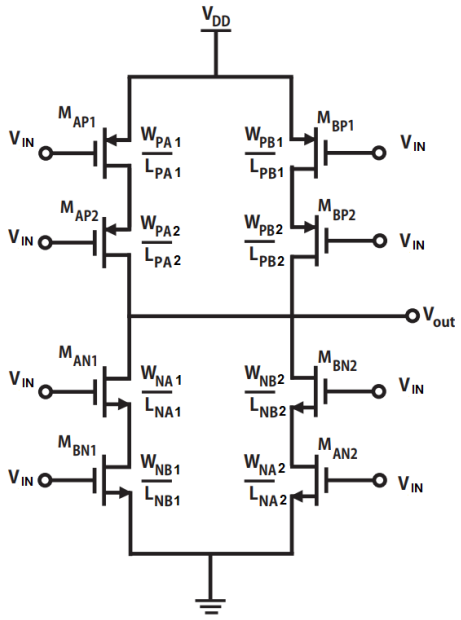
Layer	Name	Description
	Contact	Contact hole between M1 and poly/oxide
	DIFF	Diffusion area
	M1	First metal for interconnection
	M2	Second metal for interconnection
	M1pin	First metal pin
	NIMP	N+ implantation
	NWELL	N-Well
	PIMP	P+ implantation
	POLY	Polysilicon
	VTM-N	NMOS V_T implantation
	VTM-P	pMOS V_T implantation
	WELLBODY	pMOS V_T Deep N-Well

APPENDIX D – CMOS INVERTER SCHEMATIC AND LAYOUT

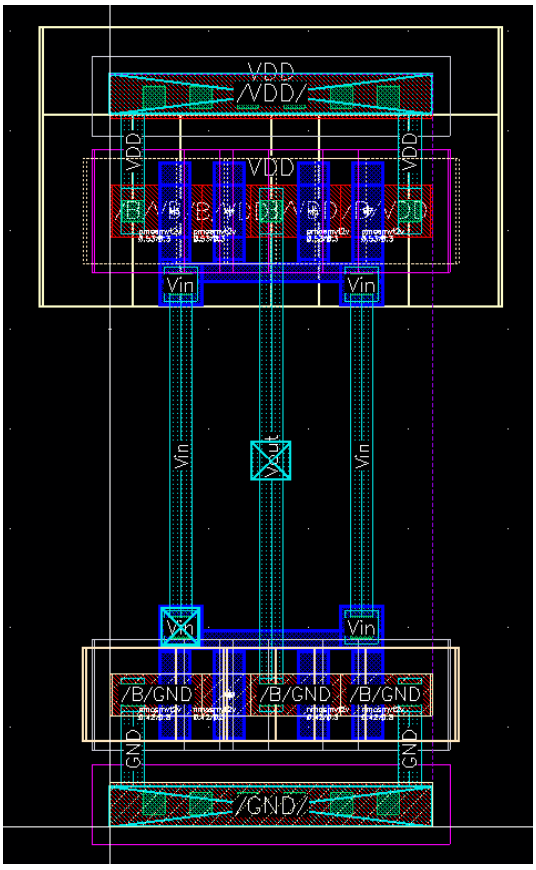
Schematic	Layout
	

APPENDIX E – CMOS INVERTER-SLICED SCHEMATIC AND LAYOUT

Schematic

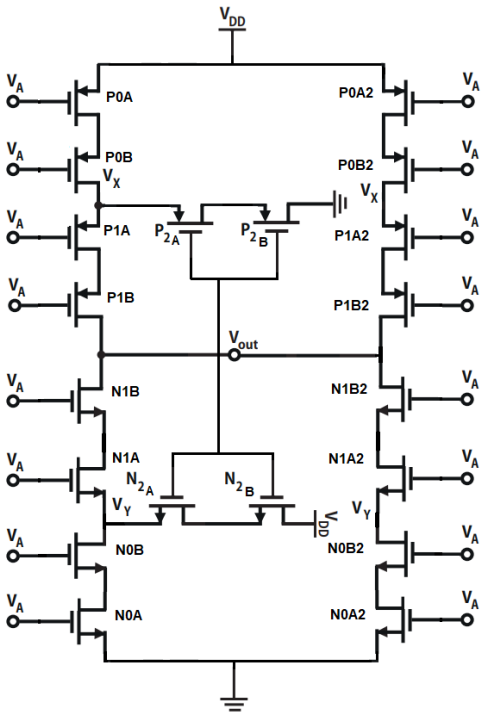


Layout

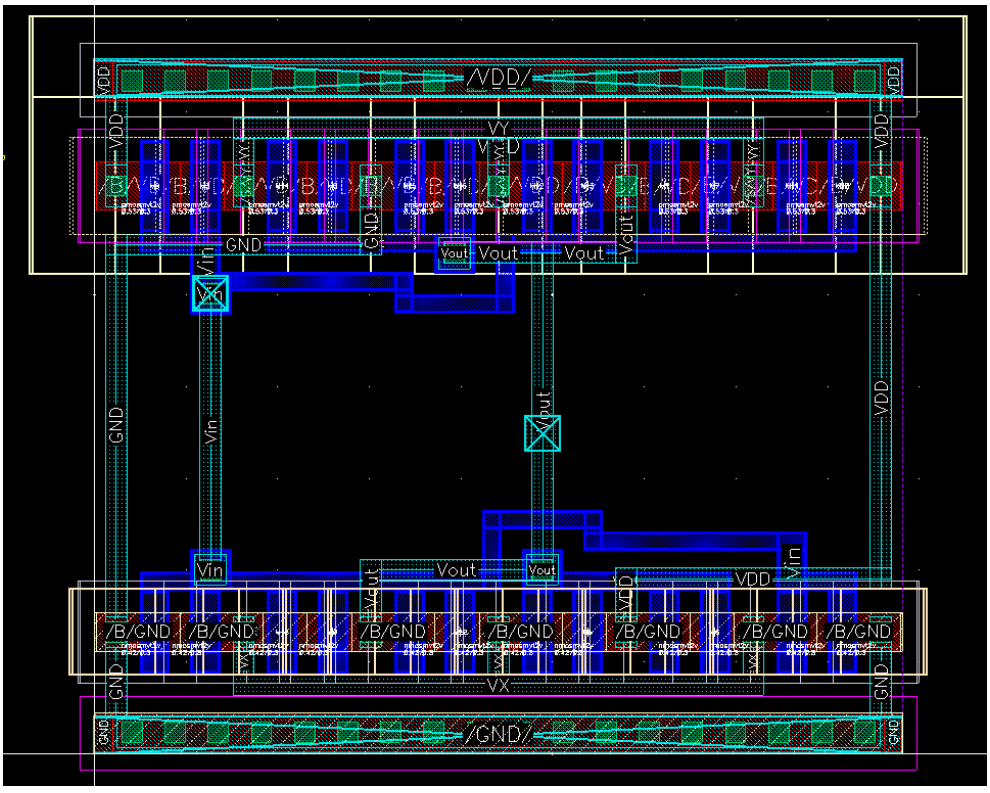


APPENDIX F – CMOS INVERTER-ST SCHEMATIC AND LAYOUT

Schematic

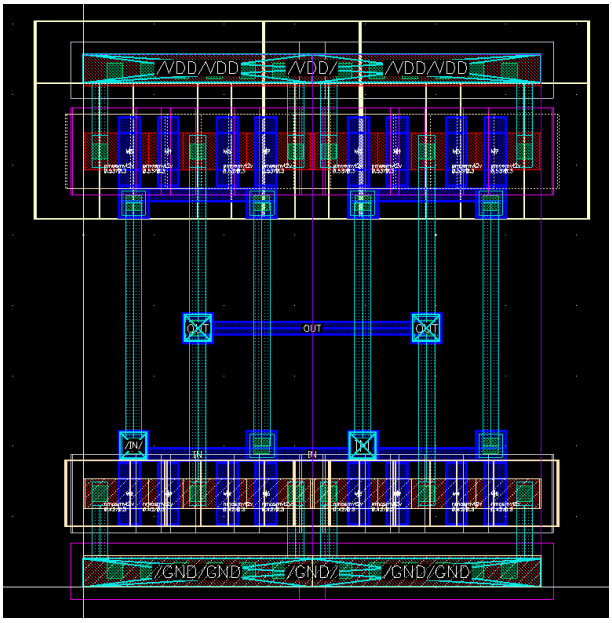


Layout

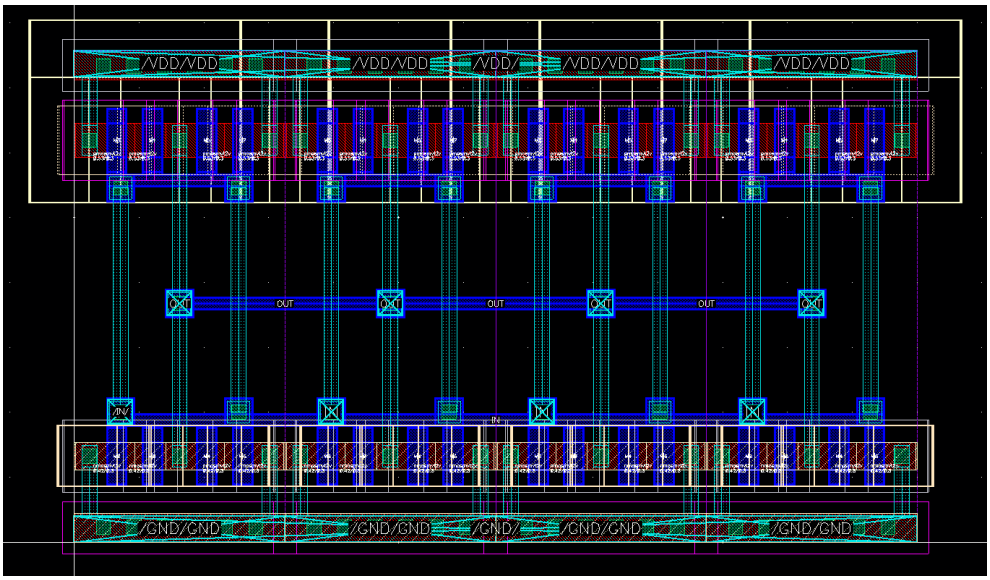


APPENDIX G – CMOS INVERTER-SLICED X2 AND X4 LAYOUTS

Layout - Inverter-Sliced x2

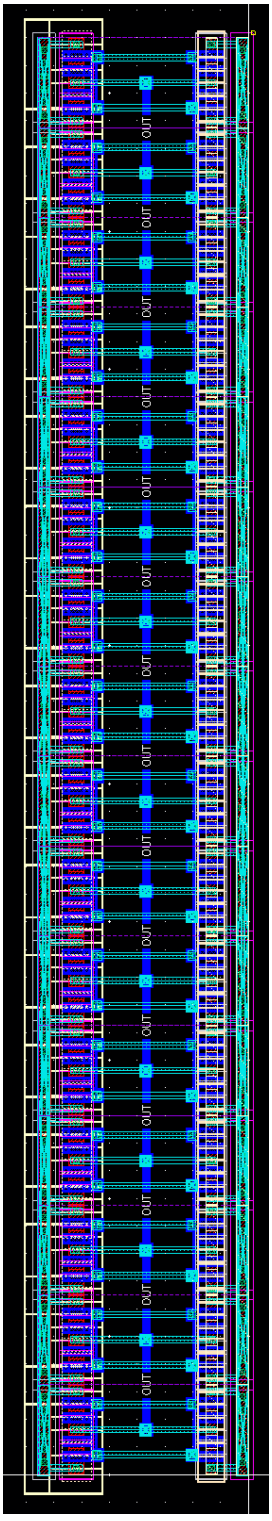


Layout - Inverter-Sliced x4



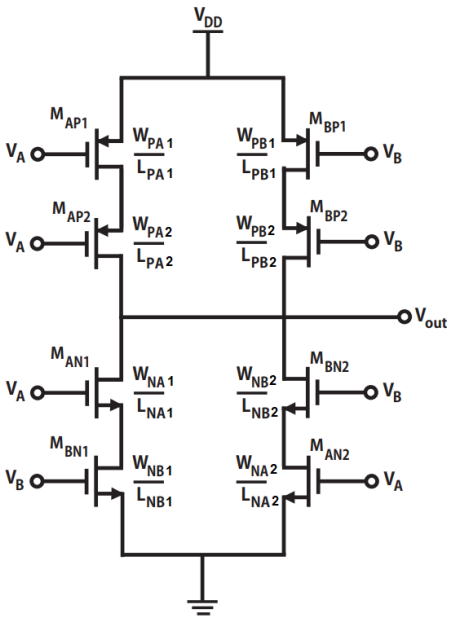
APPENDIX H – CMOS INVERTER-SLICED X16 LAYOUT

Layout - Inverter-Sliced x16

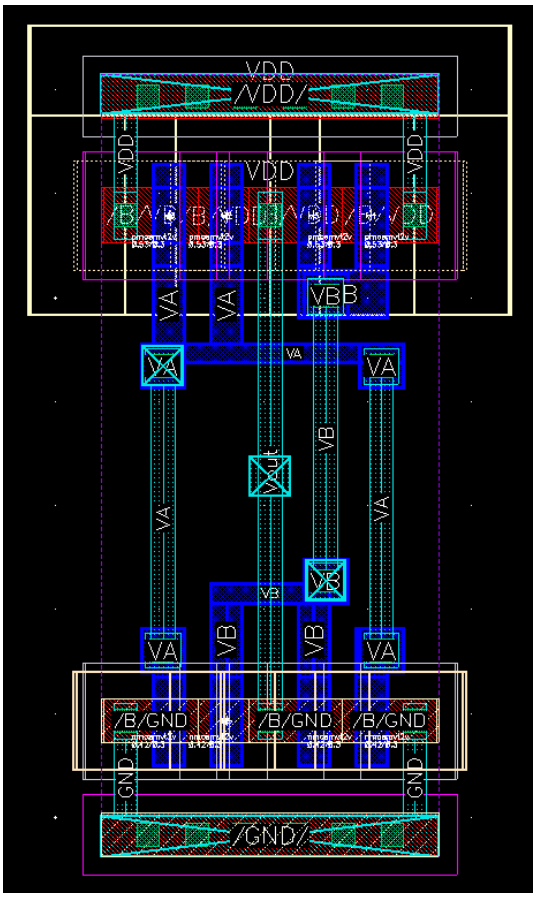


APPENDIX I – CMOS NAND-SLICED SCHEMATIC AND LAYOUT

Schematic

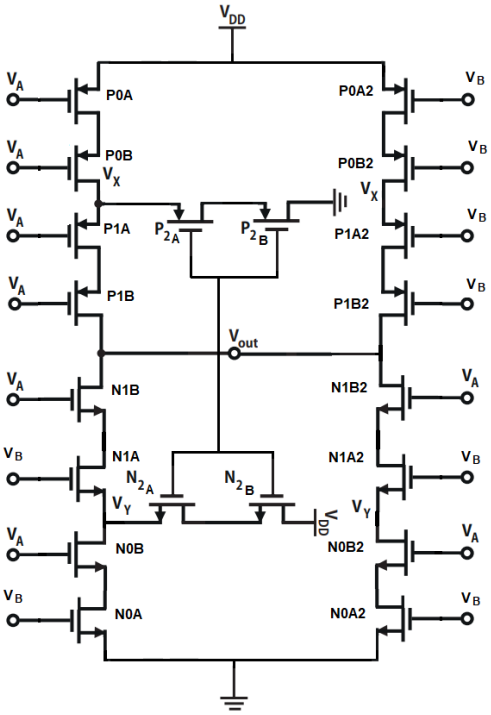


Layout

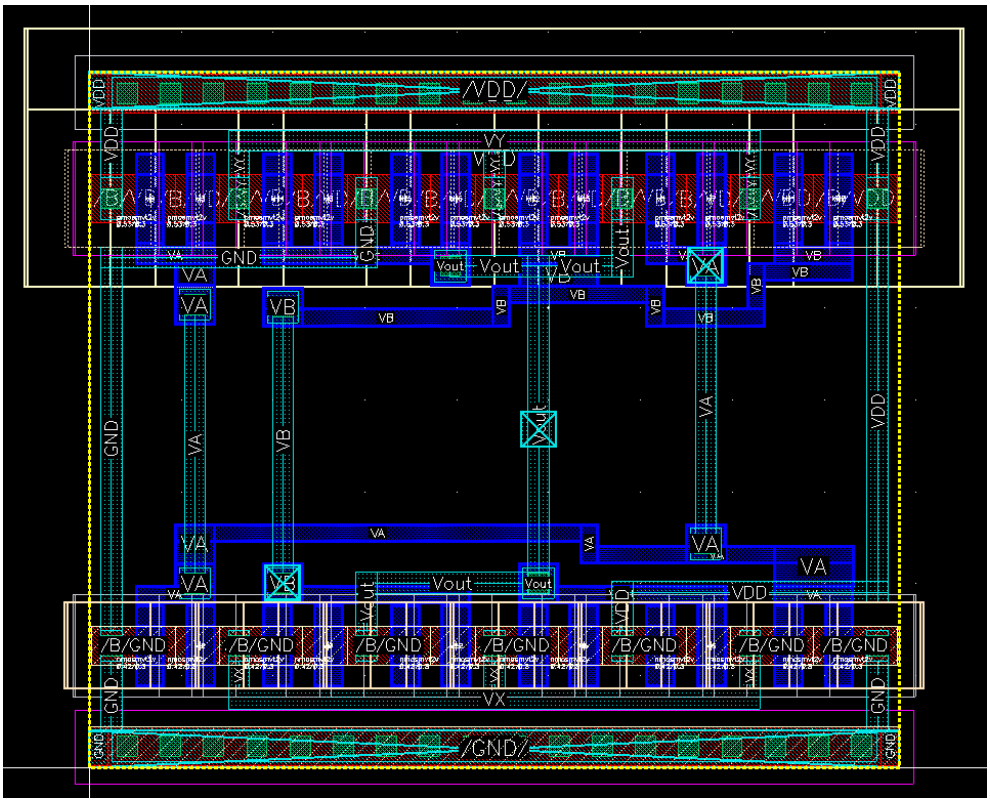


APPENDIX J – CMOS NAND-ST SCHEMATIC AND LAYOUT

Schematic

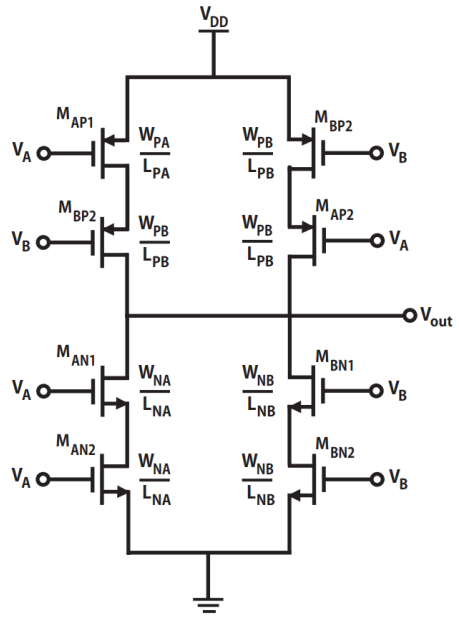


Layout

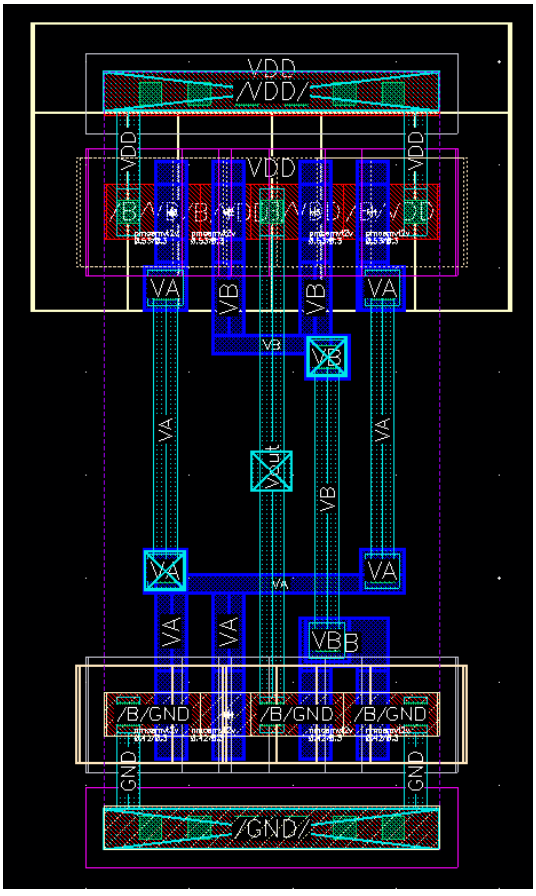


APPENDIX K – CMOS NOR-SLICED SCHEMATIC AND LAYOUT

Schematic

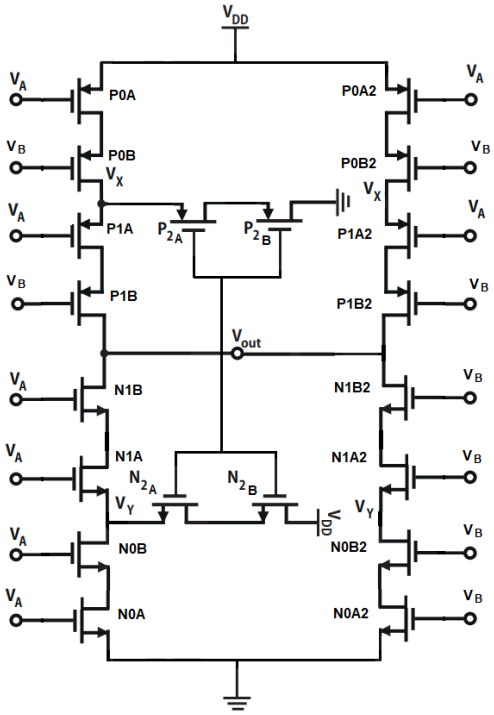


Layout

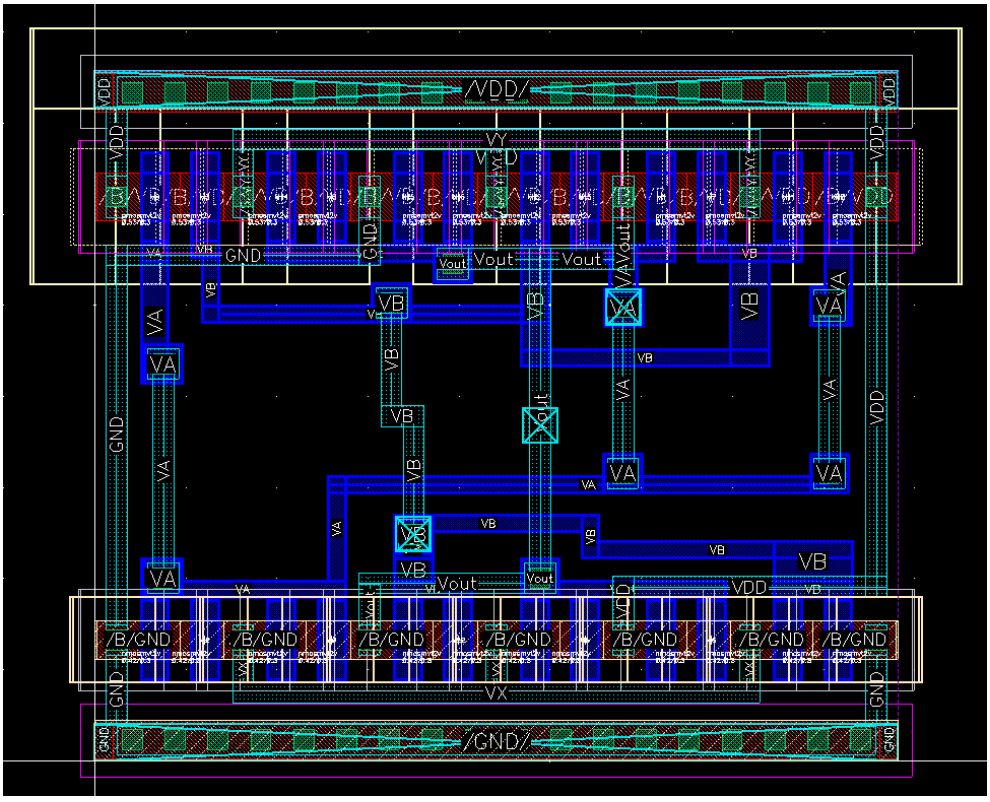


APPENDIX L – CMOS NOR-ST SCHEMATIC AND LAYOUT

Schematic

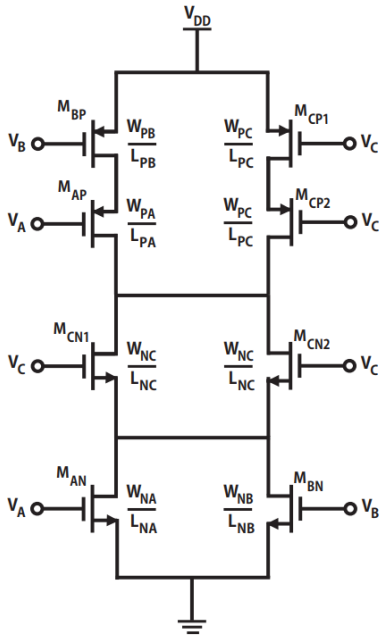


Layout

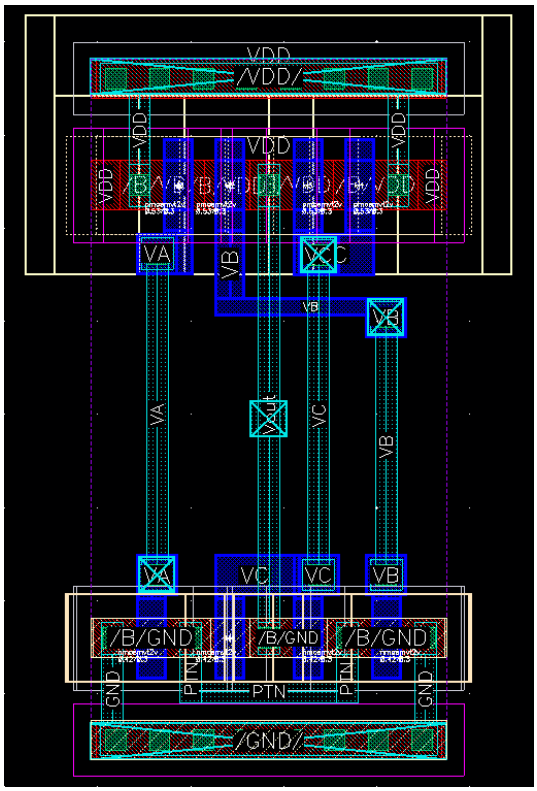


APPENDIX M – CMOS OAI21-SLICED SCHEMATIC AND LAYOUT

Schematic

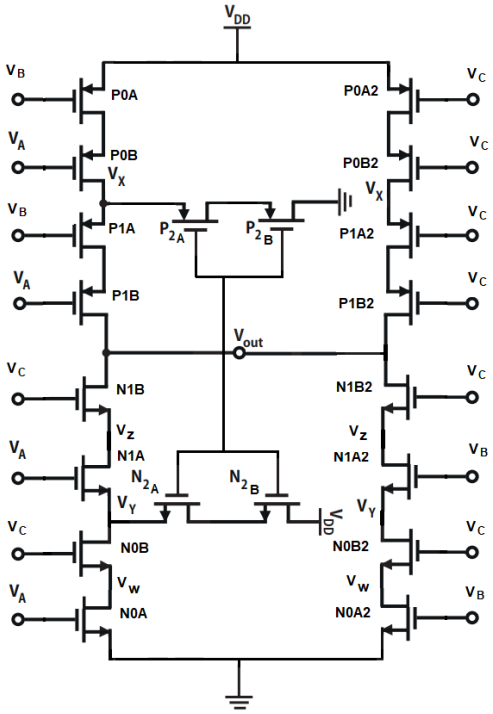


Layout

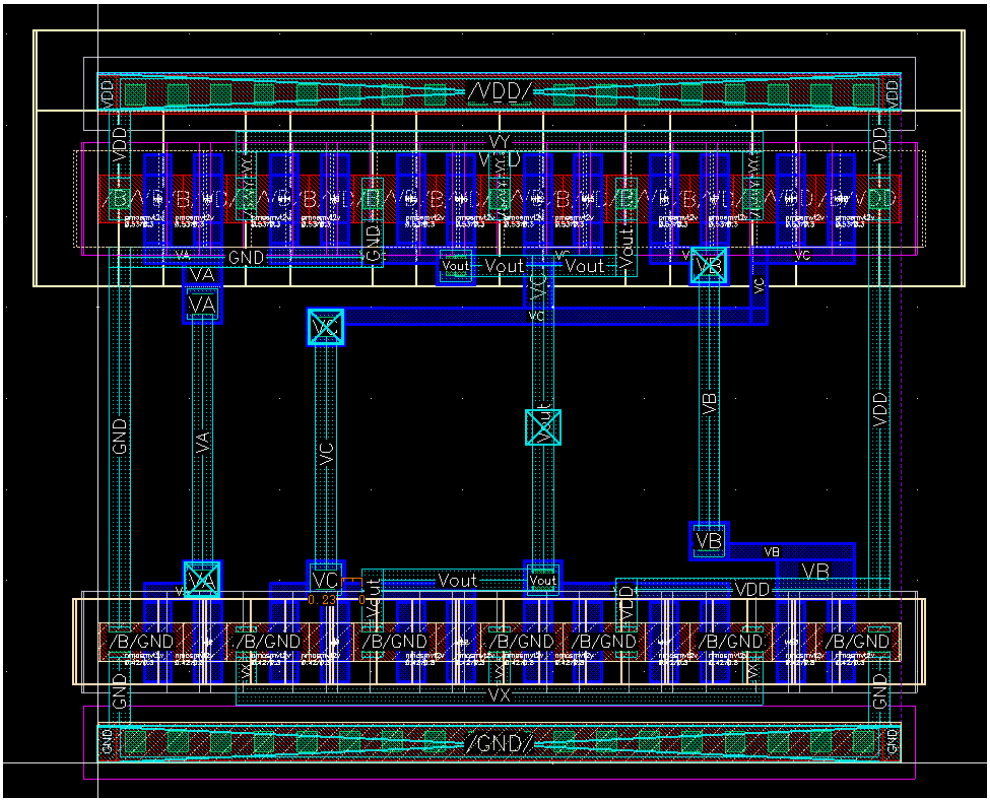


APPENDIX N – CMOS OAI21-ST SCHEMATIC AND LAYOUT

Schematic

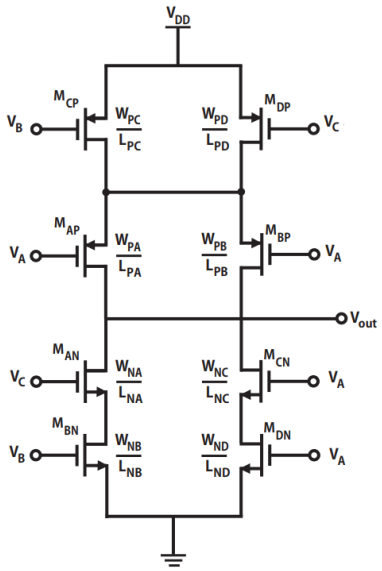


Layout

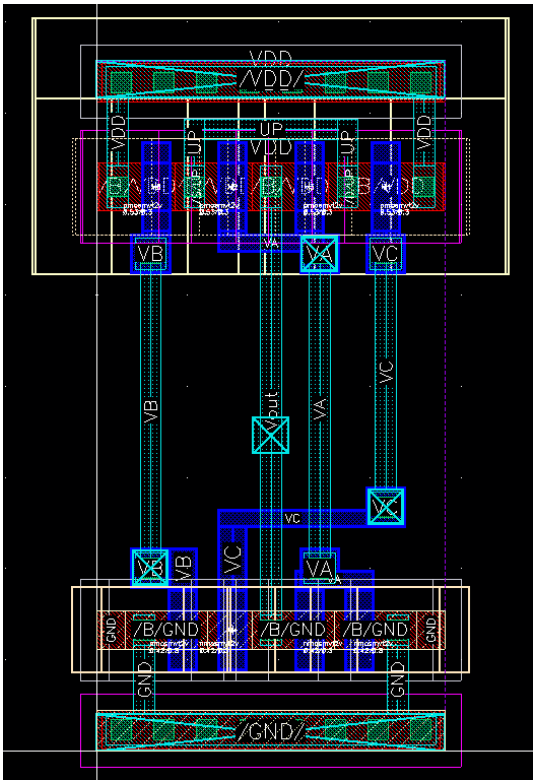


APPENDIX O – CMOS AOI21-SLICED SCHEMATIC AND LAYOUT

Schematic

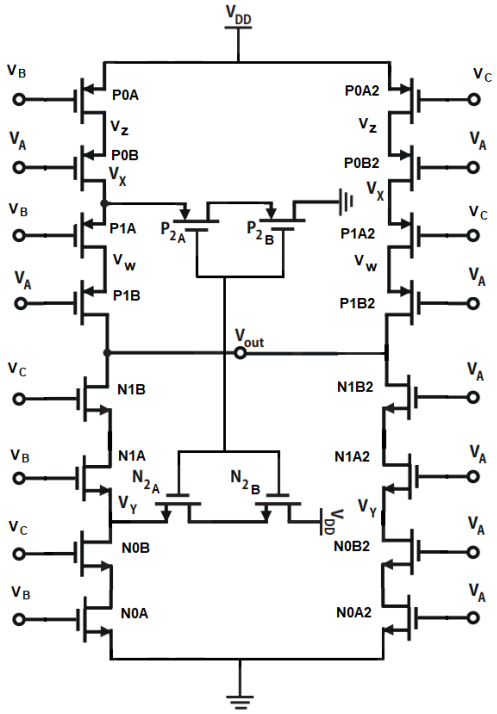


Layout

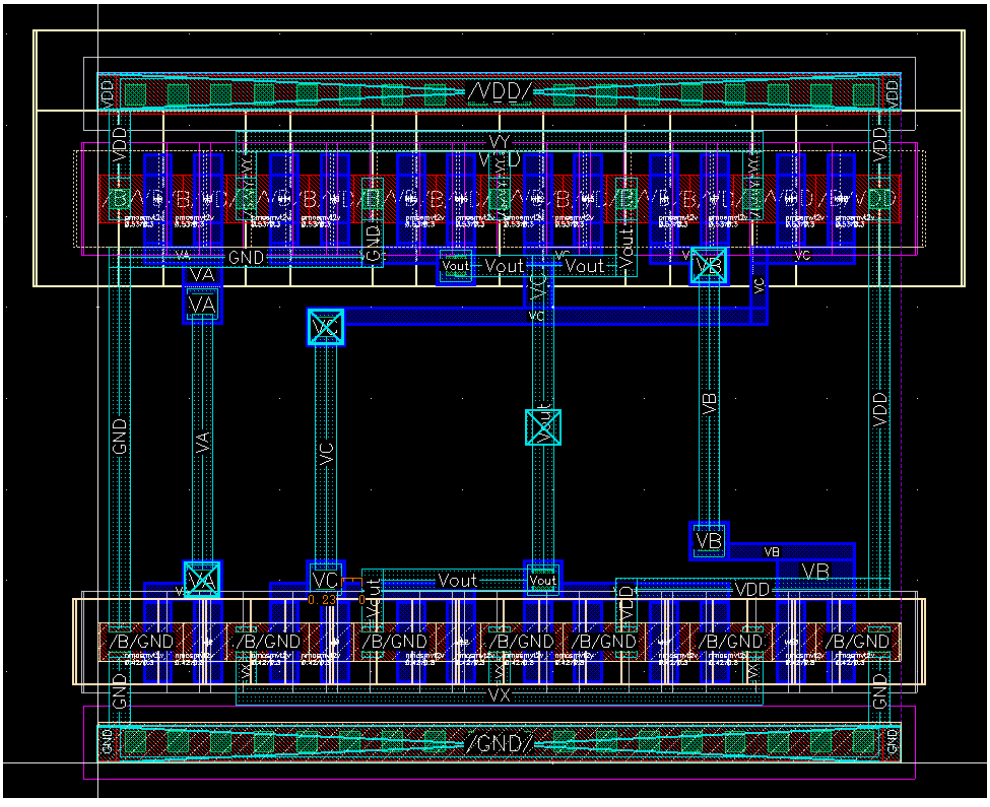


APPENDIX P – CMOS AOI21-ST SCHEMATIC AND LAYOUT

Schematic

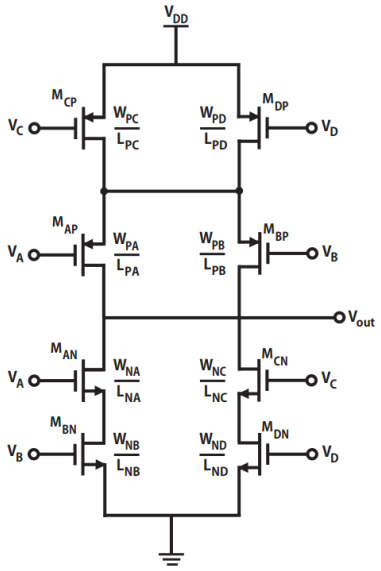


Layout

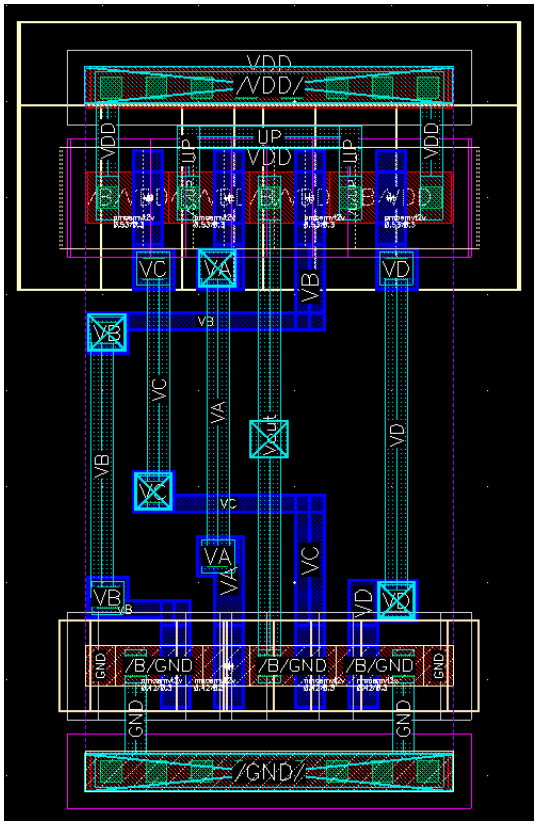


APPENDIX Q – CMOS AOI22-SLICED SCHEMATIC AND LAYOUT

Schematic

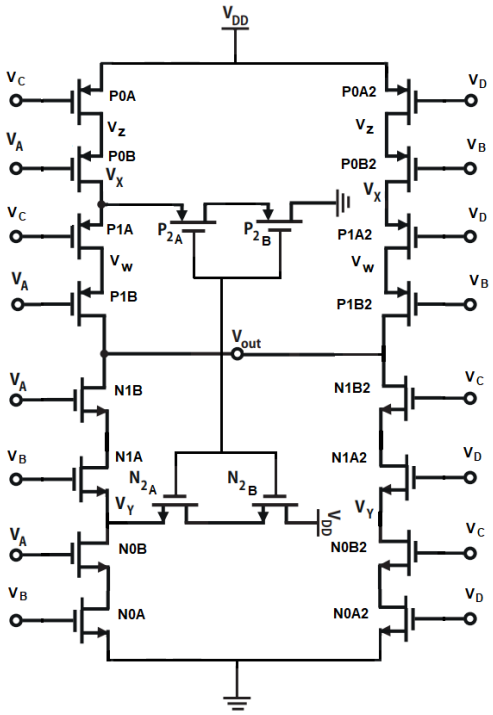


Layout

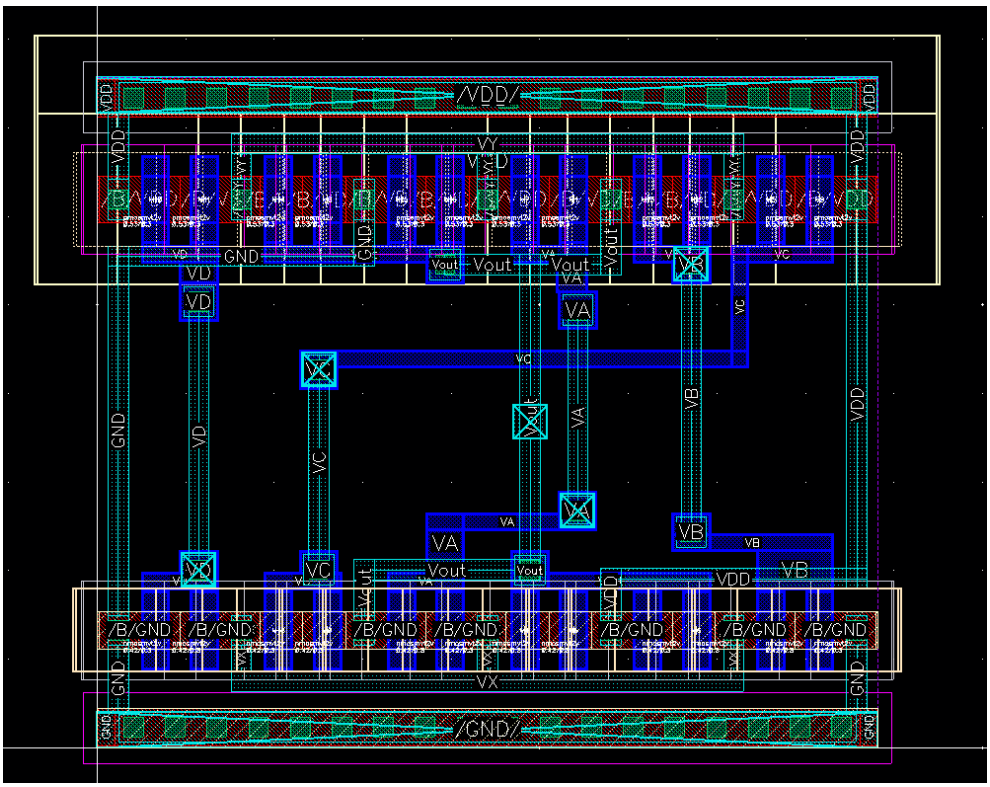


APPENDIX R – CMOS AOI22-ST SCHEMATIC AND LAYOUT

Schematic

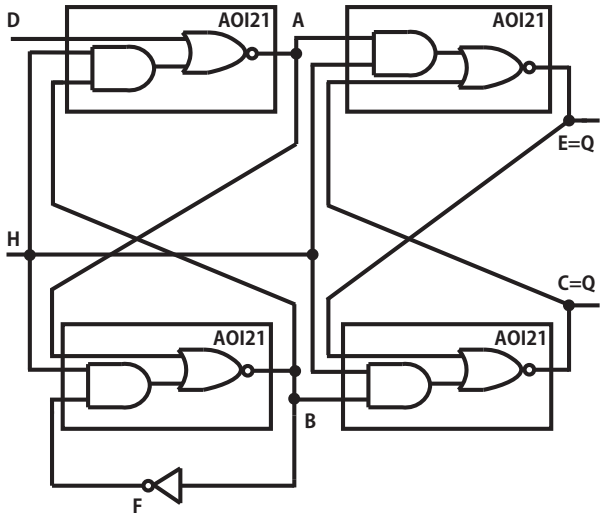


Layout

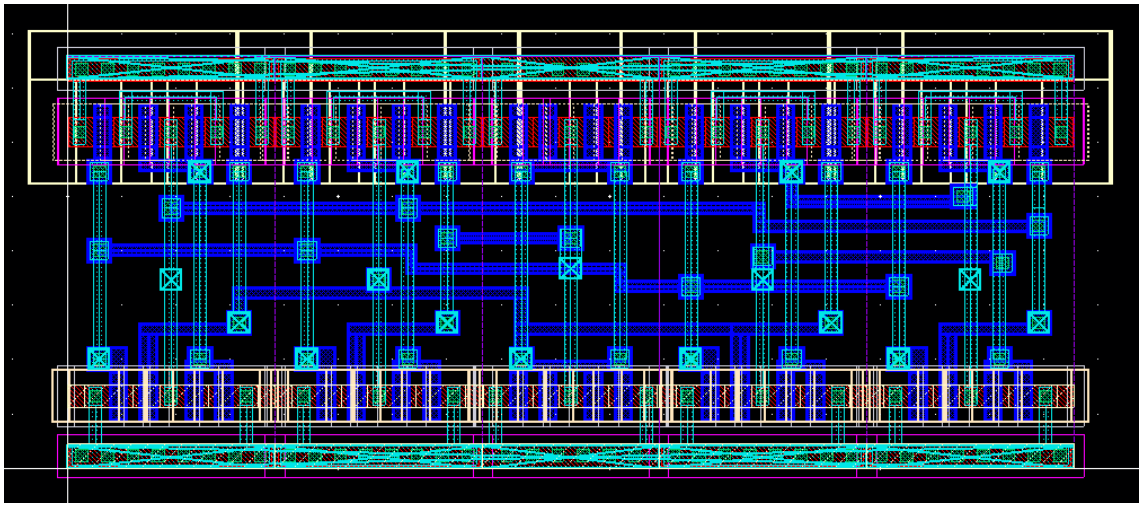


APPENDIX S – CMOS DFF-SLICED SCHEMATIC AND LAYOUT

Schematic

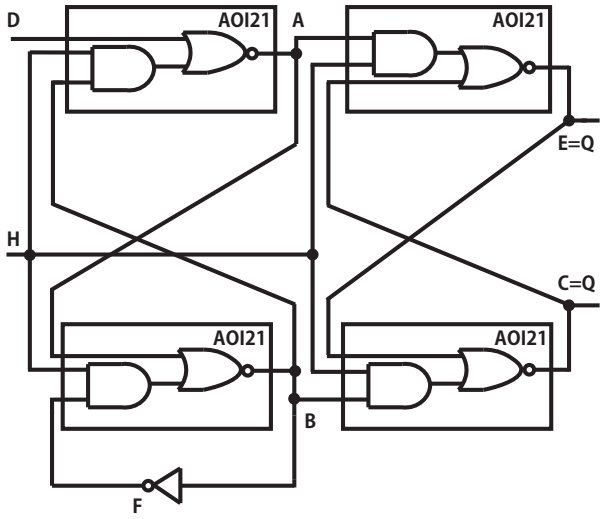


Layout

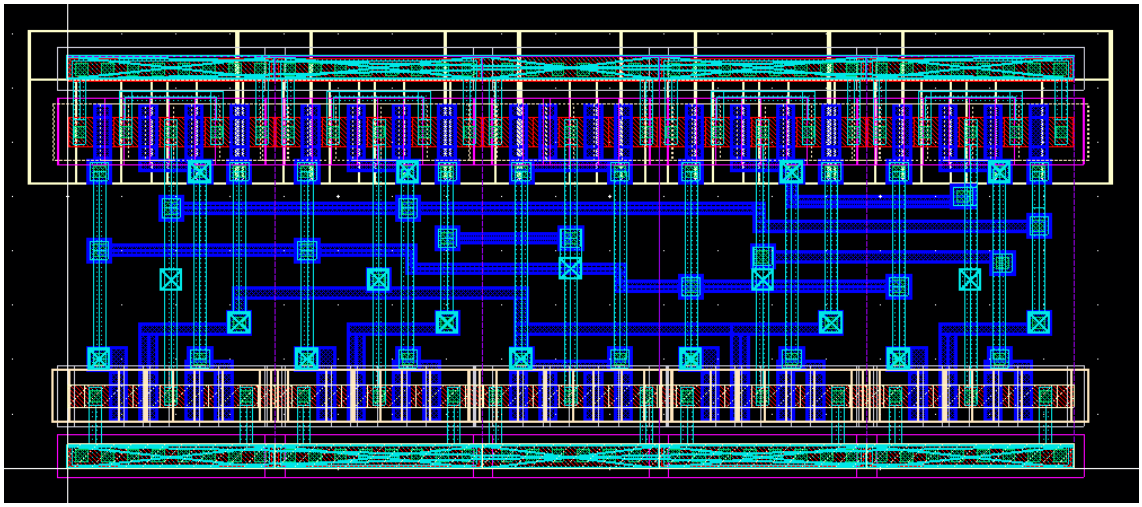


APPENDIX T – CMOS DFF-ST SCHEMATIC AND LAYOUT

Schematic

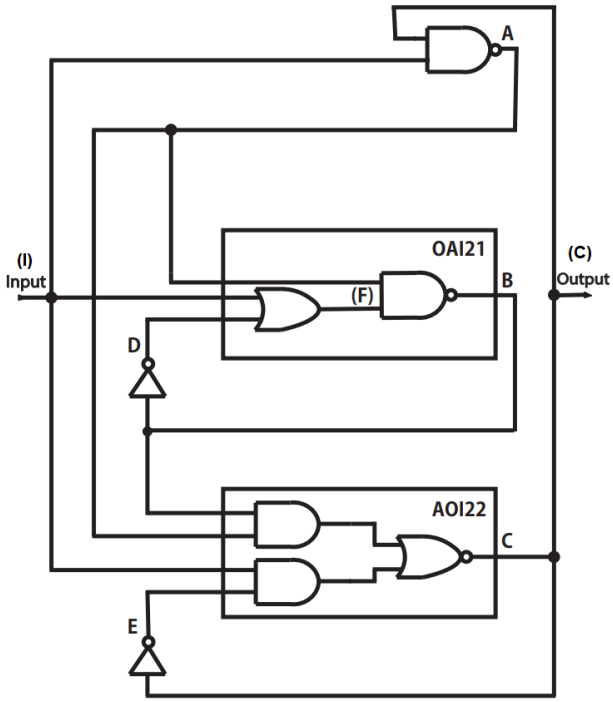


Layout

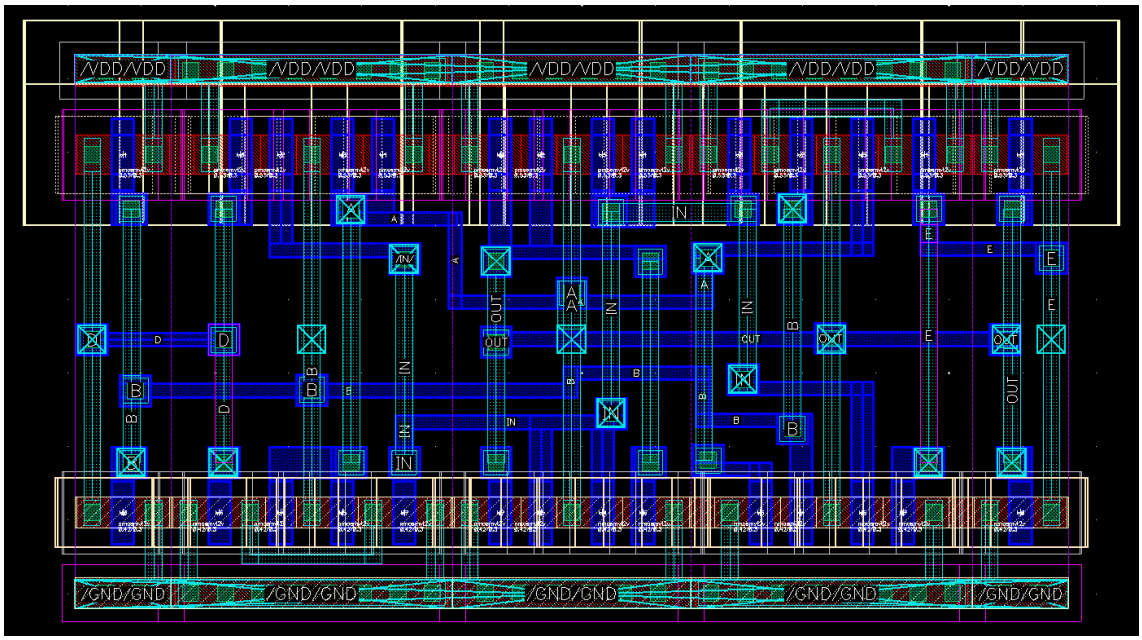


APPENDIX U – VITTOZ SLICED FREQUENCY DIVIDER BY 2 SCHEMATIC AND LAYOUT

Schematic

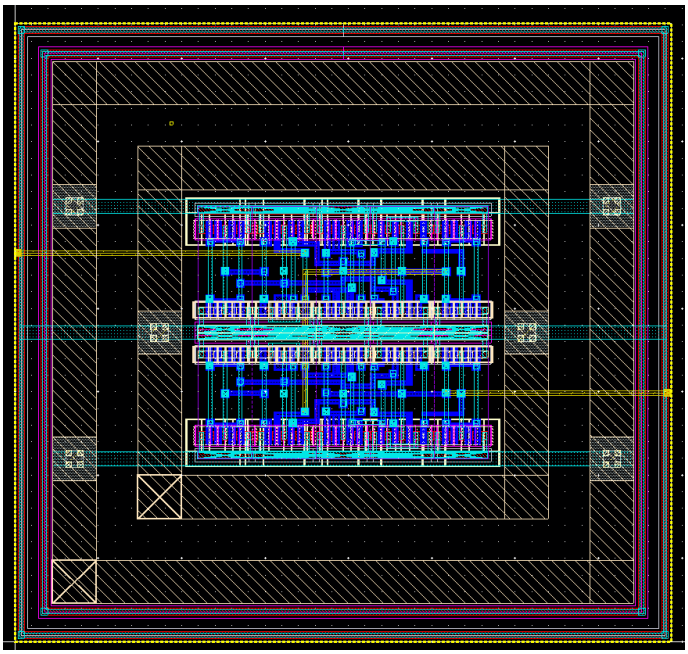


Layout

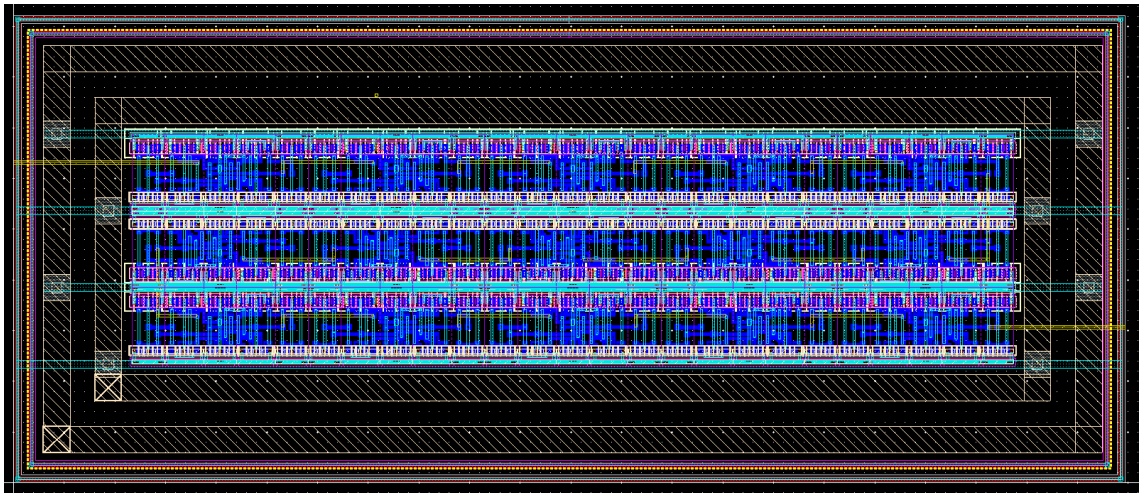


APPENDIX V – VITTOZ SLICED FREQUENCY DIVIDER BY 4 AND 15 STAGES FREQUENCY DIVIDER CHAIN LAYOUTS

Layout

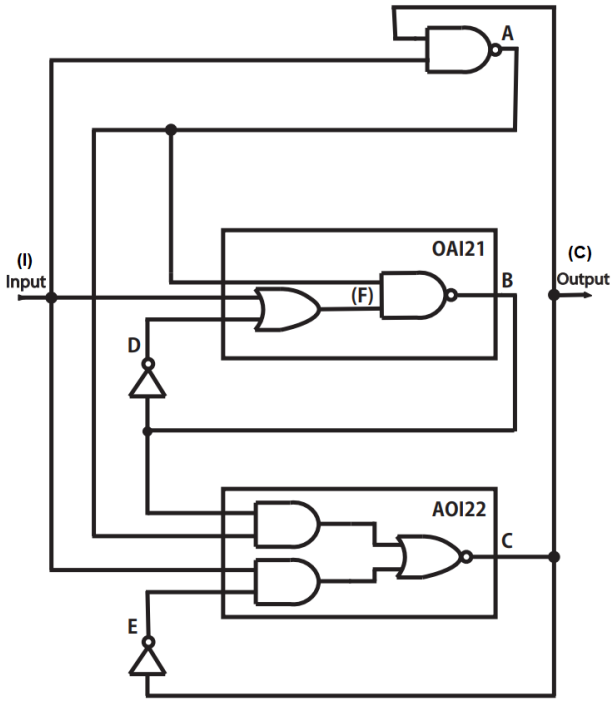


Layout

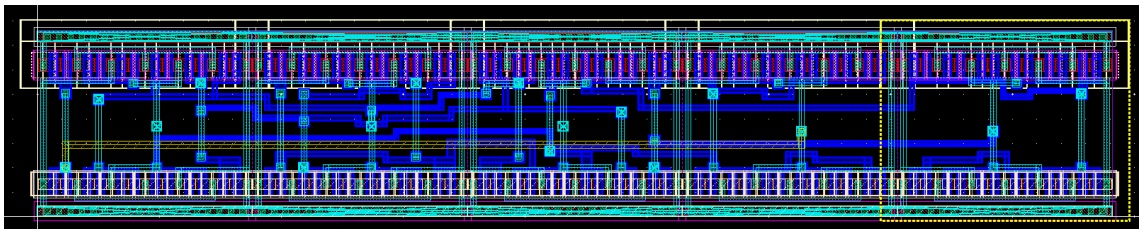


APPENDIX W – VITTOZ ST FREQUENCY DIVIDER BY 2 SCHEMATIC AND LAYOUT

Schematic

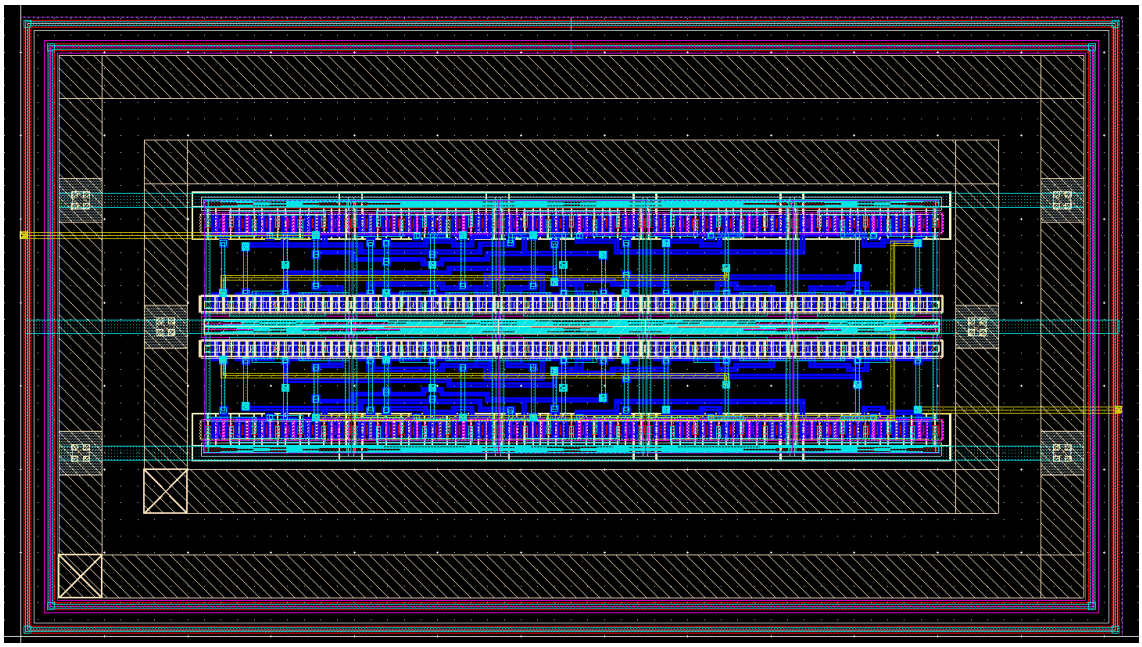


Layout

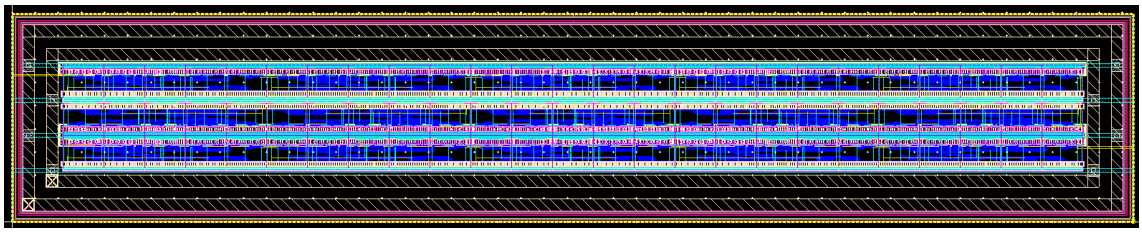


APPENDIX X – VITTOZ ST FREQUENCY DIVIDER BY 4 AND 15 STAGES FREQUENCY DIVIDER CHAIN LAYOUTS

Layout

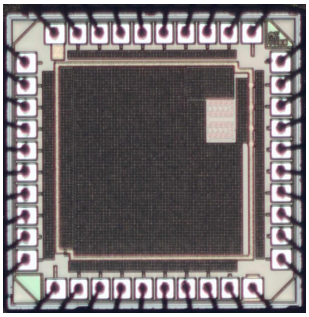
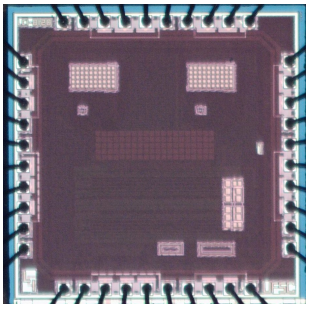
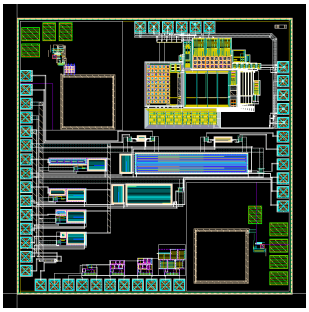


Layout



APPENDIX Y – DESIGNED CHIPS

Table 14 – Chips designed during the master's research.

Chips Topview	Characteristics	Implemented Circuits
	**Chip 1** **Submitted:** Nov. 2017 **Technology:** 130 nm **Die area:** 2.4 mm^2 **Package:** DIP40 **Status:** Arrived at LCI	Standard and ST Logic: Inverter NAND 15 stages frequency divider
	**Chip 2** **Submitted:** Fev. 2020 **Technology:** 180 nm **Die area:** 3.0 mm^2 **Package:** DIP40 **Status:** Arrived at LCI	Sliced Logic: 15 stages frequency divider
	**Chip 3** **Submitted:** May 2021 **Technology:** 180 nm **Die area:** 3.0 mm^2 **Package:** CLCC68 **Status:** Send by the foundry	Sliced and ST Logic: Inverter Ring oscillator Frequency divider by 4 15 stages frequency divider

ANNEX A – PARAMETER EXTRACTION

The 4-parameter model is only completely functional when using the correct parameters. Therefore, it is appropriate to learn how to determine the four parameters.

Laboratory experiments use parameter extraction methods commonly for the electrical characterization of electronic devices. Reproducing these methods in simulators makes the extraction procedure viable when a test chip is unavailable.

A.1 EXTRACTION OF THRESHOLD VOLTAGE (V_{T0}), SPECIFIC CURRENT (I_S) AND SLOPE FACTOR (n)

The values of the threshold voltage (V_{T0}), specific current (I_S) and slope factor (n) are extracted based on the g_m/I_D method [57], which is given by:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{dln(I_D)}{dV_G} = \frac{2}{n\phi_t(\sqrt{1+i_f}+\sqrt{1+i_r})} \tag{33}$$

For V_{DS} lower than the thermal voltage, in the linear region ($if \approx ir$) equation (34) is reduced to:

$$\frac{g_m}{I_D} \cong \frac{1}{n\phi_t\sqrt{1+i_f}} \tag{34}$$

Thus, if we neglect the variation of the slope factor n with the gate voltage, the channel is under the threshold condition ($i_f \approx i_r = 3$) when the transconductance-to-current ratio g_m/I_D is at half its maximum value. Consequently, we have a direct method that allows us to determine the threshold voltage and the specific current from the g_m/I_D curve in the linear region.

The effect of a non-zero drain-to-source voltage can be included to improve the accuracy. For $V_{DS} = \phi_t/2$ and $i_f = 3$ we obtain $i_r = 2.12$ from equation (35). For this value of i_r, V_T is the gate voltage for which g_m/I_D=0.531$(g_m/I_D)_{max}$ and I_D =0.88I_S.

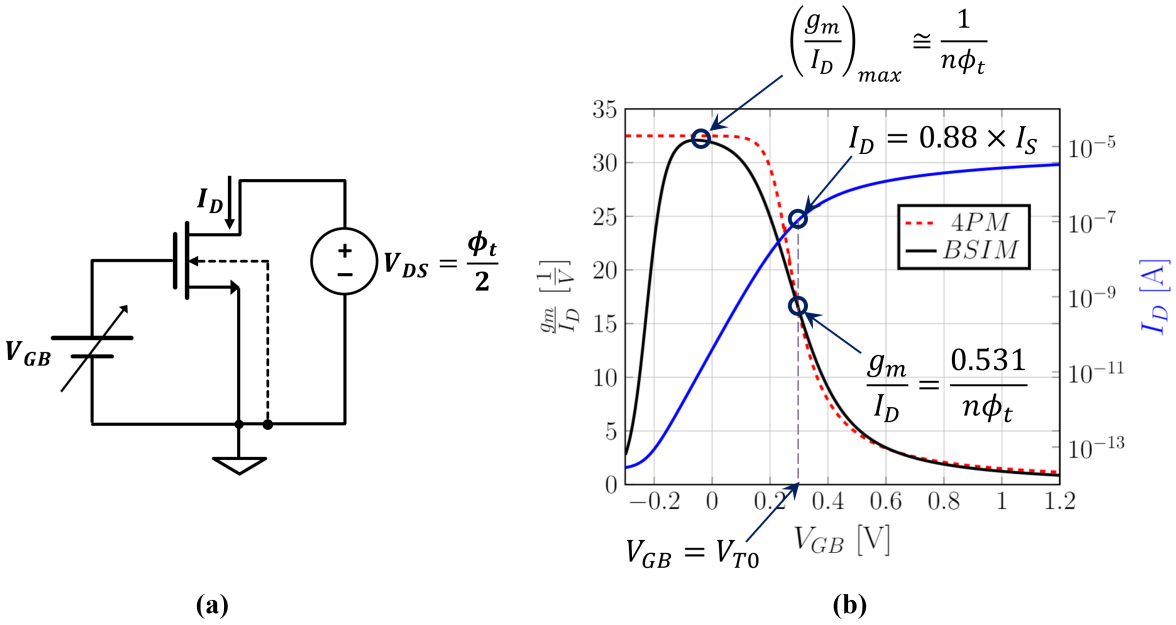
$$V_{DS} = \phi_t\left[\left(\sqrt{1+i_f}-\sqrt{1+i_r}\right)+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)\right] \tag{35}$$

The slope factor (n) can be extracted from (36), which is the asymptotic value of the g_m/I_D curve in a weak inversion.

$$\left(\frac{g_m}{I_D}\right)_{max} \approx \frac{1}{n\phi_t} \tag{36}$$

Figure 42(a) presents the circuit configuration to obtain the g_m/I_D characteristic and Figure 42(b) presents the values used to determine the parameters.

Figure 42 – (a) Circuit to measure the g_m/I_D characteristic in the linear region; (b) measurements of g_m/I_D and I_D as a function of V_{GB}; the annotated points are used to determine V_{T0} and I_S [57].



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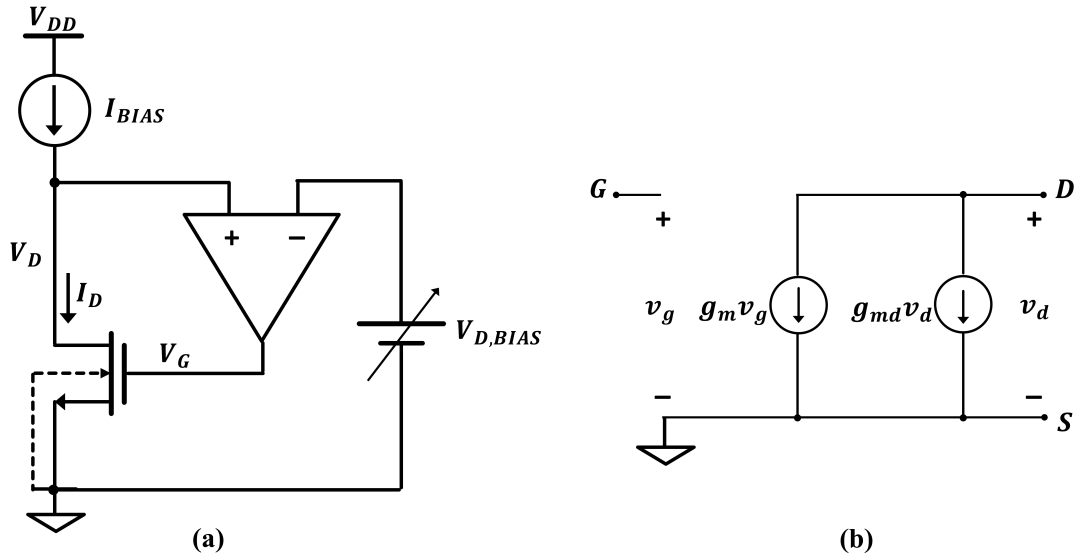
A.2 EXTRACTION OF DRAIN-INDUCED BARRIER LOWERING FACTOR (σ)

The DIBL factor (σ) is a small-signal parameter that affects the intrinsic voltage gain of the common source amplifier. Figure 43 presents a schematic to determine the common-source intrinsic gain (CSIG) and the equivalent small-signal model of the amplifier. An ideal operational amplifier was included in determining the common source intrinsic gain through simulation, as shown in Figure 43(a), to set the DC operating point required for the small-signal measurement.

In saturation, the use of the ratio of the gate to the drain transconductance characteristics yields the CSIG in (37).

$$A_{V,CS} = -\frac{g_m}{g_{md}} = -\frac{1}{\sigma} \tag{37}$$

Figure 43 – (a) Circuit to determine the CSIG and (b) its equivalent small-signal model.



Source – Reference [29].