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Analysis of Radiation Effects in Full Adder Circuits at 7nm FinFET Technology

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Analysis of Radiation Effects in Full Adder Circuits at 7nm FinFET Technology

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Ciência da Computação.

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ABSTRACT

The development of new technologies and new manufacturing processes in the semiconductor industry lead to the integration of billions of transistors into a single chip. This massive integration contributes to the reduction in operating voltage, power consumption, area, and costs of integrated circuits. However, the lower voltage operation and the low capacitance of the nanometer devices contributes to make them more susceptible to be affected by environment noises. This issue renders robustness a relevant aspect to be considered on the design of integrated circuits on advanced technologies nodes. Single Event Transient (SET) are non-destructive errors due to the interaction of environment energetic particles with silicon. A SET can temporarily change the correct value on combinational cells, compromising the expected behavior of the output values and, consequently, the proper functioning of the entire system. Because Full Adder (FA) is one of the primary cells of the Arithmetic and Logic Unit (ALU), and one of the most crucial component on computer systems, mitigating SET effects on them can improve more complex systems robustness. SET mitigation techniques can be adopted in different stages during the integrated circuit design flow. At the circuit level, the most explored techniques found in the literature are the use of Schmitt Triggers (ST), Decoupling Cells (DCELL), Transistor Sizing (TS), and Transistor Reordering. The goal of this work is to evaluate the radiation sensitivity in internal nodes of four full adder topologies. Additionally, the study aims to investigate the impact of using DCELL, TS, and combining these two techniques on SET effects for nominal (NV) and near-threshold voltage operation (NTV). The results show that the critical nodes and critical vectors can vary depending on the voltage operation and mitigation technique applied, mainly because they can influence the sensitivity of the circuit. However, TS can decrease the sensitivity of the output nodes, especially at nominal operation, for all topologies evaluated, while DCELL presented better improvements at NTV operation. Furthermore, at NTV operation, the mitigation techniques have side effects increasing the sensitivity of the internal critical nodes, despite the decrease in the total error occurrence. The adoption of mitigation techniques can reduce up to 60% the total error occurrence at nominal voltage, depending on the topology, and more than 35% at NTV in the circuits investigated. Moreover, the Hybrid topology presented, on average, 2% fewer errors than the Mirror at nominal voltage and 5% more errors than the Mirror for NTV. Among the PTL topologies at nominal voltage TFA presented 12% less errors than the TGA and up to 11% at NTV. Due to the relevance of FAs to digital designs, this set of information about the chosen FA topologies can assist designers to decide which circuit and mitigation technique are the most suitable for different requirements. Moreover, this work also maps all the internal nodes showing the critical parts for the circuits.

Keywords: Microelectronics. Circuit-level Design. Reliability. Single Event Transient. Mitigation. FinFET.

RESUMO

O desenvolvimento de novas tecnologias e processos de fabricação na indústria de semicondutores levou à integração de bilhões de transistores em um único chip. Essa integração maciça contribui para a redução da tensão de operação, consumo de energia, área e custos dos circuitos integrados. No entanto, a operação em baixa tensão e a baixa capacitância dos dispositivos nanométricos contribuem para serem mais suscetíveis e afetados por ruídos externos. Esse problema torna a robustez um aspecto relevante a ser considerado no projeto de circuitos integrados em nós de tecnologia avançada. Single Event Transient (SET) são erros não destrutivos devido à interação de partículas energéticas do ambiente com o silício. Um SET pode temporariamente alterar o valor correto em células combinacionais, comprometendo o comportamento esperado dos valores de saída e, consequentemente, o funcionamento adequado de todo o sistema. Como o Somador Completo (FA) é uma das células principais da Unidade Aritmética e Lógica (ULA) e um dos componentes mais cruciais em sistemas de computadores, a mitigação dos efeitos do SET neles pode aprimorar a robustez de sistemas mais complexos. Técnicas de mitigação do SET podem ser adotadas em diferentes estágios durante o fluxo de design de circuitos integrados. No nível do circuito, as técnicas mais exploradas encontradas na literatura são o uso de Schmitt Triggers (ST), Decoupling Cells (DCELL), Transistor Sizing (TS) e Transistor Reordering. O objetivo deste trabalho é avaliar a sensibilidade à radiação em nós internos de quatro topologias de somadores completos. Além disso, o estudo visa investigar o impacto do uso de DCELL, TS e a combinação dessas duas técnicas nos efeitos do SET para operação de tensão nominal (NV) e operação de tensão próxima ao limiar (NTV). Os resultados mostram que os nós e vetores críticos podem variar dependendo da operação de tensão e da técnica de mitigação aplicada, principalmente porque elas podem influenciar a sensibilidade do circuito. No entanto, TS pode diminuir a sensibilidade dos nós de saída, especialmente na operação nominal, para todas as topologias avaliadas, enquanto DCELL apresentou melhorias mais significativas na operação NTV. Além disso, na operação NTV, as técnicas de mitigação têm efeitos colaterais aumentando a sensibilidade dos nós críticos internos, apesar da diminuição na ocorrência total de erros. A adoção de técnicas de mitigação pode reduzir até 60% a ocorrência total de erros na tensão nominal, dependendo da topologia, e mais de 35% em NTV nos circuitos investigados. Além disso, a topologia Híbrida apresentou, em média, 2% menos erros do que a Mirror na tensão nominal e 5% mais erros do que a Mirror em NTV. Entre as topologias PTL na tensão nominal, a TFA apresentou 12% menos erros do que a TGA e até 11% menos em NTV. Devido à relevância dos FAs para designs digitais, esse conjunto de informações sobre as topologias de FA escolhidas pode auxiliar os projetistas a decidir qual circuito FA e técnica de mitigação são mais adequados para diferentes requisitos. Além disso, este trabalho também mapeia todos os nós internos, mostrando as partes críticas dos circuitos.

Palavras-chave: Microeletrônica. Design de Circuitos Integrados. Confiabilidade. Single Event Transient. Mitigação. FinFET.

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LIST OF ABBREVIATIONS AND ACRONYMS

ALU	Arithmetic and Logic Unit
ASAP7	7 nm Predictive Process Design Kit
CMOS	Complementary Metal-Oxide-Semiconductor
DCELL	Decoupling Cell
FA	Full Adder
FinFET	Fin Field-Effect Transistor
IC	Integrated Circuit
LET	Linear Energy Transfer
LETth	Linear Energy Transfer Threshold
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
NTV	Near-threshold Voltage
NV	Nominal Voltage
PTM	Predictive Technology Model
RHBD	Radiation-Hardening by Design
RVT	Regular Voltage Technology
SBU	Single Bit Upset
SE	Soft Error
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SET	Single Event Transient
SEU	Single Event Upset
SOI	Silicon-On-Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
TFA	Transmission Function Full Adder
TGA	Transmission-Gate Adder
TS	Transistor Sizing
VLSI	Very Large Scale Integration

CONTENTS

1 INTRODUCTION

The advancement of technology scaling has made possible the development of more efficient and sophisticated electronic devices (JANSSON et al., 2017). This progression in technology has enabled the integration of a larger number of transistors into a single die. As a result, it has led to an increase in computational capability while reducing the overall area, consequently driving down the costs associated with integrated circuits.

The Fin Field-Effect Transistor (FinFET) structure is a 3D device with a vertical fin-like structure that allows better control of electrical current flow. FinFETs have replaced traditional planar transistors in modern integrated circuits, as they offer improved performance, lower power consumption, and reduced leakage current. This technology is a key enabler for the development of smaller, faster, and more energy-efficient electronic devices, making it widely used for advanced nodes process in the semiconductor industry.

In conjunction with these technological developments, voltage operation conditions have also played a pivotal role. By reducing the operating voltage, electronic devices have achieved remarkable gains in power efficiency. Lower voltage operation has not only reduced power consumption but has also significantly contributed to enhancing the cost-effectiveness of integrated circuits with penalties on overall performance (DE; VANGAL; KRISHNAMURTHY, 2017).

However, as voltage operation and devices size are scaled down, electronic components become increasingly vulnerable to radiation-induced interference, a phenomenon that significantly impacts their reliability and performance in electronic systems (DODD et al., 2010). This susceptibility to radiation is particularly relevant when considering Single Event Effects (SEE), which is caused by the interaction of energetic particles coming from space or terrestrial noise with silicon. With the advent of nanometer technologies, the minimum charge required to induce a Soft Error (SE) decreases. This reduction can be attributed to factors such as decreased nodal capacitances, lower supply voltages, and higher-frequency operations. Consequently, these technological advancements elevate the probability of a memory element latching onto a SE pulse generated within the combinational logic (DODD et al., 2010).

The Full Adder (FA) is one of the primary combinational cells of the Arithmetic and Logic Unit (ALU) and one of the most crucial component on computer systems (NAVI et al., 2009). Moreover, FA is generally part of the critical path in most systems making this digital component strongly affects the overall performance of the whole system.

While FinFET devices offer attractive attributes for mitigating radiation-induced soft errors, it is essential to recognize that Single Events Effects, still have the potential

to deposit sufficient amount of energy, quantified by the Linear Energy Transfer (LET) required to induce a SE. This underscores the importance of examining Single Event Transient (SET) effects on FA circuits for radiation-sensitive applications.

1.1 MOTIVATION

In the contemporary landscape of integrated circuits, the miniaturization and increasing complexity of electronic systems have led to a growing concern regarding the susceptibility of circuits to SETs, particularly in the context of FA circuits. As these circuits play a fundamental role in arithmetic and logic operations, any vulnerability to soft errors can have cascading effects on the reliability of larger systems.

The motivation for this research is rooted in the critical need to address the impact of SETs on the robustness and reliability of FinFET combinational cells, which are prevalent in modern integrated circuits. The reduction in supply voltages, coupled with the escalating usage of microelectronics in diverse applications, has amplified the importance of understanding and mitigating the effects of SETs, even in scenarios not traditionally associated with radiation-induced errors.

The proposed solution aims to fill a crucial gap in current knowledge by systematically analyzing various circuit-level methods to mitigate the effects of SETs in a specific group of FA circuits. The chosen focus on FinFET logic cells is particularly relevant given their widespread use in advanced integrated circuits.

1.2 OBJECTIVE

The main goal of this work is analyze two circuit-level methods in three approaches aimed at mitigating the effects of SET for a group of four FA circuits. Additionally, this work will provide information about the robustness to radiation and the susceptibility of SET for the selected circuit topologies. It will consider how input vectors and different current pulse types influence these aspects across different voltage operations.

In this way, the objective of this work is devised in:

- To explore radiation sensitivity across two voltage operation scenarios.
- To assess the efficacy of two circuit-level techniques in three distinct scenarios for mitigating the effects of SETs.
- To demonstrate the mitigation tendency when different radiation particle characteristics are integrated into circuit-level design.
- To present a comprehensive trade-off analysis, weighing the advantages and drawbacks of each mitigation approach concerning area, performance, and power consumption.

- To provide an overall comparison between all techniques employed in the study.

In this study, we delve into two circuit-level techniques in three approaches designed to enhance the robustness of FinFET logic cells to soft errors. The first approach is the integration of decoupling cells, which act as reservoirs of charge to stabilize voltage levels, mitigate noise, and reduce power supply voltage fluctuations. Decoupling cells serve to enhance the overall performance and reliability of the circuit by minimizing electrical interference, providing a stable voltage supply, and ultimately, improving the circuit's resilience to soft errors (ZIMPECK et al., 2021).

The approach explored is Transistor sizing, a process that involves determining the physical dimensions of transistors within an integrated circuit. This includes selecting the appropriate width and length of transistors to optimize their functionality in terms of speed, power consumption, and area usage. For FinFETs, this sizing is primarily achieved by increasing the number of fins. By carefully adjusting transistor sizes, designers can fine-tune the performance of the circuit to meet specific requirements, thus contributing to the circuit's ability to withstand soft errors.

The final approach involves using both DCELL and Transistor Sizing to investigate the impact of combining these techniques. This method examines how the dual application affects overall performance and error resilience, despite the potential penalties in area and power consumption.

To evaluate the impact of the mitigation strategies, we compare the performance of FinFET logic cells with and without the application of these techniques. This comparison is based on a set of predefined metrics that serve as quantifiable indicators of the improvements achieved by incorporating Decoupling cells, Transistor sizing and combining both of them. These metrics help us evaluate the effectiveness of each technique in making FinFET logic cells more robust to soft errors, providing insights into the potential advantages and trade-offs associated with these circuit-level methods.

1.3 WORK ORGANIZATION

The organization of this work is structured as follows. It is divided into seven chapters, each with its own distinct focus. The Chapter 2 delves into the theoretical foundation of multigate devices, with a specific emphasis on FinFET transistors. This chapter provides a comprehensive exploration of FinFET operations, the evolution of manufacturing technology, layout design, predictive models, voltage operation, including both nominal and near-threshold operation modes, and an in-depth analysis of combinational cells, with a special emphasis on Full-Adder Circuits. It also explores (SEE), particularly SET, and concludes with a detailed definition of Radiation-Hardening by Design RHBD Schematic techniques.

Chapter 3, undertake a comprehensive review of relevant prior research within

the field. This examination of related literature establish a contextual foundation for the current research, offering insights and perspectives that contribute to a deeper understanding of the subject matter at hand. Within Chapter 4, it is provide a detailed account of the methodology used for modeling SET in the selected FA topologies, as well as the application of RHBD techniques. Additionally, we will discuss the tools and model devices utilized in our research.

Chapters 5 and 6 presents the results of the experiments, showcasing the potential of each circuit-level mitigation technique applied in the selected FA topologies and discussing the technical drawbacks of each approach. Furthermore, this chapter facilitates a comprehensive comparison of the proposed techniques, both internally and with related works.

The final chapter, Chapter 7, offers the research preliminary findings, reinforcing the initial contributions made throughout this work and outlining potential avenues for the conclusion of this research.

2 THEORETICAL FOUNDATION

This research addresses a set of different subjects, encompassing the emerging device technologies and radiation effects. Within this chapter, we initiate a preliminary exploration of fundamental concepts crucial to our investigation. These include the landscape of multigate devices, the nuanced of different voltage operation, the role of full adder circuits in digital computation, and the strategic application of RHBD techniques. Each of these concepts lays the groundwork for a comprehensive understanding of the challenges at the intersection of radiation resilience and cutting-edge electronic systems.

2.1 FINFET DEVICES

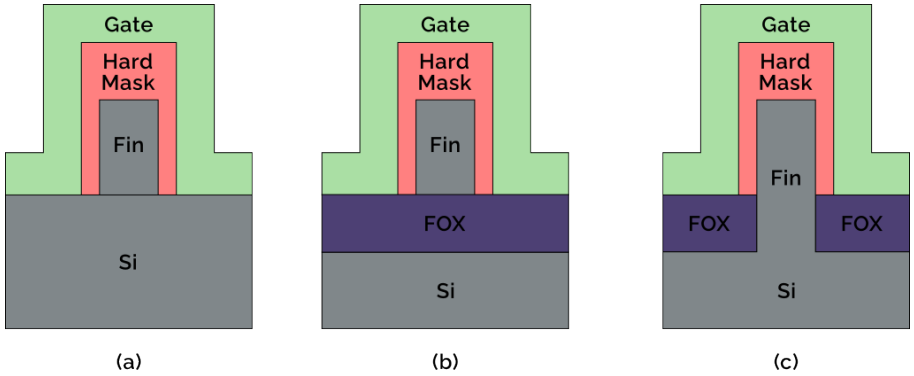
Due to the ongoing efforts to enhance current drive and improve control over short-channel effects, MOS transistors have progressed from classical, planar, single-gate devices into three-dimensional structures with a multi-gate design. A FinFET is a type of transistor architecture used in the design and manufacturing of integrated circuits. It is a three-dimensional structure that improves upon the traditional planar Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) design.

In a FinFET, the channel is raised above the substrate, allowing better control over the flow of current. This vertical fin structure helps mitigate issues associated with traditional planar transistors, such as leakage current and power consumption. The increased control over the channel also enables more efficient use of space, allowing for the integration of a larger number of transistors on a chip. The adoption of FinFETs has contributed to improved performance, energy efficiency, and overall transistor density in integrated circuits (COLINGE, 2007). FinFET technology has become a standard in modern semiconductor manufacturing processes, especially as chip features have shrunk to smaller nanometer scales.

Various manufacturing methods exist for FinFET devices, including Silicon-On-Insulator SOI FinFET and bulk FinFET. Figure 1 illustrates the comparison between FinFETs implemented on conventional wafers, SOI and bulk with insulator.

Bulk FinFET, introduced and adopted by Intel starting at the 22 nm node in 2012, utilizes the triple gate model (AUTH, 2012). In this design, the fin share the same silicon substrate, as illustrated in Figure 1 (a). The decision to employ bulk FinFETs was motivated by lower manufacturing costs and the application of the planar CMOS fabrication model, despite having slightly lower electrical characteristics compared to SOI FinFETs. In contrast, SOI FinFETs feature physically isolated fins achieved by an oxide layer, as seen in Figure 1 (b). Additionally, bulk FinFETs can be constructed with a dense insulator to prevent inversion between the fins, as shown in Figure 1 (c).

Figure 1 – Types of FinFET Technology.



Source: Adapted from (COLINGE, 2007).

2.2 VOLTAGE OPERATION

Nominal voltage operation and near-threshold voltage operation in Very Large Scale Integration (VLSI) circuits represent distinct approaches to designing circuits with different considerations for power consumption, performance, and energy efficiency.

Nominal voltage operation is the conventional and standard approach in VLSI circuit design. In this mode, circuits are designed to operate at a standard voltage level that ensures reliable and high-performance functioning. The emphasis is on achieving a balanced performance with considerations for speed, power consumption, and overall efficiency. Circuits designed for nominal voltage provide a reference point for achieving optimal processing speeds and are suitable for applications where performance is a primary concern.

On the other hand, near-threshold voltage operation involves running circuits at voltage levels close to the threshold voltage of the transistors. This approach is chosen to minimize power consumption, making it particularly suitable for applications with stringent power constraints. Operating at lower voltage levels offers the potential for improve energy efficiency by an order of magnitude (KAUL et al., 2012). However, this comes with challenges related to maintaining reliability, avoiding errors, and ensuring the circuit meets performance requirements under lower voltage conditions.

The key usage difference lies in the trade-off between power consumption and performance. Nominal voltage operation prioritizes speed and overall performance, making it more appropriate for applications where high processing speeds are crucial, even at the cost of increased power consumption. Near-threshold voltage operation, on the other hand, prioritize energy efficiency with some degradation on delay, making it suitable for applications where minimizing power consumption is a critical requirement.

2.3 FULL ADDER CIRCUIT

The addition operation holds significant importance in computational systems, serving as the foundation not only for ALU operations but also for tasks like multiplication, address generation, and various filtering purposes (WESTE; HARRIS, 2010). Given the critical role of this circuit, numerous FA architectures have been proposed in the literature, aiming to meet diverse constraints related to speed, power, and area (WESTE; HARRIS, 2010; ZHUANG; WU, 1992; CHANG; GU; ZHANG, 2005).

The FA circuit consists of two outputs and three inputs: Sum, which propagates the addition result after computation; Cout, which carries the most significant bit of the addition result to the next stage of the sum; and inputs A and B, which receive the operands for the addition operation. Cin is responsible for receiving the Most Significant Bit (MSB) value propagated from the Cout. Table 1 presents the truth table for the Full Adder circuit.

Table 1 – Truth table for Full Adder.

Inputs			**Outputs**	
A	**B**	**Cin**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

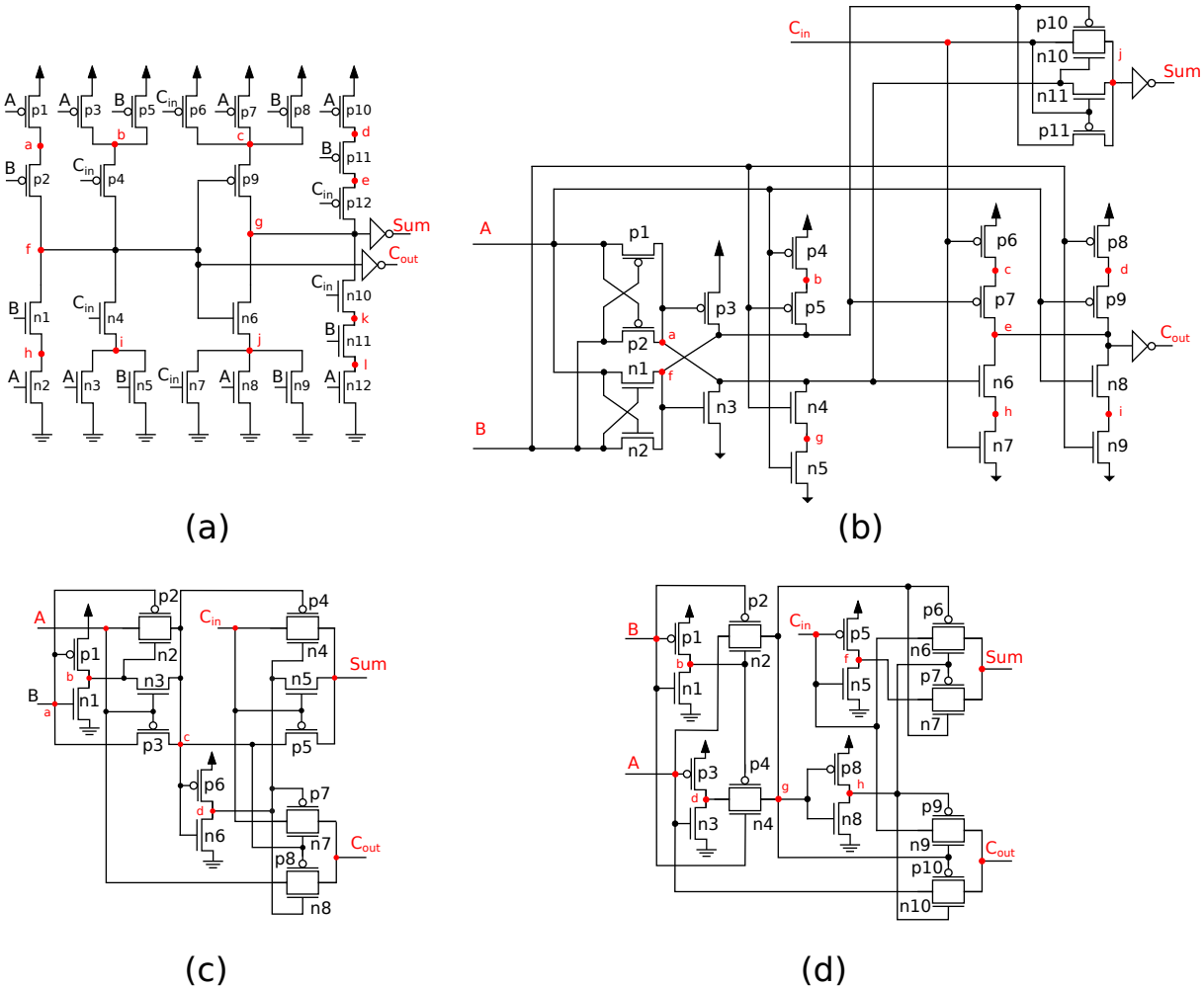
Source: The author.

This work adopts four FA topologies, highlighting all internal target nodes for SET insertion, as shown in Figure 2 (a)-(d). The complementary CMOS full adder, Figure 2 (a) known as Mirror FA, utilizes the conventional CMOS structure featuring pMOS pull-up and nMOS pull-down network of transistors (CHANG; GU; ZHANG, 2005). The output stage incorporates series transistors forming a weak driver, necessitating additional buffers at the final stage to ensure sufficient driving power for cascaded cells. The complementary CMOS style offers robustness against voltage scaling and transistor sizing, crucial for reliable operation at low voltage and various transistor sizes. Furthermore, the layout of the Mirror FA circuit is straightforward and area-efficient, attributed to complementary transistor pairs and a reduced number of interconnecting wires.

The topology in Figure 2 (b) is the Hybrid Full Adder. This FA encompass a XOR/XNOR, sum, and carry-out subcircuits, adopting a pass logic design style for simultaneous and efficient generation of XOR and XNOR functions used (CHANG;

GU; ZHANG, 2005). A well-driven carry-out is achieved through the complementary CMOS-style circuit. Additionally, the last-stage inverter decouples the output and input to enhance driving capability. Despite a higher transistor count compared to other designs, the Hybrid circuit demonstrates high energy efficiency across a broad supply voltage range.

Figure 2 – Full Adders topologies.



Source: Mirror (a) and Hybrid (b) from (CHANG; GU; ZHANG, 2005), TFA (c) from (ZHUANG; WU, 1992), and TGA (d) from (WESTE; HARRIS, 2010).

A transmission function full adder (TFA) is a CMOS full adder designed based on the transmission function theory (ZHUANG; WU, 1992). It has simpler circuit with less transistors being used in the design to perform the FA Boolean expression, the topology is shown in Figure 2 (c).

A transmission-gate adder (TGA), shown in Figure 2 (d), is a different full adder design that uses transmission gates to form multiplexers and XORs. This topology has the advantage of using fewer transistors and having equal Sum and Cout delay time (WESTE; HARRIS, 2010).

The four full adder topologies were chosen for this work because they are among the most commonly found in the literature, providing a comprehensive set for analyzing radiation robustness. Additionally, these topologies represent a diverse range of design approaches, including complementary logic, pass transistor logic, and a hybrid implementation that combines both methods. This multidisciplinary selection ensures a thorough evaluation of the different techniques and their effectiveness in enhancing the robustness of FinFET-based processors in radiation environments.

2.4 COSMIC RADIATION AND INTEGRATED CIRCUITS

Cosmic rays are high energy particles created in space by nuclear reactions in stars, in supernovas, and explosions in the galactic nucleus (ZIEGLER, 1996). There are different types of cosmic rays and they are categorized as follow:

- **Primary cosmic rays**: galactic particles that enter the solar system and can hit the Earth. Solar cosmic rays, the particles generated by the Sun and contained in the solar wind, are also considered as primary cosmic rays (AUTRAN; MUNTEANU, 2015).
- **Secondary cosmic rays**: particles in the Earth's upper atmosphere produced by the collision between primary cosmic rays and the atoms in the air. Those interactions create cascade reactions and generate more particles (e.g. neutrons, neutrinos, electrons) (AUTRAN; MUNTEANU, 2015).
- **Terrestrial cosmic rays**: Particles that finally hit the Earth. Less than 1% of the terrestrial particles are primary cosmic rays. The other 99% of particles is mostly composed of third to seventh generation particles (ZIEGLER, 1996).

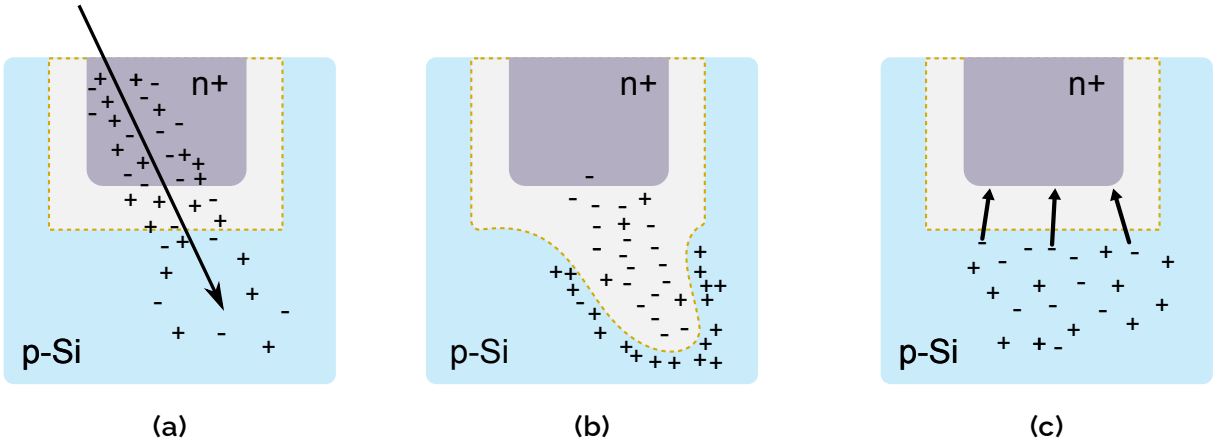
In the semiconductor industry, this energetic particles hitting integrated circuits circuit can lead to Single Event Effects, so they have to be cared about due the affect the reliability of the systems. In addition, with the transistor size reduction and increase integration, following Moore's law, circuit reliability to radiation is diminishing. Where only one transistor was affected by a radiation strike, now several transistors can suffer from one single strike.

2.4.1 Radiation effects on transistors

When an energetic particle hits a transistor junction, the impact triggers the charge collection mechanism of the device, collecting charge while the particle tracks into the depletion region (LEE et al., 2015). Figure 3 illustrates the three steps in the interaction between alpha particles and a PN junction. When an electrical charged particles penetrate silicon, they create an ionization track of electron-hole pairs, known as direct ionization Figure 3 (a). This process generates a parasitic current and causes

funneling in the space charge region Figure 3 (b). Finally, the remaining charges diffuse, producing a diffusion current Figure 3 (c). This current is the source of a soft error.

Figure 3 – Effects of radiation on a PN junction.



Source: Adapted from (LECAT-MATHIEU DE BOISSAC, 2021).

The energy transferred by ionization can be calculated using the Linear Energy Transfer. The LET represents an estimation of the energy collected by the material during the ionization process by an incident particle. It is defined as the energy loss per unit distance for a particle with a given density. The Q_{coll}, defined by the Eq. (2), is the amount of charge collected due to an ion strike in the junction. I_o is the minimum current to cause a fault, obtained by simulations. The term τ_α is the collection time constant of the junction, and τ_β is the time constant for the initially establishing the track. The term Q is the constant charge that the particle deposits along its track and L is the charge collection depth.

$$LET = \frac{Q_{coll}}{Q \times L} \tag{1}$$

$$Q_{coll} = I_o \times (\tau_\alpha - \tau_\beta) \tag{2}$$

The LET can also be expressed in terms of charged deposited by the particle to the material per unit path length, typically in MeV/cm (mega-electron volts per centimeter). It provides information about the density of ionization events along the path of a charged particle as it travels through a material. High-LET radiation tends to deposit more energy in a smaller volume, leading to a higher probability of causing ionization and potentially affecting the operation of electronic devices. For silicon the conversion factor is (GOMEZ TORO, 2014) :

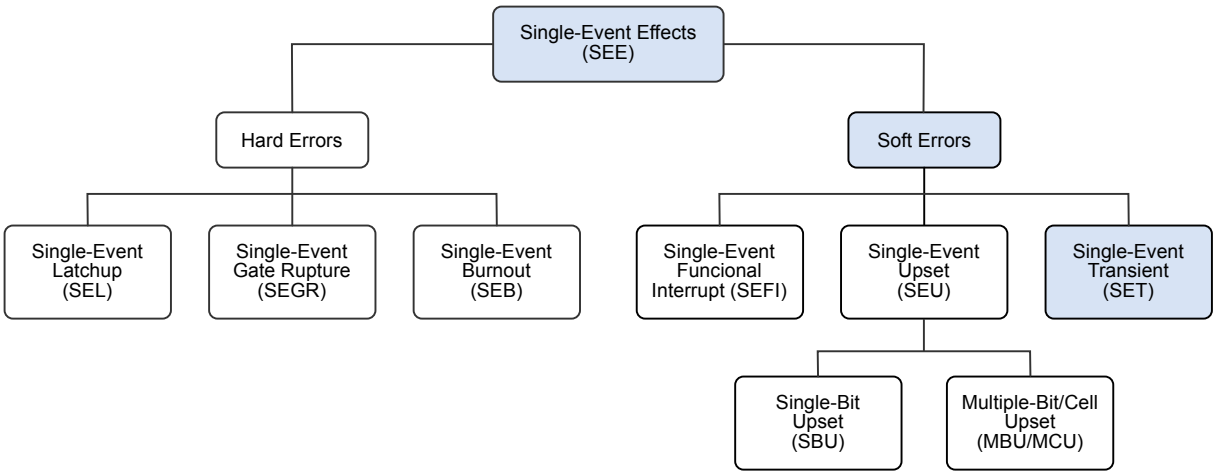
$$1 fC/\mu = 0.0969 MeV/(cm^2/mg) \tag{3}$$

Linear Energy Transfer is often used to characterize the impact of ionizing radiation, such as cosmic rays or particles from radioactive decay, on the performance and reliability of electronic components (SCHRIMPF et al., 2012).

2.4.2 Classification of radiation effects

The parasitic current caused by ionization is the main phenomenon affecting transistors. Transistors respond differently to this ionization, resulting in induced errors that can degrade their performance either permanently or temporarily. Single Event Effects is a broader term that classifying these errors and is crucial for focusing research efforts on finding effective solutions. As shown in Figure 4, SEEs can be categorized into two main types: soft errors and hard errors. Soft errors are nondestructive and reversible corruptions of a signal or data, whereas hard errors are permanent damages to the device or circuit. This work will focus on soft errors, as hard errors are beyond its scope.

Figure 4 – Classification of Single Event Effects.



Source: Adapted from (LECAT-MATHIEU DE BOISSAC, 2021).

Soft Errors is a broader term that encompasses various errors, including Single Event Upset (SEU), Single Event Functional Interrupt (SEFI), Single Bit Upset (SBU), and Single Event Transient.

A Single Event Upset is a type of error in a digital circuit caused by a single ionizing particle striking a sensitive node results in a transient voltage spike, which can flip a bit in memory or disrupt the operation of logic circuits. An SEU occurs in a memory element (such as a latch, flip-flop, RAM cell, or asynchronous memory logic) as a result of either latching an SET or a direct ionizing strike on the memory element. Single Event Upsets are the most common type of soft errors in memories and sequential logic. SEUs do not cause permanent damage to the device, but they can lead to temporary data corruption or malfunction until the system is reset or the error is corrected.

Since an SEU is stored in a memory element, the error is not transient. It can persist for several clock cycles in synchronous logic or until the next transition edge of an input signal in asynchronous logic. This prolonged presence of the error makes SEUs a significant concern in maintaining the reliability of electronic systems.

SEUs are primarily a concern in environments with high levels of radiation, such as space, where cosmic rays and other high-energy particles are prevalent. However, they can also occur at ground level due to particles from cosmic rays and radioactive decay in the materials used in the device. The increasing density and miniaturization of integrated circuits make them more susceptible to SEUs, necessitating robust error detection and correction mechanisms to ensure the reliability of electronic systems.

On the other hand, Single Event Transient is also a class of non-destructive errors caused due to a single ionizing particle strike in a device silicon however on combinational circuits. Because the non-sequential circuits outputs are based on the logical relationship to the input without retention capabilities any voltage glitch in the transistor may cause a temporary change in the output. When a charged particle interacts with a semiconductor device, it can deposit energy and generate electron-hole pairs. This can lead to a transient voltage glitch in the affected circuit, potentially causing incorrect operation.

The SET can affect the combinational cells resulting in wrong output values that, if held in the memory elements, can compromise the system's correctness (FERLET-CAVROIS; MASSENGILL; GOUKER, 2013). The SET effects on over 180 nm technologies are not noticed mainly due to electrical and logical masking (SHIVAKUMAR et al., 2002). However, with the advance to sub-90 nm nodes, the effects of charge collection has increased, show the need to understand and consider the SET effects during IC design steps in order to enhance reliability (REJIMON, 2006).

2.5 RADIATION-HARDENED-BY-DESIGN TECHNIQUES

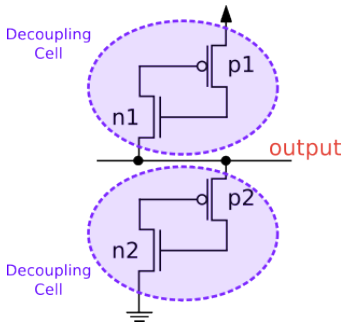
At advanced technology nodes, a significant reliability concern arises from the circuits vulnerability to environments noise. While radiation effects in electronic systems were initially predominantly associated with avionic or space applications, the electronic devices scaling and the use of low supply voltages have extended the relevance of these concerns to terrestrial applications (DODD et al., 2010).

Enhancing the reliability of integrated circuits involves radiation hardening strategies that can be explored from fabrication process modifications to different circuit design implementations. Because Radiation-Hardening-by-Process (RHBP) techniques has high costs and low-grade performances Radiation-Hardening-by-Design (RHBD) techniques are alternatives that have proven effective in ensuring resilience against radiation effects, particularly in highly-integrated technologies (LACOE et al., 2000).

Complete mitigation or some level of hardness against radiation effects can be achieved through circuit-based techniques. Circuit design modifications may lead to the incorporation of components or filtering elements, experimentation with different transistor arrangements, gate sizing, transistor folding, hardware redundancy, increase of the capacitance in vulnerable nodes, and other strategies (CHEN et al., 2017; LACOE et al., 2000; LILJA et al., 2013).

The circuit-level mitigation techniques of SET effects chosen for this work are the use of Decoupling Cell (DCELL) and exploring different transistor sizing (TS). DCELLs are composed of two transistors arranged in the cross-coupled mode, showed in Figure 5. Using two Decoupling Cells are recommended to achieve a more robust design for filtering positive and negative hit particles. DCELLs are responsible for increasing the total capacitance in the node applied, ensuring higher noise immunity in logic gates (REIS, R. et al., 2020). Generally, DCELLs are applied only to the output of the circuit to minimize noise interference. However, we opt to extend the traditional approach to observe the effects of the DCELL insertion on the internal node under evaluation, i.e, where the particle collision is happening.

Figure 5 – Decoupling Cell.

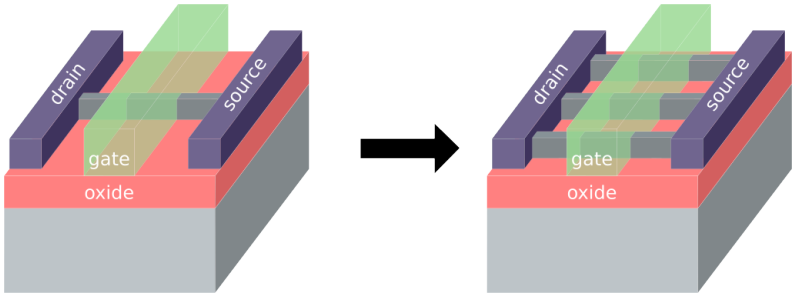


Source: Adapted from (ZIMPECK et al., 2021).

Sizing the transistors in FinFET technologies is related to the increase in the number of fins, as Figure 6 shows. When the number of fins is increased, the drive current of the transistor rises because the effective channel width is expanded. This improvement in drive current allows the transistor to switch faster, enhancing the overall performance and speed of the circuit (CLARK et al., 2016).

In the radiation scenario sizing the transistor leads to an increase in the amount of charge a particle must deposit in the depletion region to generate a SET. The TS was applied to all transistors of the FAs circuits, increasing the number of fins from one to three. Despite the area increase of TS, the design rules of the 7 nm ASAP7 technology recommends the adoption of the three fins to ensure the best routability of the circuits (CLARK et al., 2016). Thus, the area increase of TS strategy in the experiment is in an acceptable range for FinFET designs.

Figure 6 – Transitor Sizing.



Source: The author.

3 RELATED WORK

Some works have presented discussions about a variety of FAs using different logic styles (NAVI et al., 2009; DA SILVA; MEINHARDT; REIS, R., 2019). The key focus of these works is on reducing average power consumption and delay. The effects of nanometer variability is also a current research topic, mainly process variability on FAs (DOKANIA; IMRAN; ISLAM, 2013; AMES et al., 2016).

Other mitigation techniques are proposed to reduce the impact of process variability on these circuits (DOKANIA; ISLAM, 2015; MORAES et al., 2018; ZIMPECK et al., 2021). In (ZIMPECK et al., 2021), it is explored the influence of process variations and radiation-induced soft errors on FinFET logic cells, using the 7 nm technological node as a case study. The authors utilize the MUSCA SEP3 (HUBERT et al., 2009) radiation event generator for accurate soft error estimation and investigate four circuit-level mitigation techniques: transistor reordering (BUTZEN et al., 2010), decoupling cells (ANDJELKOVIC, M. et al., 2018), Schmitt Trigger (MORAES et al., 2018), and sleep transistors (RICARDO REIS YU CAO, 2014). The study evaluates the effectiveness of these techniques against various levels of process variation and radiation characteristics, offering a comprehensive trade-off analysis regarding reliability gains and design costs in terms of area, performance, power consumption, and SET resilience.

SET effects have been studied for different circuits, for example XOR (DE AGUIAR; MEINHARDT; REIS, R. A. L., 2017) and majority voters (OLIVEIRA, I. F. V. et al., 2022; AGUIAR, Y. de et al., 2017; BRENDLER et al., 2020). The authors at (OLIVEIRA, I. F. V. et al., 2022) evaluates various majority voter designs to determine their effectiveness in fault tolerance, particularly in radiation-prone environments. The study focuses on the resilience of these designs against SEUs and single-event SETs, which are critical for ensuring reliable operations in electronic circuits used in space and other high-radiation environments. The research compares the performance of different majority voter circuits, analyzing their ability to mitigate faults and maintain operational integrity. The evaluation is based on metrics such as error rate, power consumption, and area overhead. The results highlight the trade-offs between robustness and resource efficiency, providing valuable insights for designing more reliable digital systems. The findings underscore the importance of selecting appropriate majority voter designs to enhance fault tolerance in critical applications.

The authors of (AGUIAR, Y. Q. et al., 2020) presents transistor folding as layout technique for RHBD logic gates. This approach aims to mitigate the effects of SETs in integrated circuits, which are critical for ensuring the reliability of electronic devices in radiation-prone environments. The study emphasizes the effectiveness of transistor folding in enhancing circuit robustness without significantly impacting performance metrics like area, power, and speed. By employing Monte Carlo simulations,

the researchers demonstrate the improved resilience of circuits using this technique compared to conventional designs.

In (AZIMI; DE SIO; STERPONE, 2021), it is discussed a design for a radiation-hardened full-adder cell implemented in 45-nm technology. This design improves resilience against SETs through selective duplication of sensitive transistors based on radiation sensitivity analysis. Experimental results indicate a 62% reduction in SET sensitivity compared to the standard design, with improvements in performance and power overhead, and no increase in area overhead for the specific topology evaluated.

However, as far as we could investigate, there is a lack of more studies evaluating the radiation robustness FAs in multigate technologies considering different voltage scenarios and different full adder topologies.

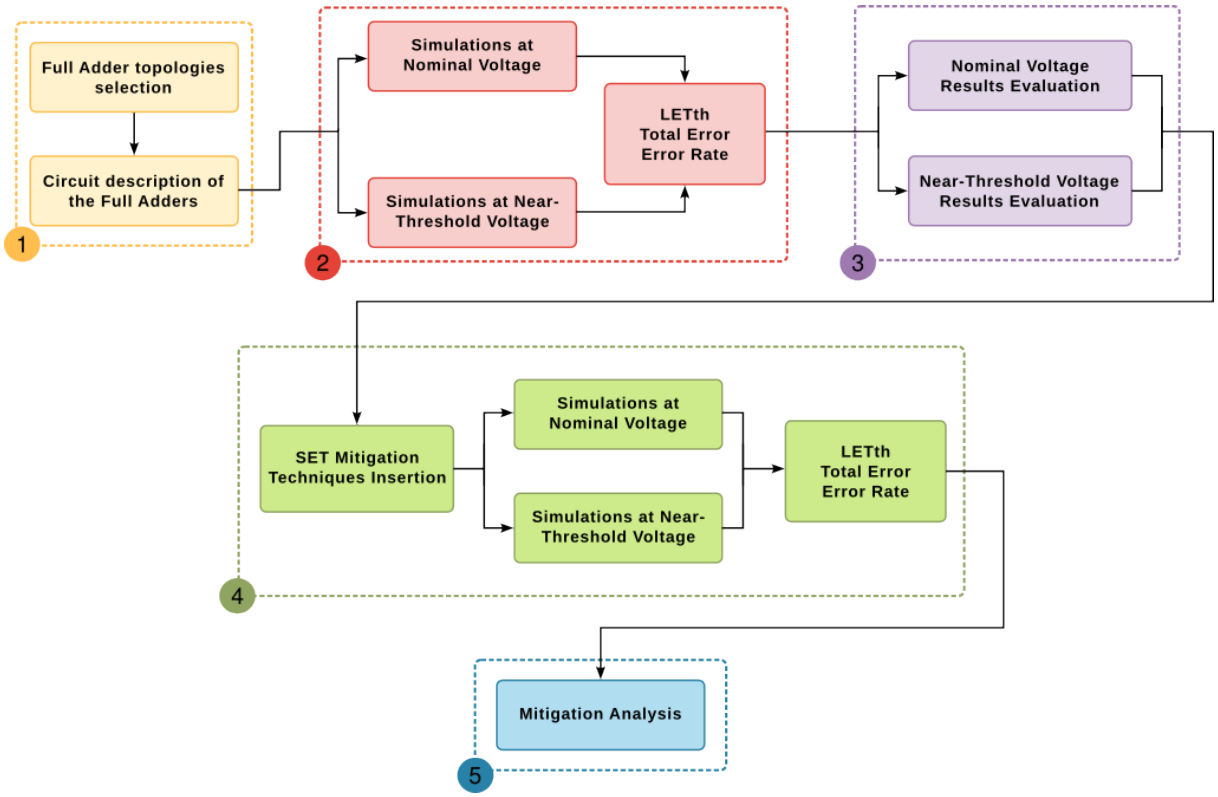
Table 2 – Related work summary.

Authors	**Focus**	**Key Findings**
Navi et al., 2009	Power consumption on FAs	Reduction on average power consumption and delay.
Da Silva et al., 2019	Variability on FAs	Reduction on average power consumption and delay.
Dokania et al., 2013	Variability on FAs	Comparative analysis for FAs designs offering minimum variabilities.
Ames et al., 2016	Variability on FAs	Process variability is the main responsible for the high delay and power.
Dokania et al., 2015;	Mitigation techniques for variability on FAs	Circuit-level technique to mitigate the adverse effects of PVT variations.
Moraes et al., 2018;	Mitigation techniques for variability	Improvement in average delay and power consumption.
Zimpeck et al., 2021	Mitigation techniques for process variability	Provides a trade-off analysis on reliability gains and design costs.
Oliveira et al., 2022;	SET effects on majority voters	Comparative analysis of radiation sensitivity.
Brendler et al., 2020	SET effects and variability on majority voters	Comparative analysis of radiation sensitivity.
Aguiar, Y. de et al., 2020	SET effects on majority voters	Comparative analysis of radiation sensitivity.
Azimi et al., 2021	Radiation-hardened FAs design	Reduction in the SET sensitivity.

4 METHODOLOGY

The goal of this work is to evaluate the sensitivity of full adder circuits, observing the impact of SET faults. For this purpose, this study presents comparison results for a subset of common full adder topologies found in the literature operating under nominal voltage (NV) conditions and near-threshold voltage (NTV). Subsequently, this work defines a comparative methodology based on electrical simulations in order to estimate the robustness of different topologies, identifying their critical points. Finally, fault mitigation techniques are inserted at the circuit level, and their effectiveness in enhancing radiation robustness is also evaluated using electrical simulations.

Figure 7 – Workflow.



Source: The author.

Currently, the workflow consists of five different steps, as shown in Figure 7: (1) a pre-study, (2) nominal and NTV simulation, (3) sensitivity results evaluation, (4) mitigation techniques insertion and lastly, (5) mitigation results analysis.

The first step involves selecting a subset of the most common full adder topologies. These topologies were described in Simulation Program with Integrated Circuit Emphasis (SPICE) to perform electrical simulations using the 7nm FinFET Predictive Technology Model (PTM) by (CLARK et al., 2016). All transistors on all circuits were set to the minimum size of 1-fin to represent a critical scenario for robustness tests. Two

inverters were inserted in the input signals to emulate a realistic input slope, and the load capacitance was adjusted to correspond to a fanout of 4.

The second step is the core of the proposed workflow. In this step, electrical simulations are conducted to obtain important metrics such as LET threshold (LETth), total error propagated, and error rate for each node. The nominal and near-threshold voltage for the devices was set to 0.7 V and 0.35 V, respectively. Fault simulation is conducted at the circuit level using HSPICE. Each internal node is tested individually to simulate the impact of a particle hit. In our work, we define the SET pulse as the voltage glitch occurring at the output of a logic gate, influenced by the deposited charge in any internal device. The radiation pulse is introduced as an independent current source at the target junction of the device, represented by the circuit node in the simulation and evaluation (SAYIL, 2016). Depending on the location of the ion impact, there are two types of single-event hits: n-hit and p-hit. An n-hit causes a high-to-low transition at the sensitive node, while a p-hit results in a low-to-high transition (DUAN; WANG, L.; LAI, 2011). The experiments involve determining the minimum current required to induce an output flip in the circuit, followed by calculating the minimum LETth based on the equation in (WANG, F.; AGRAWAL, 2008). The experiment concludes when the simulation requires a LETth value exceeding 100 $MeVcm^2/mg$. The current value is increased at 0.5 μA step to determine the minimum current to provoke the unexpected behavior on one of the FA outputs. The second step is essential for evaluating and identifying the critical parts of each circuit.

Step 3 comprises all the result evaluation that will guide the SET mitigation strategies. The focus is on evaluating and interpreting the results obtained from the default conditions simulations in stage (2) in order to find the critical internal nodes for each topology and also critical current to generate a SET.

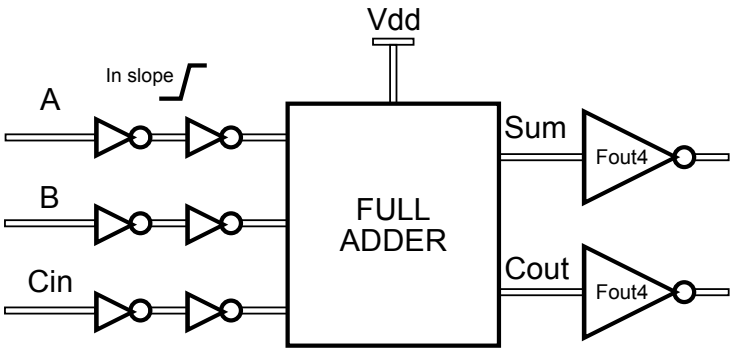
Mitigation techniques, specifically DCELL and Transistor sizing, are introduced to address Single Event Transient effects, in the fourth stage of the workflow. The DCELL is inserted only to the target node that will receive the pulse strike, and the transistor fins are sized according to the sizing strategy of the circuit being simulated. Subsequently, another round of SPICE simulation using the HSPICE tool is conducted for the modified circuits, operating at both nominal voltage and near-threshold voltage. The same metrics (LETth, Total error occurrence, and Error rate) are captured.

In step four, the mitigation techniques are applied to the same circuits and the results are collected. Finally, in the last step, the same metrics from step two are analyzed to understand the improvements in radiation robustness provided by each chosen technique.

4.1 ELECTRICAL SIMULATION

The circuits were simulated using the 7 nm ASAP7 Regular Voltage Technology (RVT) model (CLARK et al., 2016). The nominal operation adopts the nominal voltage for the RVT devices (0.7 V), and the near-threshold voltage is defined as half of the nominal voltage (0.35 V). Despite the recommendation of using 3-fin transistors (CLARK et al., 2016), in order to represent the critical scenario for robustness tests, all transistors on both circuits adopt the minimum size of 1-fin. Figure 8 illustrate the simulation environment used for the experiments in this work. To emulate a realistic input slope, we insert two inverters in the input signals. The load capacitance is set up to correspond to a fanout of 4.

Figure 8 – Test environment for simulations.



Source: The author.

4.2 RADIATION EFFECTS EVALUATION

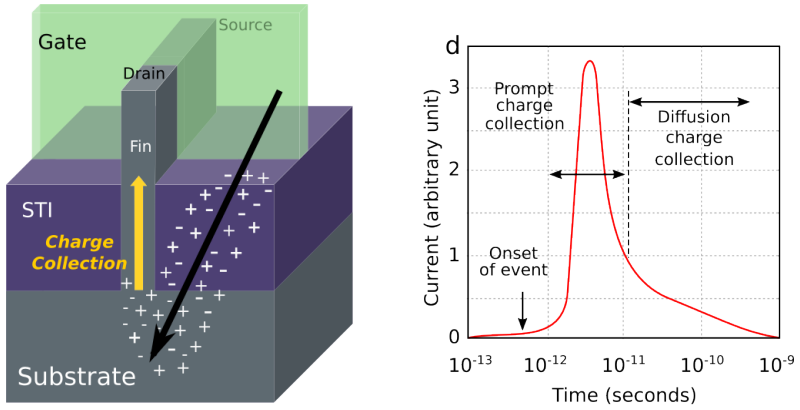
When an energetic particle hits a transistor junction, the impact triggers the charge collection mechanism of the device, collecting charge while the particle tracks into the depletion region (LEE et al., 2015), as illustrated in Figure 9 (a). The Linear Energy Transfer estimates this collected charge, thus, this metric is adopted to evaluate the robustness of an under-evaluation cell.

This work adopted the equation model defined in (SAYIL, 2016). The LETth is calculated for the FAs topologies using the Eq. (1).

In this work, the collection time constant is set to 200 ps, the initially constant time is set to 10 ps (SAYIL, 2016). The value of the Q and L constants on Eq. (1) for the FinFET devices used are 10.8 fC/μm and 21 nm (FANG; OATES, 2011), respectively.

In our work, we define the SET pulse as the voltage glitch occurring at the output of a logic gate, which is influenced by the quantity of deposited charge. Within our analyzed circuits, the transistor demonstrates sensitivity to charge collection when it is reverse biased and when there exists a low-resistance path between the affected node and the output. Depending on the location of impact from the incident ion, there are two

Figure 9 – Charge collection mechanism.



Source: Adapted from (LEE et al., 2015).

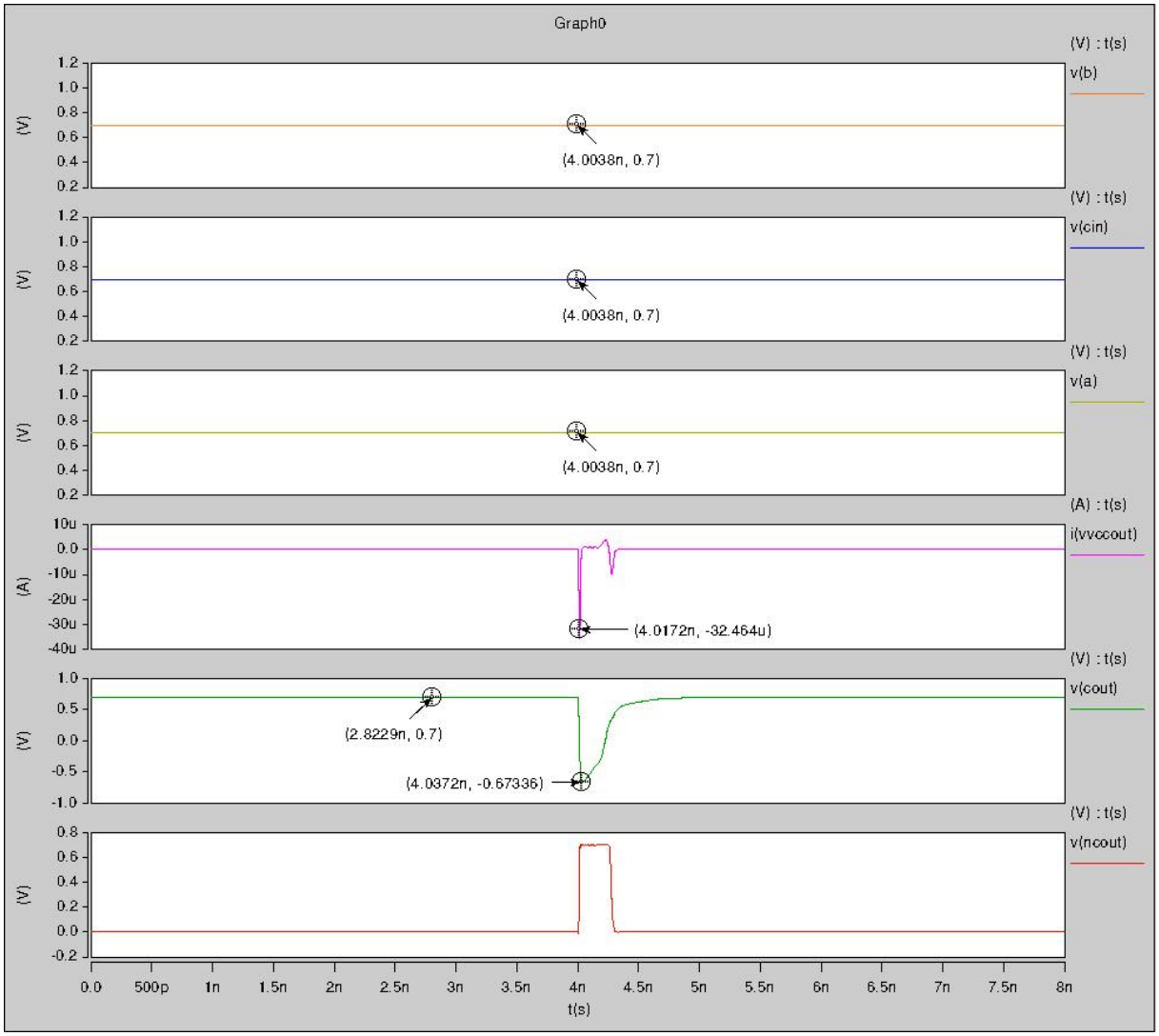
types of single-event hits: n-hit and p-hit. An n-hit results in a high-to-low transition at the sensitive node, whereas a p-hit causes a low-to-high transition (DUAN; WANG, L.; LAI, 2011). Thus, the radiation effect of a particle hitting at the junction of a device is described as a double exponential transient pulse shown in Figure 9 (b). The pulse can be modeled as a low-to-high (010) to reflect p-hits or a high-to-low (101) to n-hits. This work adopted the equation model defined in (SAYIL, 2016). The fault simulation is carried out at the circuit level using HSPICE and the radiation pulse is introduced as an independent current source at the target junction of the device, represented by the circuit node in the simulation and evaluation. The current value is increased at 0.5 μA step to determine the minimum current to provoke the unexpected behavior on one of the FA outputs. The simulations were performed in parallel using a Python script in order to automate and speed up the experiments results.

The experiments consist of finding the minimum current necessary to provoke an output flip of the circuit to them calculate the minimum LET, i.e., the LET threshold based on the equation in (WANG, F.; AGRAWAL, 2008). The experiment defines as a limit to be considered a robust a node (i.e. a robust junction) when the simulation requires a LETth value over 100 $MeVcm^2/mg$ since most particles encountered in space have lower LET (ANDJELKOVIC, Marko; KRSTIC, 2024). The circuit-level abstraction with electrical simulations allows us to evaluate all internal nodes, highlighted in red in Figure 2, and all input vectors, observing the fault propagation to each output function of the FA. This experiment was carried out for nominal voltage and NTV operation. The error susceptibility rate is the relation between the number of errors per node (or vector) and the total errors observed on the circuit.

Figure 10 illustrates the radiation glitch for a given pulse under the input combination 111 during a n-type hit. The current source i(vvccout), representing the charge collected of -32.454 μA, generates a voltage drop in V(cout) from 0.7 V to 0.67336 V.

This voltage drop is then propagated through V(ncout), demonstrating that a fault was captured by the charged circuit at the output.

Figure 10 – SET waveform example.



Source: The author.

4.3 RESULTS EVALUATION

In our investigation of SETs in FA circuits, understanding the distribution of errors across different nodes is vital for pinpointing vulnerable areas and devising effective mitigation strategies. The formula used to calculate the error rate is presented in (4). This expression involves two key variables: E_n, which represents the total errors found for a specific node, and E_{total}, which signifies the total errors observed in the entire topology. The formula calculates the ratio of errors at the specific node. This ratio is then multiplied by 100 to express the result as a percentage. The resulting E_r represents the

proportion of errors attributed to the specific node in relation to the total errors observed in the topology.

$$E_r = \frac{E_n}{E_{total}} \times 100 \tag{4}$$

Also, the influence of the input vector must be consider in the radiation evaluation. Different input vectors can lead to variations in the occurrence of errors within a circuit. By analyzing the impact of each input vector, it becomes possible to identify specific combinations that are more prone to propagating failures. This information is invaluable for localizing and understanding the sources of errors within the circuit.

Analyzing different radiation pulse types is crucial for understanding how specific environmental conditions, represented by distinct pulse patterns, impact the performance and reliability of integrated circuits. Each pulse type represents a unique set of challenges and stressors on the circuit components, influencing their response to radiation-induced effects.

4.4 SET MITIGATION TECHNIQUES INSERTION

To mitigate the impact of radiation, three distinct approaches are employed: DCELL, TS, and a combined strategy utilizing both DCELL and TS. The implementation of these techniques involves incorporating specific modifications into the SPICE descriptions of the transistor network constituting the evaluated FA circuit. In the DCELL technique, the extra cross-coupled circuit is inserted into each internal target node, ensuring that DCELL is applied to every node in the circuit under test. In the transistor sizing approach, all internal transistors of the topology under test are resized from 1-fin to 3-fin, including in the DCELL when combining both techniques. These tailored modifications precede the rerun of simulations to assess the effectiveness of each mitigation technique. Subsequently, the results derived from the application of these techniques are meticulously examined and discussed to evaluate their impact on enhancing the circuit's resilience against radiation-induced effects.

5 RESULTS ANALYSIS

The evaluation of the radiation sensitivity begins with testing the circuits while operating at their nominal voltage and then at NTV. This allows us to understand the impact of radiation in both typical and non-typical operating conditions. Throughout the evaluation process, reference values of absolute LETth are available for each result table. The complete result simulations can be checked in the Apendix A. LETth values greater than 100 MeVcm2/mg indicate nodes that are not sensitive to SET (ANDJELKOVIC, Marko; KRSTIC, 2024) and this condition where the circuit remains robust are denoted by a "-" in the results tables. To identify critical cases that are more susceptible to radiation-induced errors, we highlight them in red within the tables. By focusing attention on these critical cases, significant insights can help to highlight potential weaknesses within the circuit's radiation tolerance and develop targeted mitigation strategies to enhance overall reliability.

The presentation of results will follow a structured format. Initially, findings for the nominal voltage operation will be presented, covering the error rate, critical nodes, critical input vectors, and the critical hit type. Subsequently, a similar set of results will be provided for the NTV operation. Finally, an overall comparison between the two voltage operations will be outlined.

5.1 NOMINAL VOLTAGE

The nominal voltage denotes the predetermined standard operating voltage level at which a digital circuit is engineered to achieve optimal functionality. It represents the voltage necessary to uphold the performance of the circuit under typical operational circumstances. This particular voltage typically derives from the precise specifications of the process technology employed in the production of integrated circuits. The utilization of a circuit at its nominal voltage is fundamental in satisfying the stipulated requirements for performance, speed, and reliability, all while maintaining a reasonable power consumption. Within the context of the technology applied in this research, the nominal voltage is defined as 0.7 V.

5.1.1 Error Rate

Based on the total error analysis for each node we can identify the most and least sensitive nodes, highlighted in Figure 11, 12, 13, and 14. The total error is indicative of the robustness of each node in the face of faults, with lower values signifying less sensitivity. Also the finds in this sections is summarized in Table 7.

The analysis of LETth in Table 3 for the Mirror FA at nominal voltage sheds light on node *k*, which exhibit a higher probability to generate transient errors in this

topology. Node *k* collectively contribute to nearly 13% of all error occurrences observed in our experiments, emphasizing its significance in the error rate landscape. Nodes *e*, *f*, *g*, *l*, *Sum* and *Cout* also demonstrate notable error rates, although these values vary depending on the input pulses. These nodes can be considered moderately sensitive, as their error rates range from 9% to 10% of the total error occurrence. Nodes that are farther from the output in the Mirror FA topology exhibit greater resilience to noise interference. This increased resilience is attributed to the the capability of the transistor network to mask potential glitches in the signal. Specifically, nodes driven by more than one transistor, such as nodes *b*, *c*, *i*, and *j*, have shown a higher resistance to error propagation.

To summarize, node *k* emerges as the most sensitive components in the Mirror FA topology, while nodes *e*, *f*, *g*, *l*, *Sum* and *Cout* exhibit moderate sensitivity. Nodes *b*, *c*, *i*, and *j* demonstrate relatively lower sensitivity to faults, highlighting their robustness.

Table 3 – LETth for all nodes of Mirror FA at Nominal Voltage ($MeVcm^2/mg$).

Pulse	Input	Nominal													
		a	b	c	d	e	f	g	h	i	j	k	l	Sum	Cout
010	000	-	-	-	-	-	-	-	-	-	-	97	-	45	45
	001	-	-	-	-	-	-	-	96	-	-	67	97	-	45
	010	-	-	-	-	-	-	-	-	-	-	52	59	-	45
	011	-	-	-	-	-	27	-	-	47	-	-	-	45	-
	100	-	-	-	-	26	-	-	-	-	-	98	-	-	45
	101	27	-	-	-	-	27	-	-	48	-	-	-	45	-
	110	51	27	-	-	-	27	-	48	-	-	-	-	45	-
	111	-	-	-	-	-	60	-	-	-	-	-	-	-	-
101	000	-	-	-	42	21	46	**14**	89	-	**14**	20	40	-	-
	001	-	41	-	-	26	20	27	20	-	47	52	59	37	-
	010	-	41	-	26	26	20	27	97	-	47	97	-	37	-
	011	83	-	39	85	53	-	20	-	-	-	71	-	-	37
	100	41	-	-	-	78	21	27	96	20	47	66	97	37	-
	101	-	-	40	-	83	-	20	-	-	-	20	20	-	37
	110	-	-	39	55	43	-	20	-	-	-	20	-	-	37
	111	-	-	19	-	80	-	19	-	-	-	27	48	37	37

*Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100MeVcm^2/mg$.

Turning our attention to the Hybrid FA, Table 4 reveals that nodes *c* and *d* stand out with the highest error rates. This consistency suggests that these nodes emerge as the most susceptible to error generation, experiencing significant disruptions under fault conditions. Together they represent approximately 20% of the total error occurrences observed at nominal voltage. Nodes *a*, *e*, *f*, *h*, *i*, *j*, *Sum* and *Cout* display moderate levels of sensitivity very similar to the critical ones, as indicated by their error rate, which is close to 9% each. These nodes are moderately susceptible to faults, with their performance affected to a noticeable extent. Node *Cin* consistently exhibits a robust performance across diverse fault propagation scenarios, as indicated by the absence of errors in the simulations. The consistent stability of *Cin* emphasizes its robust behavior against faults, highlighting its capacity to maintain functionality without notable disruptions. This resilience can be attributed to the signal path of *Cin* being

associated with either a pass transistor logic or a complementary logic circuit subpart, which effectively filters out potential SET error glitches.

In summary, nodes *c* and *d* emerge as the most sensitive components in the Hybrid FA topology, while nodes *a*, *e*, *f*, *h*, *i*, *j*, *Sum* and *Cout* exhibit similar degrees of sensitivity. Node *Cin* exhibits a sensitivity that is not context-dependent, demonstrating an absence of errors even across different pulse scenarios. This analysis provides insights into the robustness of each node in the Hybrid FA topology under worst-case fault propagation conditions. This insight into the error rate distribution provides a foundation for exploring targeted mitigation techniques, aiming to fortify these vulnerable nodes and enhance the overall robustness for this topology.

Table 4 – LETth for all nodes of Hybrid FA considering worst fault propagation at Nominal Voltage($MeVcm^2/mg$).

Pulse	Input	Nominal												
		a	b	c	d	e	f	g	h	i	j	Cin	Sum	Cout
010	000	51	-	-	-	-	-	-	-	-	-	-	45	45
	001	78	-	-	-	-	-	-	-	-	26	-	-	45
	010	-	-	-	-	-	29	62	59	-	64	-	-	45
	011	-	96	26	26	27	25	66	47	-	-	-	45	-
	100	-	29	-	-	-	30	-	59	54	65	-	-	45
	101	-	25	26	-	27	25	-	47	69	-	-	45	-
	110	65	-	-	49	26	-	-	-	46	-	-	45	-
	111	73	-	49	49	49	-	-	-	46	31	-	-	-
101	000	-	-	-	39	20	59	-	38	38	24	-	-	-
	001	-	-	**8**	39	20	51	-	94	38	-	-	36	-
	010	20	-	40	59	20	-	19	20	96	-	-	36	-
	011	28	-	12	14	-	-	28	-	-	39	-	-	36
	100	19	12	40	-	20	-	91	20	20	-	-	36	-
	101	28	13	12	-	-	-	-	-	-	39	-	-	36
	110	-	19	-	21	-	85	-	-	-	20	-	-	36
	111	-	20	19	19	-	58	-	-	-	-	-	36	36

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100MeVcm^2/mg$.

The outcomes for the TGA topology at operating nominal voltage are detailed in Table 5. Notably, nodes *h* and *Sum* emerge as the most susceptible to error generation, constituting combined an average of 28% of the total error occurrences. This indicates their heightened vulnerability to errors, making them the most sensitive nodes in the TGA topology. The elevated total errors suggest that these nodes may experience substantial disruptions or malfunctions under fault conditions. An interesting observation is that, in contrast to other topologies, this configuration exhibits outputs that are less robust to SETs compared to its internal nodes. On the other hand, nodes *b*, *Cout* and *g* also demonstrate significant total errors, although these values vary depending on the input pulses. These nodes appear to be moderately sensitive, and their total errors suggest potential susceptibility to faults. Analyzing the LET values associated with these nodes errors could provide further insights into the nature and severity of potential sensitive parts for this topology.

Overall, nodes *h* and *Sum* emerge as the most sensitive components in the TGA topology, while nodes *b*, *Cout* and *g* demonstrate varying degrees of sensitiv-

ity. Node Sum, with its consistently lower total errors, appears to be among the less sensitive nodes in the topology. Further examination of LET values can improve the understanding of how radiation affects the performance of each node.

Table 5 – LETth for all nodes of TGA FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Nominal									
		B	b	A	d	Cin	f	g	h	Sum	Cout
010	000	45	-	48	-	47	-	28	-	28	27
	001	45	-	48	-	-	-	28	-	-	27
	010	-	47	46	-	47	-	-	46	100	28
	011	-	48	45	-	-	47	-	47	28	-
	100	46	-	-	-	47	-	-	45	100	28
	101	46	-	-	-	-	47	-	55	28	-
	110	-	54	-	46	47	-	27	-	28	-
	111	-	54	-	47	-	-	28	-	-	-
101	000	-	39	-	-	-	-	-	39	-	-
	001	-	39	-	-	38	95	-	40	**21**	-
	010	36	82	-	38	-	37	22	89	**21**	-
	011	36	80	-	37	37	-	22	89	90	**21**
	100	-	52	38	96	-	37	22	91	**21**	92
	101	-	56	42	-	37	-	24	90	90	**21**
	110	38	-	38	-	-	-	88	39	-	**21**
	111	38	-	38	-	38	95	88	52	**21**	**21**

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100MeVcm^2/mg$.

Additionally, similar to the TGA topology, we observe that an output node is among the most susceptible to propagate transient errors. This similar behavior between TGA and TFA could be linked to the absence of a buffer structure in the output, as evident in the designs illustrated in the previous Figure 2.

In the context of the TFA FA topology, as indicated in Table 6, nodes *e* and the output *Cout* demonstrate higher susceptibility to error generation, each contributing an average of 14% to the total error occurrences. Nodes closer to the output exhibit higher degrees of sensitivity, with some nodes demonstrating almost the same error rate of the two critical ones. Nodes B, A, and Cin, being closer to the output, present diverse error rates across different pulse scenarios. Node B shows a consistent error rate, while nodes A and Cin exhibit variability in their error rates. This sensitivity suggests that these nodes may be susceptible to disruptions, with potential impacts on system performance. Nodes b, e, and f display distinct behavior, with varying error rates in response to different pulse inputs. Nodes b and f, however, demonstrate sensitivity in certain cases, indicating their potential susceptibility to faults.

The cumulative error rate in node Sum is context-dependent, emphasizing the importance of a comprehensive analysis across different pulse scenarios. This variability underscores the need to consider specific conditions to accurately assess the behavior and sensitivity of node Sum in fault propagation scenarios.

To summarize, the analysis of error rates for each node in the TFA FA topology highlights varying sensitivities and robust behaviors. The context-dependent nature

of certain nodes emphasizes the need for a detailed examination of different pulse scenarios to fully understand their fault tolerance and overall performance.

Table 6 – LETth for all nodes of TFA FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Nominal							
		B	b	A	Cin	e	f	Sum	Cout
010	000	55	-	55	47	34	-	28	27
	001	51	-	47	-	29	-	-	27
	010	-	44	48	47	-	43	-	28
	011	-	43	45	-	83	47	27	100
	100	47	-	-	41	-	42	-	28
	101	46	-	-	-	84	47	27	-
	110	-	53	-	47	29	-	28	-
	111	-	48	-	-	27	-	-	-
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	37	-	46	21	-
	010	39	97	-	-	21	85	**14**	-
	011	37	92	-	38	19	-	-	21
	100	-	67	40	96	23	85	**14**	93
	101	-	65	40	38	23	-	-	21
	110	37	-	38	-	-	52	-	21
	111	37	-	38	37	-	67	21	21

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 7 – Error rate analysis for each FA topology

FA Topology	**Most Sensitive Nodes**	**Moderately Sensitive Nodes**	**Least Sensitive Nodes**	**Notes**
Mirror FA	Node k (13% of errors)	Nodes e, f, g, l, Sum, Cout (9% to 10% of errors)	Nodes b, c, i, j	Sum same error rate of Cout
Hybrid FA	Nodes c and d (20% of errors)	Nodes a, e, f, h, i, j, Sum, Cout (9% each)	Node Cin (no errors)	Cin node shows high robustness
TGA FA	Nodes h and Sum (28% of errors)	Nodes b, Cout, g	Node Sum	Outputs less robust compared to internal nodes
TFA FA	Nodes e and Cout (14% of errors)	Nodes B, A, Cin (varying error rates)	Node A	Sum output context-dependent

5.1.2 Input Vectors

In the context of a FA circuit, an input vector combination refers to a specific arrangement of input values applied to the circuit to perform a computation. A FA is a digital circuit designed to add binary numbers and account for values carried over from previous addition stages. The input vectors for a FA consist of three binary inputs: A, B, and Cin (carry-in). In the field of radiation hardness, the sensitivity of a circuit

to radiation events can vary depending on the specific combination of input vectors applied. Certain input vector combinations may lead to conditions where the circuit is more vulnerable to radiation-induced errors.

For the Mirror full adder at nominal voltage, a notable observation from Table 3 is that 16% of the total errors manifest in response to the input vector 011. However, vector 100 also contributes significantly to error propagation, albeit with a slightly lower rate of 12% compared to vector 011. The critical LETth are associated with the vector 000, establishing it as the pivotal input combination with the lowest LETth and, consequently, the most critical for the Mirror circuit at nominal voltage.

Shifting our focus to the Hybrid FA results presented in Table 4, a distinct pattern emerges in the error rates corresponding to different input vectors. The vector 000 stands out with the lowest error rate, constituting a mere 8% of the total error occurrences. In contrast, the vector 011 demonstrates the highest error rate at almost 15% of the total occurrences. Of particular significance is the vector 001, which exhibits the lowest LETth, designating it as the critical vector for the Hybrid FA.

Table 5 reveals that, for the TGA FA, vector 011 contributes close to 17% of the total error occurrences. Although this vector also exhibits the critical LETth value, except for vector 000, all other input combinations eventually reach the LETth of 21 $MeVcm^2/mg$. This emphasizes that, for this topology, the critical values are not dependent on input combinations.

Much like the preceding topologies, the TFA FA demonstrates that vector 011 is highly susceptible to generating transient errors, contributing an average of 18% to the total error occurrences. However, in this topology, the critical LETth values occur for the 010 and 100 input combinations. Additionally, vector 000 exhibits only 6% of errors, making it the most robust combination in this context.

This comprehensive analysis of input vectors sheds light on specific combinations that significantly influence error rates, aiding in the identification of critical scenarios and potential avenues for targeted mitigation strategies. The findings aid in identifying critical scenarios and offer potential avenues for targeted mitigation strategies, as summary for this section results is presented in Table 8.

5.1.3 Hit Type

In the context of radiation-induced effects on digital circuits, different electrical pulse types, specifically high-to-low and low-to-high transitions, result from the interaction of energetic particles with the circuit components.

The high-to-low pulse occurs when an energetic particle, such as a proton or heavy ion, interacts with the semiconductor material of a digital circuit. This interaction deposits charge along the path of the particle, creating an electrical potential that can lead to a transient voltage drop or a pulse from a high logic level to a low logic level,

Table 8 – Input vector sensitivity analysis for each FA topology

FA Topology	**Most Error-Prone Input Vectors**	**Critical Input Vectors (Lowest LETth)**	**Least Error-Prone Input Vectors**
Mirror	011 (16% of errors) 100 (12% of errors)	000	000
Hybrid	011 (15% of errors)	001	000 (8% of errors)
TGA	011 (17% of errors)	011	000
TFA	011 (18% of errors)	010 100	000 (6% of errors)

which can be called a n-hit.

Conversely, the low-to-high pulse, or p-hit, is characterized by an energetic particle causing a transient increase in voltage. Similar to the n-hit pulse, this occurs when charge is deposited along the path of the particle, creating a potential that leads to a temporary voltage rise or a pulse from a low logic level to a high logic level. The results for the pulse type across the evaluated topologies are summarized in Table 9.

Examining the impact of different radiation hit type on the Mirror FA presented in the first column of Table 3, the n-hit emerges as the critical one. This pulse generates the lowest LETth across all outputs, highlighting its significance in inducing transient errors. Moreover, the n-hit is responsible for nearly 57% of the total transient errors observed in the simulations, showcasing its dominant role in error propagation. Notably, this rate is up to 20% higher compared to the results associated with the p-hit, further emphasizing the critical nature of the high-to-low pulse in the Mirror Full Adder.

Shifting our focus to the Hybrid FA result on Table 4, the analysis reveals that the majority of errors, close to 58%, occur during the n-hit. This pulse stands out as the primary contributor to error generation in this topology, underscoring its significance in influencing the overall error characteristics of this particular FA circuit.

In the TGA FA, the n-hit was responsible for inducing errors in up to 57% of cases. Notably, 44% of these errors manifested in the Sum output. This observation underscores the significance of the n-hit as the critical pulse for this topology. This behavior can be attributed due to the paths that are more susceptible to charge deposition and subsequent transient errors when subjected to the high-to-low interaction.

In contrast to the other examined topologies, the TFA full adder exhibited a unique behavior in response to radiation, as evidenced by consistent results for both p-hit and n-hit pulses in the simulations. Unexpectedly, the error rates were approximately 50% for both hit types, showcasing a balanced susceptibility to transient errors. Upon closer examination of individual output nodes, it was observed that the Cout output exhibited a consistent error rate of around 17%, while the Sum output displayed a slightly

higher susceptibility, reaching approximately 34% for both hit type. This uniformity in error rates across different hit types suggests that the TFA topology might possess a symmetric vulnerability to radiation-induced effects, impacting both rising and falling transitions in a comparable manner.

Table 9 – Hit type percentage for each FA topology.

FA Topology	n-hit rate	p-hit rate	Additional Notes
Mirror	57%	43%	Lowest LETth across all outputs is due the n-hit.
Hybrid	58%	42%	The primary contributor to error generation is n-hit.
TGA	57%	43%	Sum output is most sensitive node due to n-hit.
TFA	50%	50%	Balanced susceptibility to both hit types.

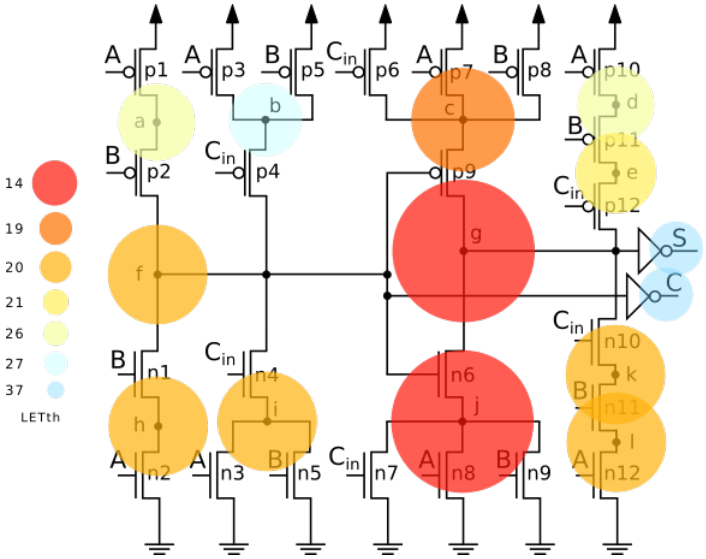
5.1.4 Critical Nodes

Understanding the behavior of internal nodes in FA circuits is crucial for assessing their vulnerability to Single Event Transients. In our investigation, we conducted a thorough analysis of critical nodes, focusing on their LETth values, which provide insights into their internal resilience to transient errors induced by radiation. This critical node analysis considers the worst LETth value among all input vector combinations and hit-types. The achievements in this section are summarized in Table 10.

In Figure 11, we present the LETth values for various nodes of the Mirror FA, emphasizing nodes *g* and *j* as the critical ones due to their remarkably low LETth values. This analysis lays the foundation for comprehending the potential impact of radiation on these specific nodes. Nodes *g* and *j* demonstrates the lowest LETth value of 14 $MeVcm^2/mg$, highlighting its higher sensitivity to radiation-induced effects. These internal nodes appears to be critical, as its lower LETth value suggests a greater vulnerability compared to other nodes, specially the output ones. Nodes *c*, *f*, *h*, *i*, *k* and *l*, exhibit relatively moderate sensitivities with lowest LETth values ranging from 19 to 20 $MeVcm^2/mg$. Despite their relatively higher sensitivity, these nodes can still impact the correctness of the topology. Nodes *Sum* and *Cout* demonstrate lowest LETth values of 37 $MeVcm^2/mg$. The outputs stands out as less critical, indicating a lower sensitivity to radiation-induced effects compared to the cumulative effects seen in internal nodes. This behavior may be attributed to the ability of the output load to mask SET errors glitch, preventing their propagation.

Ultimately, the critical nodes in the Mirror Full Adder, based on the lowest LETth values, are *g* and *j* . These internal nodes are more susceptible to radiation-induced effects, while other nodes exhibit varying degrees of resilience. The outputs appears to be less critical in the context of cumulative effects, emphasizing the need for careful consideration of individual internal node sensitivities for robust design and performance under radiation exposure.

Figure 11 – Mirror Full Adder critical nodes at nominal voltage.



Source: The author.

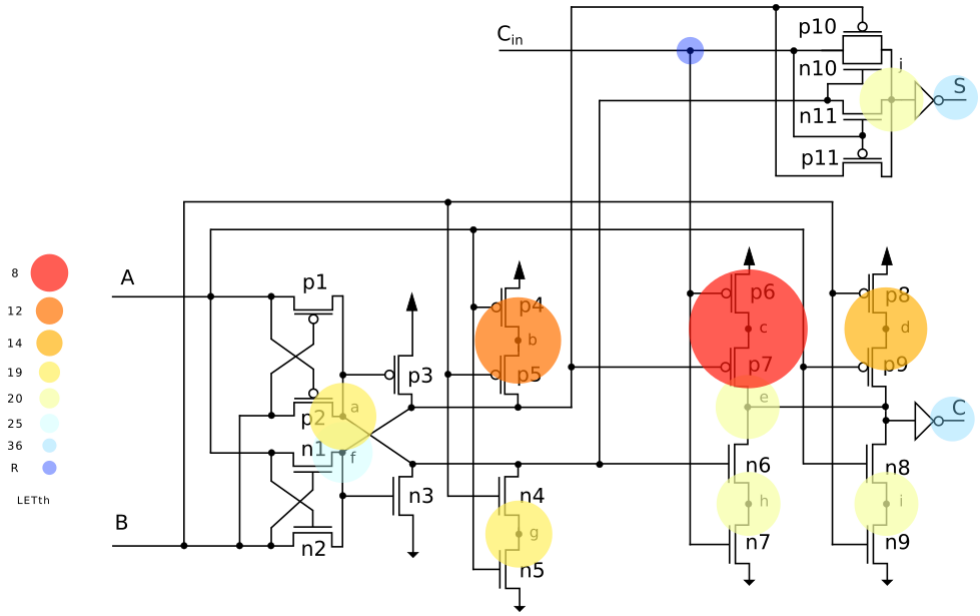
Moving on to the Hybrid FA configuration, Figure 12 offers a detailed illustration of critical nodes, among which node *c* stands out as the most sensitive. With an LETth of 8 $MeVcm^2/mg$, node *c* is identified as the critical node, signifying its heightened susceptibility to SET. Nodes *c* stands out as the most critical component, demonstrating the lowest LETth values of 8 $MeVcm^2/mg$. This node exhibit a heightened vulnerability to radiation-induced disturbances, suggesting that it is less resilient under adverse conditions. Nodes *b* and *d* also emerge as sensitive components with LETth values of 12 and 14 $MeVcm^2/mg$, respectively. Although they are more resilient than node *c* their lower LETth values indicate a notable susceptibility to radiation-induced errors. All the other nodes display a moderate sensitivity with an LETth value higher than 20 $MeVcm^2/mg$, indicating a capacity to withstand radiation-induced effects to a reasonable extent.

In essence, the Hybrid FA demonstrates varying levels of sensitivity among its nodes. Node *c* appear as the most critical and less resilient components, while nodes *b* and *d* also exhibit notable sensitivity. Nodes *Sum* and *Cout* stand out as less susceptible components in the context of radiation-induced effects, similar to the Mirror FA. This analysis gives valuable insights into the Hybrid Full Adder performance under different radiation pulse inputs.

This sensitivity analysis not only informs about vulnerability in specific nodes but also sets the stage for further exploration into mitigation strategies tailored to enhance the robustness of these critical nodes. As we delve deeper into our study, we aim to correlate these critical nodes with observed errors and investigate potential circuit-level techniques to mitigate the impact of SETs on each FA topology.

The analysis of the lowest LET values in the TGA full adder reveals critical nodes that are less resilient to radiation-induced errors. In the Figure 13, the lowest LET values

Figure 12 – Hybrid Full Adder critical nodes at nominal voltage.



Source: The author.

for each node are highlighted, shedding light on the nodes that are more prone to radiation-induced errors. Examining the results, the nodes associated with the outputs *Sum* and *Cout* exhibit particularly low LET values. Specifically, these two output nodes stands out with the lowest LET value of 22 $MeVcm^2/mg$, making it a critical node in terms of susceptibility to SET errors. Additionally, node *g* also demonstrate relatively low LET values, emphasizing its vulnerability to radiation-induced disturbances. Conversely, nodes *h* and *b* exhibit higher LET values, suggesting a greater resilience to transient events. These nodes can be considered more robust in the face of ionizing particles.

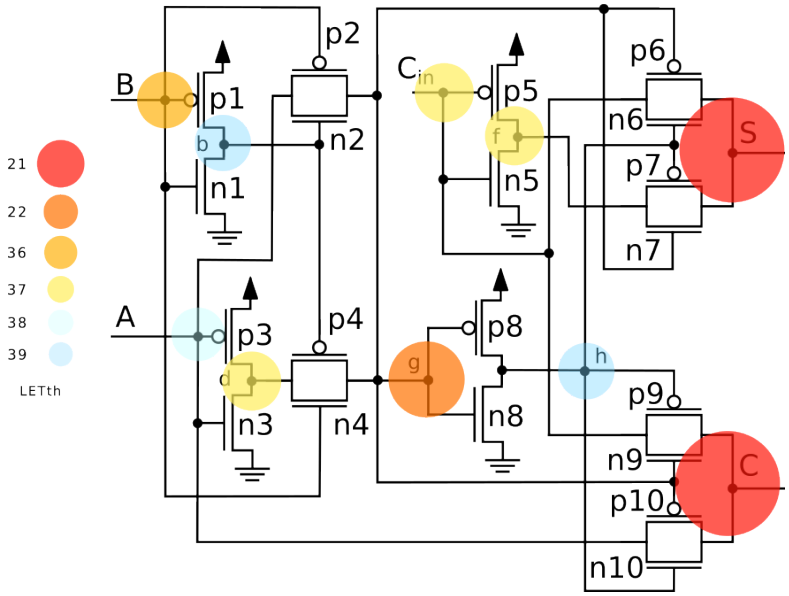
To summarize, the vulnerability of the TGA full adder to radiation-induced errors is highlighted by the lowest LET values, with nodes *Sum* and *Cout* being the critical points of concern. Unlike the two previous topologies, the outputs stand out as critical points. This can be attributed to the absence of a buffer structure in the outputs and the utilization of Pass Transistor Logic.

The examination of the lowest LETth values in the TFA full adder unveils node *Sum* with heightened sensibility to generate errors. In the provided Figure 14, the LETth associated with this output emerges as critical point due to their notably low LET value of 14 $MeVcm^2/mg$, indicating reduced resilience to ionizing particle impacts.

Moreover, nodes *e* and *Cout* are among the critical ones presenting the low LET values, with values of 19 and 21 $MeVcm^2/mg$, respectively. These LET values designate these nodes as particularly susceptible to radiation-induced disturbances, making them critical areas of concern in terms of reliability.

On the other hand, nodes *b* and *f* display higher LET values of 43 and 42, indicating a relatively greater resilience to propagate SETs. These nodes can be viewed

Figure 13 – TGA Full Adder critical nodes at nominal voltage.

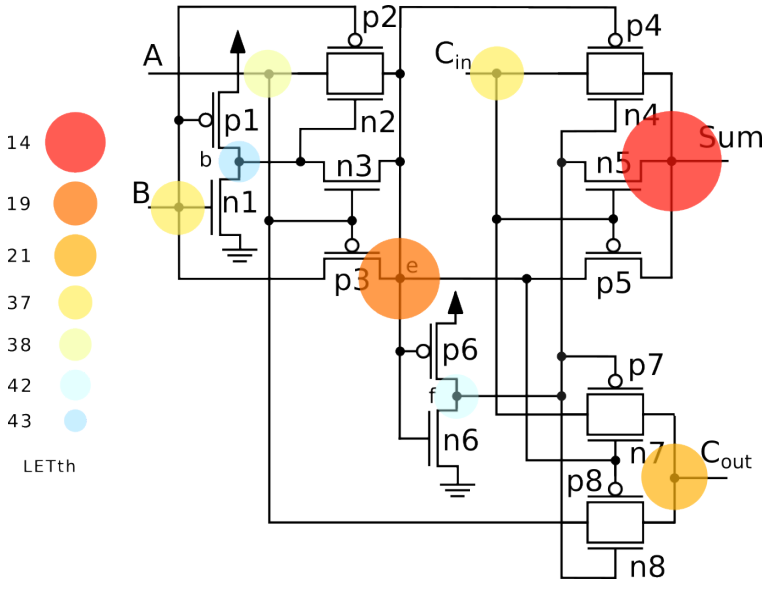


Source: The author.

as more robust within this topology when facing radiation-induced errors.

Summarizing, the analysis of sensitive nodes in the TFA full adder suggests that the output node *Sum* is the critical part for the circuit. Additionally, nodes *e* and *Cout* must be carefully considered in a reliable design due to their low LETth values. This information is crucial for designing circuits that prioritize reliability, especially in areas where radiation exposure is a concern.

Figure 14 – TFA Full Adder critical nodes at nominal voltage.



Source: The author.

Table 10 – Critical Nodes for Each FA Topology Based on Lowest LETth Values

FA Topology	**Critical Nodes (Lowest LETth)**	**LETth**	**Comments**
Mirror FA	*g*, *j*	14 $MeVcm^2/mg$	Most critical: *g*, *j* Moderately critical: *c*, *f*, *h*, *i*, *k*, *l* Less critical: *Sum*, *Cout*
Hybrid FA	*c*	8 $MeVcm^2/mg$	Most critical: *c* Moderately critical: *b*, *d* Others higher than 20
TGA FA	*Sum*, *Cout*	22 $MeVcm^2/mg$	Most critical: *Sum*, *Cout* Moderately critical: *g*
TFA FA	*Sum*, *Cout*	14 $MeVcm^2/mg$	Most critical: *Sum*, *Cout* Moderately critical: *e*

5.1.5 Nominal Voltage Comparison

For the Mirror FA at nominal voltage, nodes *e* and *k* exhibit higher probabilities of generating transient errors. Interestingly, the resilience of the Carry-out internal path compared to the Sum internal circuit is highlighted, indicating potential areas for targeted mitigation efforts. The Hybrid FA, nodes *c* and *d* emerge with the highest error rates. This distribution of error rates provides valuable insights for exploring circuit-level techniques to fortify these vulnerable nodes and enhance overall robustness. In the TGA topology, nodes *h* and *Sum* are more likely to generate errors, highlighting a distinct susceptibility pattern where one output stands out as the most error-prone. Similarly, in the TFA FA, both an output (*Cout*) and an internal node (*e*) exhibit heightened susceptibility to propagate electrical pulses.

The impact of different input vectors on error occurrences provides nuanced insights into specific combinations that significantly influence error rates. For the Mirror FA, vector 011 and vector 100 contribute notably to error propagation, while vector 000 emerges as the critical input combination with the lowest LETth. In the Hybrid FA, vector 000 exhibits the lowest error rate, while vector 001 is identified as the critical vector due to its lowest LETth. The input most susceptible to propagate errors is 011. For the TGA topology, critical vectors, including 011, 101, 110, and 111, all result in a high logic level in the *Cout* output. Among them, vector 011 stands out as the most susceptible combination for generating errors. Lastly, the TFA topology also highlights vector 011 as the most susceptible to propagate errors, but the lowest LETth values are observed during the 010 and 100 input combinations. These results consistently indicate that the 011 vector is prone to errors across the evaluated topologies in this study. Enhancements to its datapath could potentially contribute to circuits that are

more reliable in the presence of radiation-induced events.

In the Mirror FA, the n-hit stands out as critical, associated with the lowest LETth and contributing to the majority of errors. Similarly, in the Hybrid FA, most errors occur during n-hit, emphasizing its pivotal role in influencing the overall error profile. The TGA topology also exhibits a similar trend, with pulse n-hit being responsible for the majority of errors and showing the lowest LETth values. However, in the TFA topology, both hit types present approximately the same error rate on average, becoming an exception to the observed patterns.

In the Mirror FA, nodes *g* and *j* are highlighted as critical due to their remarkably low LETth values, setting the stage for further investigation into targeted mitigation strategies for these nodes. Similarly, in the Hybrid FA, node *c* stands out as the most sensitive, underscoring its heightened susceptibility to SET. In the TGA topology, both outputs, *Sum* and *Cout*, play a significant role in error propagation, exhibiting the lowest energy interactions. Similarly TFA topology presented *Cout* as the critical vector, despite *Sum* output also be among the critical LETth observed.

In summary, this analysis provides a comprehensive perspective on the vulnerabilities and sensitivities parts of the topologies investigated to SETs. The results provide insights into specific sections of the circuits that are more susceptible to mitigation strategies, contributing to the advancement of more robust and resilient integrated circuits across diverse radiation scenarios.

5.2 NEAR THRESHOLD VOLTAGE

Reducing the voltage operation may impose side effects such as lowering frequency operation, increasing leakage power, and increasing the sensitivity of the soft error. In Near-threshold Voltage operation, the supply voltage is set very close to or just slightly above the threshold voltage of the transistors, often referred to as "subthreshold" operation. Operating a circuit in this region allows low power consumption but also presents challenges due to the decreased signal-to-noise ratio, slower operation, and increased susceptibility to variations such as process, temperature, and supply voltage variations. NTV operation is often used in applications where power efficiency is critical. In the context of the technology employed in this work, the NTV is set to 0.35V.

5.2.1 Error Rate

The total error occurrences for the Mirror FA at NTV saw a significant increase of nearly 19% compared to the results observed during nominal voltage operation. Examining the LETth results for both outputs reveals that node *c* exhibits a heightened susceptibility to generating SETs, as Table 11 shows. Node *c* is accountable for approximately 11% of all computed errors. Additionally, nodes *d*, *h*, and *i* emerge as prominent

contributors to generating interference on the outputs.

Table 11 – LETth for all nodes of Mirror FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	NTV													
		a	b	c	d	e	f	g	h	i	j	k	l	Sum	Cout
010	000	-	-	-	-	-	-	-	11	21	69	9	14	-	4
	001	-	-	78	40	-	-	2	11	-	19	8	12	-	4
	010	-	-	78	38	-	-	2	28	-	19	7	9	-	4
	011	39	41	-	-	-	2	-	11	24	44	-	-	4	-
	100	-	-	79	2	-	-	2	-	29	19	11	21	-	4
	101	2	41	-	-	-	2	-	22	24	44	-	-	4	-
	110	5	2	-	-	-	2	-	27	38	45	-	-	4	-
	111	-	-	2	5	-	-	2	-	-	-	9	-	-	-
101	000	85	-	48	-	-	3	**1**	7	10	**1**	2	4	-	-
	001	20	35	35	-	-	2	-	4	2	-	-	-	3	93
	010	48	21	36	-	-	2	-	2	46	-	-	-	3	93
	011	-	-	16	19	-	-	2	-	-	87	2	2	-	3
	100	66	21	36	41	-	2	-	44	46	-	-	-	3	92
	101	40	-	16	10	-	-	2	-	-	86	2	42	-	3
	110	21	60	15	11	-	-	2	-	-	86	25	44	-	3
	111	42	31	80	14	-	-	-	-	-	-	-	-	3	3

*Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Analyzing the Hybrid FA at NTV results from Table 12, nodes *a*, *b*, *d*, *f*, and *g* exhibit considerable susceptibility to error generation, each contributing at a rate close to 10%. Collectively, these nodes account for nearly 50% of the total error occurrences. In contrast, node *d* demonstrated the highest error rates, establishing them as the most susceptible nodes to error generation, representing approximately 12% of the total error occurrences observed at NTV. When comparing the error rate observed at nominal voltage with those at NTV, there is a notable increase of 33% in the observed errors.

Table 12 – LETth for all nodes of Hybrid FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	NTV												
		a	b	c	d	e	f	g	h	i	j	Cin	Sum	Cout
010	000	59	-	-	-	-	-	70	-	-	54	-	4	4
	001	10	-	-	-	-	60	14	43	-	**2**	-	-	4
	010	62	36	-	-	-	3	68	8	21	5	-	-	4
	011	-	35	**2**	**2**	**2**	**2**	68	20	32	-	-	4	-
	100	61	3	-	-	-	3	20	8	8	5	-	-	4
	101	-	**2**	**2**	39	**2**	**2**	44	20	10	-	-	4	-
	110	7	-	37	4	**2**	-	97	-	19	-	-	4	-
	111	17	94	4	4	**2**	42	-	97	19	3	-	-	-
101	000	45	-	74	13	**2**	12	94	3	3	**2**	-	-	-
	001	-	83	92	13	**2**	5	-	42	3	-	-	3	-
	010	**2**	61	15	10	**2**	-	**2**	**2**	43	-	-	3	-
	011	**2**	18	9	45	-	62	**2**	-	-	3	-	-	3
	100	**2**	44	15	26	**2**	-	41	**2**	**2**	-	-	3	-
	101	**2**	47	9	18	-	63	41	-	-	3	-	-	3
	110	68	14	30	56	-	6	-	-	-	**2**	-	-	3
	111	-	58	-	46	-	54	-	-	-	55	-	3	3

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Reducing the voltage operation led to a 39% increase in error occurrence for

the TGA topology, as Table 13 shows. Node *b* emerged as the most susceptible to generating errors, exhibiting a slight 1% increase compared to nodes *h* and *Sum*, which were critical in the nominal voltage operation. Despite this minor difference in NTV operation, nodes *h* and *Sum* can still be considered the most susceptible to generating errors. Additionally, nodes *Cout* and *e* should be included in the critical set for this topology due to their increased sensitivity under reduced voltage conditions.

Table 13 – LETth for all nodes of TGA FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	NTV									
		B	b	A	d	Cin	f	g	h	Sum	Cout
010	000	4	95	5	37	5	34	3	-	**2**	**2**
	001	4	95	5	37	39	-	3	-	63	**2**
	010	-	4	4	-	5	38	-	4	21	**2**
	011	-	4	4	-	57	4	-	4	**2**	28
	100	4	95	-	-	5	38	-	4	21	**2**
	101	5	-	-	-	64	4	-	5	**2**	-
	110	-	5	46	5	5	34	3	98	**2**	28
	111	-	6	50	5	-	-	3	98	-	-
101	000	-	3	-	-	-	-	-	3	-	-
	001	-	3	-	-	3	39	-	3	**2**	64
	010	3	86	52	3	47	3	**2**	89	**2**	72
	011	3	86	47	3	3	39	**2**	90	22	**2**
	100	-	10	4	41	3	39	**2**	90	22	4
	101	**2**	47	9	18	-	63	41	-	-	3
	110	3	86	3	37	45	-	21	3	67	**2**
	111	3	86	3	37	3	39	21	4	**2**	**2**

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

The TFA FA exhibited a significant deterioration in error rates, showing an increase of over 54% in errors, as outlined in Table 14. This substantial rise in the total error renders the TFA topology the most sensitive among our FA set. Notably, node *e* emerged as the most susceptible to propagate SET, contributing 14% to the total errors. Additionally, nodes *b* and the output *Cout* played critical roles, each contributing 13% to the overall errors. This heightened vulnerability of specific nodes emphasizes the importance of targeted mitigation strategies for enhancing the robustness of the TFA FA under reduced voltage operations.

5.2.2 Input Vectors

In the examination of input vector combinations for the Mirror FA, it becomes evident that vector 100 holds the highest susceptibility to error generation, as Table 11 shows. Additionally, vectors 001 and 010 contribute significantly to error propagation, collectively representing over 46% of the total SET occurrences. Conversely, the vector 000 attains the lowest LETth, designating it as the critical input combination for the Mirror topology.

Turning attention to the Hybrid FA, input vectors 010, 011, 100, and 101 share a common error rate occurrence of 14%, signifying their heightened susceptibility to

Table 14 – LETth for all nodes of TFA FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	NTV							
		B	b	A	Cin	e	f	Sum	Cout
010	000	6	95	6	4	3	-	2	2
	001	5	95	5	73	3	-	50	2
	010	-	4	4	5	75	4	62	2
	011	44	4	4	59	23	5	2	28
	100	5	94	-	5	78	4	63	2
	101	4	95	49	76	23	5	2	-
	110	45	5	48	4	3	98	2	27
	111	44	5	50	-	2	97	-	94
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	3	82	4	2	65
	010	3	42	55	47	2	36	**1**	79
	011	3	39	48	3	2	78	63	2
	100	-	5	4	43	2	36	**1**	28
	101	-	5	4	3	2	73	61	2
	110	3	80	3	53	56	4	56	2
	111	3	80	3	3	56	5	2	2

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

generating errors in this topology outputs. These vectors also correspond to the generation of the lowest LETth values, establishing them as the most sensitive ones for this topology. On the other hand the input vector 000 stands out with the lowest error rate, constituting a mere 8% of the total error occurrences.

For the TGA topology, the analysis in Table 13 reveals that 16% of the errors occur during the 011 input combination, making this vector the most sensitive. However, it is noteworthy that several other vectors, including 001, 010, 011, 100, 101, and 111, exhibit the lowest LETth value of 2 $MeVcm^2/mg$. This suggests that nearly all input vectors are susceptible to propagating errors, depending on the specific node impacted by the radiation particle. Similar to the Hybrid and Mirror topologies, vector 000 demonstrates the lowest error rate.

The TFA topology experiences a significant impact when the voltage is reduced, as illustrated in Table 14. Input vectors 010 and 100 exhibit a critical LETth of only 1 $MeVcm^2/mg$. Despite these two critical input combinations, vector 011 generates up to 21% of the total errors observed, establishing itself as the most sensitive input vector for the topology.

5.2.3 Hit Type

In the evaluation of SET pulse types, the Mirror Full Adder maintains the n-hit as the critical one, constituting up to 58% of the total observed SET episodes for the combined Sum and Cout outputs. Additionally, this hit type consistently generates the lowest LETth values on average for both outputs.

For the Hybrid FA, the n-hit exhibits a slightly higher error rate when compared with pulse p-hit. Notably, n-hit is responsible for the critical LETth values, both in terms of generating the highest error rate and holding the lowest LETth values on average.

Specifically, 58% of errors in the Hybrid FA occur during the n-hit. Furthermore, this hit type also contributes to the circuit's critical LETth value during nominal operation.

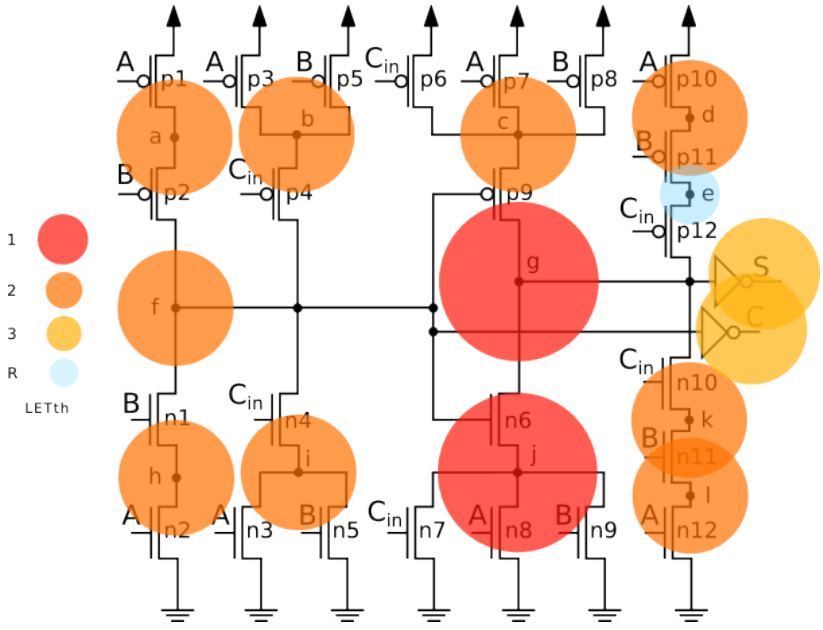
In the TGA topology, the n-hit continued to exhibit the highest susceptibility, contributing to 53% of the total error occurrence. Interestingly, both hit types generated critical LETth values, particularly when the particle strike was applied to the *Sum* node. This indicates that the *Sum* node is sensitive to both n-hit and p-hit in this topology.

In contrast to the nominal voltage operation and the other topologies, errors generated by the n-hit significantly increase for the TFA topology at NTV, accounting for nearly 53% of the total errors observed. However, it is noteworthy that for this FA the hit high-to-low is responsible for generating all the critical LETth values during the simulations.

5.2.4 Critical Nodes

In the context of the Mirror FA, Figure 15 highlight that nodes *g* and *j* stand out for exhibiting the lowest LETth values, rendering them particularly sensitive to SETs. Additionally, dropping the voltage operation resulted in a substantial 14 times worsening in the LETth values observed for this two critical nodes, decreasing it from 14 $MeVcm^2/mg$ in the nominal to 1 $MeVcm^2/mg$ in NTV operation. These observation aligns with the nominal operation, emphasizing that mitigating techniques applied to these internal nodes could prove more effective in enhancing the overall robustness of the Mirror FA against SETs.

Figure 15 – Mirror Full Adder critical nodes at NTV.



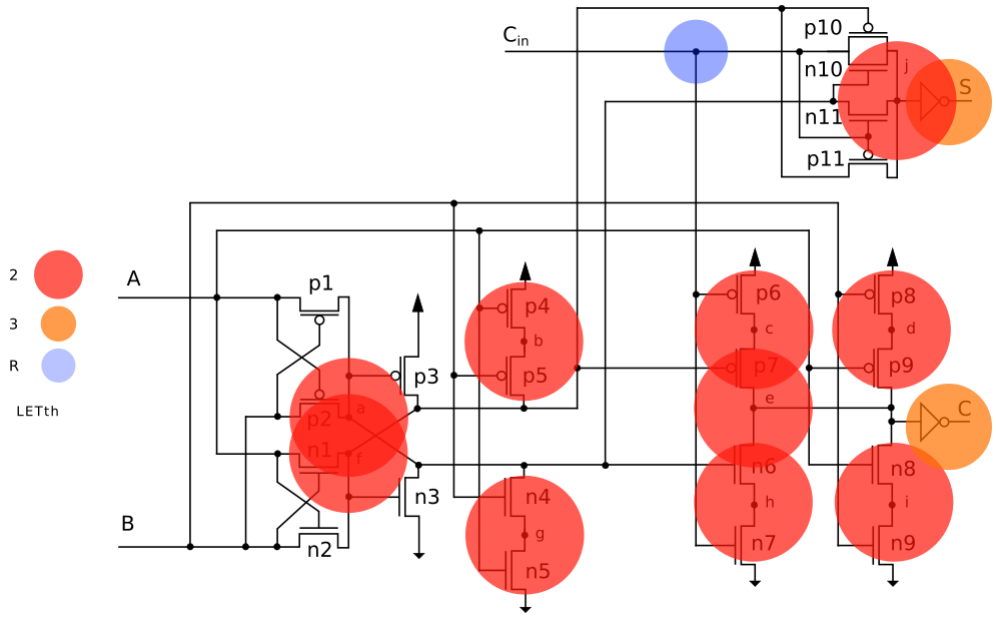
Source: The author.

Shifting focus to the Hybrid FA, it is noteworthy that almost all nodes share a

critical LETth value of 2 $MeVcm^2/mg$ with the exceptions of nodes *Sum*, *Cout*, and *Cin*. Figure 16 illustrates the critical nodes, with node *Cin* presenting the highest LETth value and emerging as the less critical one for this topology. Comparing with the results at nominal voltage operation we could elect nodes *b*, *c*, and *d* possible candidates to apply mitigation techniques in order to reduce SET for this topology at both nominal and NTV operation.

The internal nodes of the Hybrid FA, much like the Mirror FA, display an increased vulnerability and sensitivity to error generation. The utilization of a combination of complementary and PTL in its construction suggests that this may not be the most suitable technique for architectures intended to operate in noisy environments. Another noteworthy aspect for this topology is that the node *Cin* remained unaffected by the reduction in voltage operation, maintaining a LETth value above $100MeVcm^2/mg$.

Figure 16 – Hybrid Full Adder critical nodes at NTV.

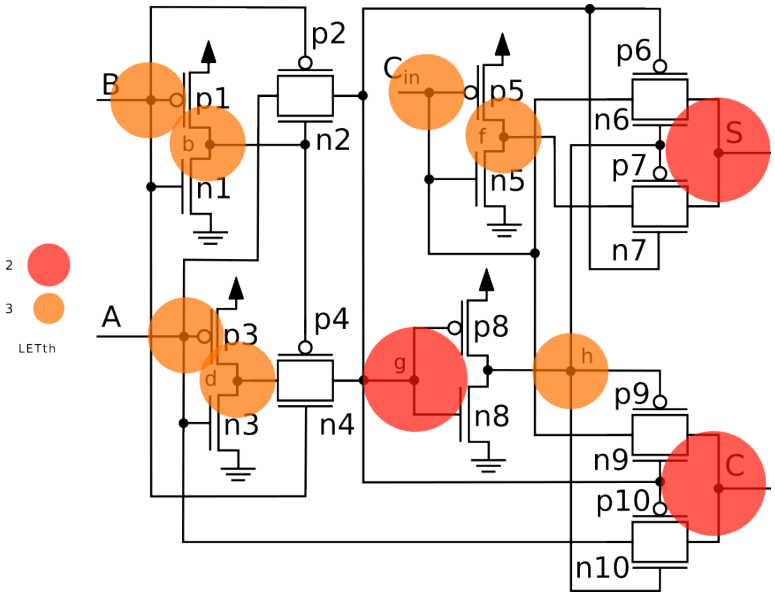


Source: The author.

Upon analyzing the TGA topology, a notably more aggressive reduction in the critical LETth is observed, reaching 2 $MeVcm^2/mg$ when operating at reduced voltage. This signifies a substantial increase of approximately 21 times in sensitivity for the critical nodes at NTV. Remarkably, the critical nodes identified as *Sum* and *Cout* at nominal voltage retained their critical status at NTV. Additionally, node *g* emerged as another critical node, exhibiting the same critical LETth value in this scenario, as Figure 17 shows. This heightened sensitivity in critical nodes underscores the impact of reduced voltage on the vulnerability of the TGA topology to radiation-induced effects.

In the case of the TFA topology, the critical node *Sum* maintained its status unchanged throughout the reduction in voltage operation. Interestingly, the simulation results reveal a substantial 14x decrease in the lowest observed LETth for the *Sum*

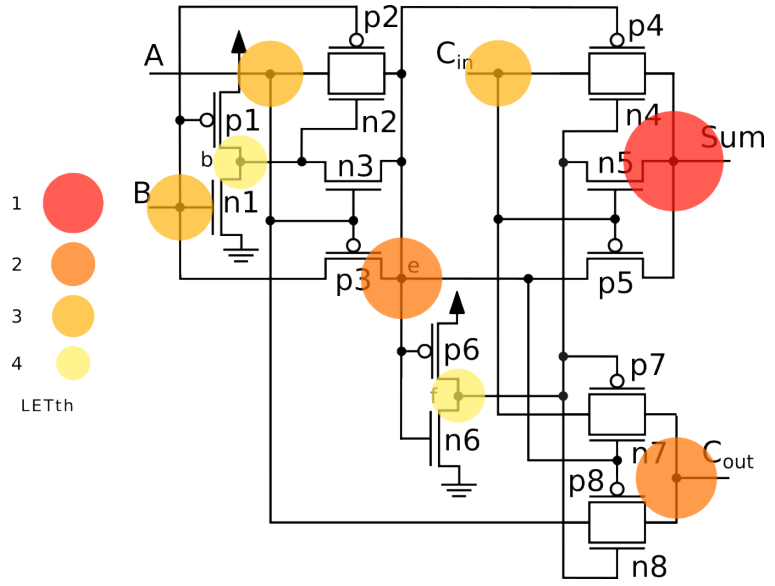
Figure 17 – TGA Full Adder critical nodes at NTV.



Source: The author.

output node. This indicates a heightened sensitivity of the *Sum* node to radiation-induced effects when operating at NTV. Furthermore, the previously moderate node *Cout* has now emerged as one of the critical nodes, exhibiting a LETth of only 2 $MeVcm^2/mg$ at reduced voltage, highlighted in Figure 18.

Figure 18 – TFA Full Adder critical nodes at NTV.



Source: The author.

This significant reduction in LETth for *Cout* underscores its increased susceptibility to SETs under NTV conditions. The observation that all nodes in this topology present LETth values of no more than 4 $MeVcm^2/mg$ highlights the overall sensitivity of the TFA architecture when operating at NTV. This sensitivity underscores the impor-

tance of carefully considering mitigation strategies to enhance radiation resilience in such scenarios.

5.3 NEAR-THRESHOLD VOLTAGE COMPARISON

NTV operation introduces distinct vulnerabilities in all FAs, highlighting variations in critical nodes, input vectors, and SET hit types. These insights inform the tailoring of circuit-level mitigation strategies for enhanced robustness also under NTV conditions.

For the Mirror FA at NTV, nodes *c*, *d*, *h*, and *i* are identified as the most susceptible to generating interference, with node *c* being particularly noteworthy, contributing nearly 11% of all errors computed. The Hybrid FA at NTV exhibits different vulnerable nodes, with nodes *a*, *b*, *d*, *f*, and *g* collectively representing almost half of total error occurrences. In comparison, node *d* present the highest error rates, constituting approximately 12% of total errors at nominal voltage. In the TGA topology, node *b* is the most likely to generate errors; however, both *h* and *Sum* exhibit similar sensitivity and could be considered as potential points for improvement. In conclusion, for the TFA topology, node *e* is the most susceptible to propagating errors, contributing nearly 14% to the total errors. However, nodes *b* and *Cout* should also be considered when applying mitigation techniques, despite their relatively high susceptibility.

In terms of input vectors, different combinations show varying error rates. In the Mirror FA at NTV, vector 100 stands out as the most error-prone, while the critical LETth values were observed for vector 000. In the case of the Hybrid FA, vectors 010, 011, 100, and 101 exhibit similar error rates, with vector 001 having the lowest LETth. For the TGA topology, vector 011 proves to be the most susceptible to propagating SETs, although almost all other vectors show critical LETth values for this topology at NTV. Lastly, in the TFA circuit, vector 011 generates more errors on average, and the lowest LETth values are present in vectors 010 and 100 conditions. Another point to highlight is that vector 00 is the least likely to contribute to propagating errors for all the analyzed topologies.

For the SET hit types, the n-hit continues to be critical for the Mirror FA, accounting for up to 58% of total SET episodes. In the Hybrid FA, pulse n-hit is slightly more error-prone than p-hit, contributing also to 58% of errors. For the TGA topology, n-hit remains the most susceptible to propagation across the circuit. Interestingly, unlike the other topologies, lowering the voltage operation makes the TFA circuit more prone to propagate low-to-high hits.

In the Mirror FA, nodes *g* and *j* prove to be the most sensitive, each with a LETth of only 1 $MeVcm^2/mg$—the lowest across all topologies in this study. The Hybrid FA demonstrates the most significant increase in sensitivity, as nearly all internal nodes now possess the lowest LETth for this topology. On the other hand, while the TGA topology becomes more sensitive, it retains the nominal behavior with nodes *Sum* and

Cout as the critical ones, now with the addition of node *g*. Finally, the TFA exhibits a similar pattern, preserving the critical nodes *Sum*, *e*, and *Cout* found in nominal operation, albeit with lower LETth values required for propagation across the topology network.

In conclusion, the analysis of NTV operation across the topologies reveals notable shifts in the susceptibility of nodes and overall sensitivity to SETs. Lowering the voltage introduces increased error rates, impacting critical nodes in each topology. The Mirror FA exhibits a drastic reduction in LETth values, particularly in nodes *g* and *j*, emphasizing the need for targeted mitigation strategies for these sensitive components. The Hybrid FA displays heightened sensitivity across its internal nodes, suggesting potential challenges in noisy environments. The TGA topology maintains critical nodes *Sum* and *Cout*, with additional sensitivity introduced in node *g*. Conversely, the TFA experiences a significant increase in error rates, with node *e* emerging as the most susceptible, reinforcing the importance of tailored mitigation approaches. Overall, the NTV operation analysis underscores the intricate interplay between voltage levels and the susceptibility of nodes, providing valuable insights for enhancing the radiation resilience of integrated circuits.

5.4 NOMINAL VS NEAR-THRESHOLD VOLTAGE COMPARISON

Examining circuits across diverse corner scenarios sheds light on potential techniques to enhance robustness in both operational contexts. This analysis seeks to uncover the nuances of how circuits react to varying voltage conditions. Identifying critical nodes, components, and operational behaviors becomes crucial in this exploration. These insights are fundamental for customizing effective mitigation strategies to fortify the resilience of FA circuits across diverse scenarios operation. The results find across both voltage scenarios are summarized in Table 15.

When comparing the two voltage operations for the Mirror FA, the most susceptible node can vary depending on the scenario analyzed. However, it is noteworthy that the node *Cout* consistently exhibits the highest susceptibility rate in both scenarios. On the other hand, nodes *k* and *l* also warrant attention for improving robustness regarding voltage operations due to their high susceptibility to propagate radiation events. In the case of the Hybrid FA, error susceptibility is more balanced among nodes, with several nodes exhibiting approximately the same error rate. Notably, among the different voltage scenarios analyzed, nodes *a*, *c*, *d*, and *f* stand out as the most susceptible to propagate interference noise to the outputs. Examining the TGA topology reveals that, despite some nuances across different voltage operations, nodes *b*, *h*, *sum*, and *cout* consistently remain among the most susceptible nodes to propagate SET errors. In the case of the TFA topology, nodes *d*, *e*, and *cout* consistently maintained critical values. It is noteworthy that node *e* remained the most susceptible to propagate errors

regardless of the voltage operation.

In terms of input vectors, different combinations show varying error rates. In the case of the Mirror FA at NTV, vector 100 emerges as the most error-prone. For the Hybrid FA, vectors 010, 011, 100, and 101 exhibit similar error rates. The TGA topology indicates that vectors 010 and 011 have higher error rates. In contrast, the TFA topology shows that vectors 010 and 011 are more prone to propagating errors. Critical input vectors are identified as follows: 000 for the Mirror FA, 001 for the Hybrid FA, and, for the TGA, all inputs except for vectors 00 and 101 can propagate the lowest LETth values. Lastly, the TFA topology designates vector 100 as the critical input, as it consistently results in the lowest LETth values across experiments.

Concerning SET hit types, the n-hit consistently emerges as critical for all topologies analyzed under both voltage operation conditions, except for the TFA topology in NTV operation, where the pulse n-hit exhibits a higher error rate. However, it is noteworthy that the critical LETth values are predominantly generated by the n-hit across the various scenarios.

Critical nodes vary between the FA topologies. For the Mirror FA, nodes *g* and *j* remain the most sensitive in both voltage operations. In the Hybrid FA, despite a higher increase in critical nodes in NTV, nodes *c* and *d* consistently exhibit the lowest LETth in both scenarios. In the TGA topology, nodes *Sum* and *Cout* consistently emerge as critical in propagating SETs regardless of the voltage scenario. Finally, for the TFA, nodes *e* and *Sum* stand out as critical nodes, presenting the lowest LETth values in both scenarios.

In conclusion, the voltage comparison across various FA topologies revealed nuanced sensitivities and critical nodes under different operating conditions. Each topology exhibited distinct responses to voltage variations, emphasizing the importance of tailored mitigation strategies. Analyzing these scenarios provides valuable insights into our investigation to explore strategies to optimize robustness and reliability in integrated circuits facing diverse voltage conditions, contributing to the advancement of radiation-hardened circuit design.

Table 15 – Comparison of sensitive nodes, critical nodes, critical input vectors, and critical hit types for each FA topology under nominal and NTV operations.

FA Topology	**Sensitive Nodes (Error Rate)**	**Critical Nodes (Lowest LETth)**	**Critical Vectors**	**Critical Hit Type**
Mirror FA (Nominal)	*k* (13% of errors)	*g*, *j* (14 MeVcm^2/mg)	000	n-hit
Mirror FA (NTV)	*c* (11% of errors)	*g*, *j* (1 MeVcm^2/mg)	100	n-hit
Hybrid FA (Nominal)	*c*, *d* (20% of errors)	*c* (8 MeVcm^2/mg)	001	n-hit
Hybrid FA (NTV)	*d* (12% of errors)	*almost all nodes* (2 MeVcm^2/mg)	010, 011, 100, 101	n-hit
TGA FA (Nominal)	*h*, *Sum* (28% of errors)	*Sum*, *Cout* (22 MeVcm^2/mg)	011	n-hit
TGA FA (NTV)	*b* (11% of errors)	*Sum*, *Cout*, *g* (2 MeVcm^2/mg)	011	n-hit
TFA FA (Nominal)	*e*, *Cout* (14% of errors)	*Sum* (14 MeVcm^2/mg)	010, 100	n-hit, p-hit
TFA FA (NTV)	*e* (14% of errors)	*Sum* (2 MeVcm^2/mg)	011	n-hit

6 SET MITIGATION TECHNIQUES

The previous evaluation shows the SET sensibility of the FA considered in this work, even adopting a multigate technology. Thus, mitigation techniques must be explored in the design to reach more elevated levels of SET robustness. This study delves into the application of Transistor Sizing and Decoupling Cells, both independently and in combination, targeting the most sensitive nodes within these circuits.

The presentation of mitigation technique results will mirror the structure of Chapter 5. The mitigation scenarios, summarized in Table 16, illustrate different approaches to enhancing the SET robustness of FAs under nominal and NTV operations. The table outlines the three primary mitigation techniques: the use of DCELL, TS, and a combination of both. For the DCELL scenario, one fin is applied to all transistors in both the full adders and the decoupling cells, which are inserted at each target node, not just on the the outputs. In the TS scenario, all transistors in the FAs are resized to three fins, while the TS + DCELL scenario combines the resizing of all transistors to three fins with the insertion of decoupling cells, also at three fins, at each target node. These configurations will be evaluated and presented to highlight the impact of each mitigation technique on the robustness of the circuits under different voltage conditions. The subsequent section will delve into results for the NTV operation. A concluding section will offer an overall comparison between the two voltage operations.

Table 16 – Summary of mitigation scenarios for nominal and NTV operations

Mitigation Scenario	Nominal Voltage	NTV Operation
DCELL	• **FAs nº fins**: 1 fin • **DCELL nº fins**: 1 fin	• **FAs nº fins**: 1 fin • **DCELL nº fins**: 1 fin
TS	• **FAs nº fins**: 3 fins	• **FAs nº fins**: 3 fins
TS + DCELL	• **FAs nº fins**: 3 fins • **DCELL nº fins**: 3 fins	• **FAs nº fins**: 3 fins • **DCELL nº fins**: 3 fins

**DCELL are always inserted in the critical nodes under test.

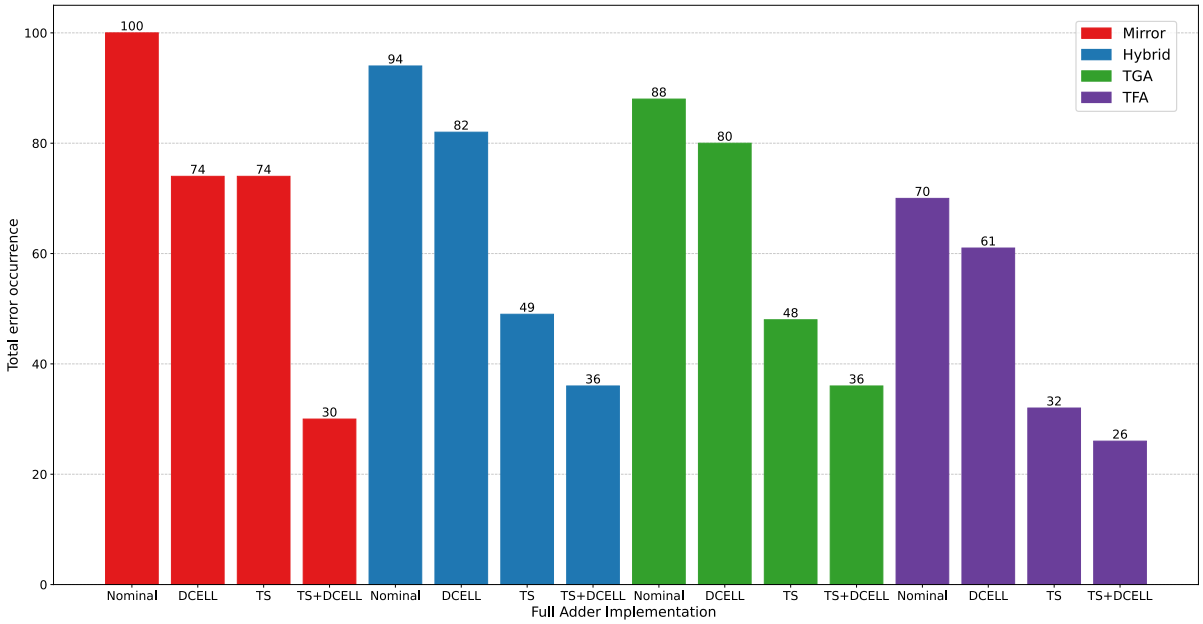
6.1 RESULTS ANALYSIS

For the SET mitigation techniques, the results will be presented in a consistent structure: first, error rate results; then input vectors; hit-type; and finally, critical nodes. Differently from the previous chapter, each section will now present results for nominal voltage and near-threshold voltage together.

6.1.1 Error Rate

Observing the total error occurrence among the topologies, it is evident that at nominal voltage operation, the Mirror FA exhibited a reduction of almost 26% when applying DCELL or TS. However, combining both techniques resulted in up to a 70% decrease in errors, as highlighted in Figure 19. For the Hybrid FA, using the DCELL technique provided a reduction of approximately 13%, while employing TS led to a reduction of about 49%. The most significant improvement for the Hybrid topology was achieved by combining TS and DCELL, resulting in a remarkable 68% reduction in errors. The TGA also showed a modest reduction in total errors when using DCELL, around 5%. However, employing the TS technique increased this reduction to up to 45%. Furthermore, the most substantial improvement was observed when both techniques were combined for this topology, resulting in almost a 60% reduction in errors. Finally, for the TFA, similar behavior for the last topologies was observed, with a reduction of approximately 13% when using DCELL, 54% when considering sizing adjustments, and nearly 63% fewer errors when combining both techniques.

Figure 19 – Total error for all topologies at nominal voltage.

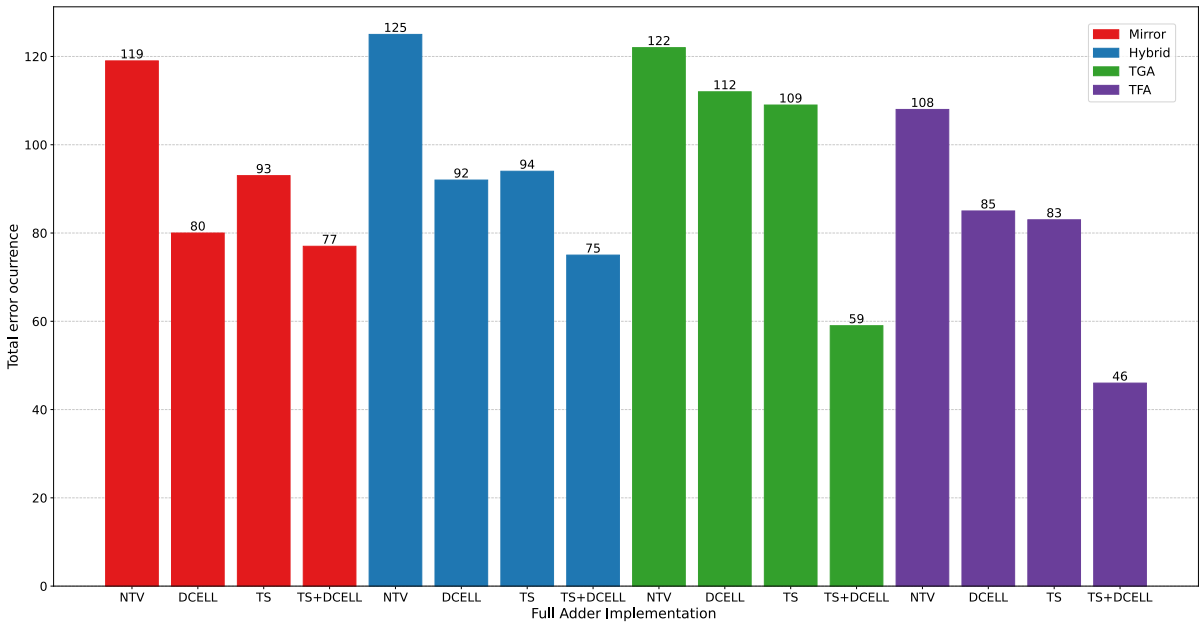


Source: The author.

Reducing the voltage operation amplifies the sensitivity of the circuits, as discussed in Chapter 5, underscoring the need for effective mitigation techniques. In the case of the Mirror FA at NTV, the application of DCELL results in a reduction of total errors by up to 32%, as presented in Figure 20. The TS technique exhibits a more modest decrease of nearly 22% in the error count. The most promising results are achieved by combining both techniques, yielding a reduction of up to 35%. For the Hybrid FA at NTV, there is an increase close to 33% in the total error occurrence compared to

nominal values without mitigation techniques. The application of DCELL on the target nodes for this topology results in a 26% decrease in the total error count, while sizing the transistors reduces it by almost 25%. The most favorable outcomes are observed when combining both techniques, achieving a total reduction of 40% in the error count. The TGA topology at NTV presented an expressive increase of almost 39% in the total number of errors compared to its implementation at nominal voltage. The use of DCELL for this topology reduced the total error occurrence by only 8%. Similarly, the use of TS reduced the errors by close to 11%. The best outcome for the TGA was achieved by combining both techniques, resulting in an expressive reduction of close to 52% in the propagated errors. For the TFA topology at NTV, the observed errors were 54% larger than its implementation at nominal voltage, making it the critical topology when comparing to switching to lower voltage operation. The usage of DCELL helps to reduce the errors by up to 21%, while sizing the transistors yields similar results with a reduction of 23%. Following the same trend as previous topologies, the best results were found when combining both techniques, with a significant reduction of up to 44%. Despite the voltage reduction potentially increasing the number of propagated errors, the results show that the use of mitigation techniques still can help improve sensitivity while preserving the potential reduction in power consumption that working at NTV can provide.

Figure 20 – Total error for all topologies at NTV.



Source: The author.

When considering the impact of these techniques, it becomes evident that a combination of DCELL and sizing adjustments consistently yields the most substantial reduction in total errors across all topologies in the two voltage operation evaluated.

This combined approach leads to a remarkable decrease in errors, showcasing its effectiveness in enhancing the robustness of the circuits. While individual techniques such as DCELL or sizing adjustments also contribute to error reduction, their impact is notably increased when utilized together. Therefore, for reducing the total error observed, the combination of DCELL and sizing adjustments emerges as the preferred technique in the context of enhancing the reliability of the analyzed topologies.

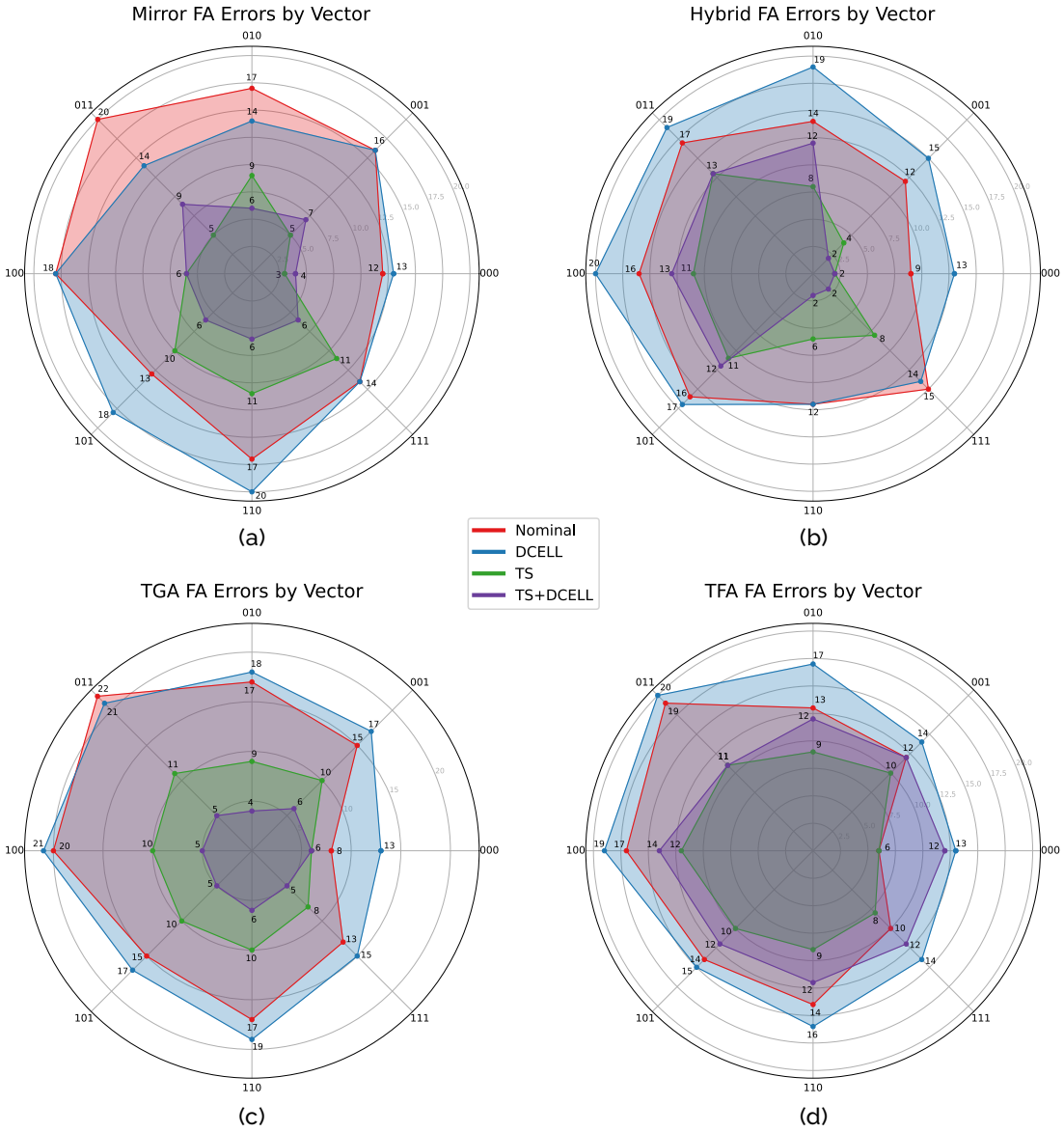
These improvements can be explained because adjusting the transistor sizes can help in reducing the susceptibility of nodes to charge collection caused by ionizing radiation. By resizing transistors appropriately, the charge collection in sensitive nodes can be minimized, thereby reducing the likelihood of SET occurrence. Furthermore, capacitive decoupling methods like DCELL help in stabilizing the voltage levels in critical nodes by providing additional capacitance. This helps in mitigating voltage fluctuations caused by radiation-induced charge deposition, thereby ensuring better signal integrity and reducing the likelihood of erroneous state transitions.

6.1.2 Input Vectors

The most susceptible vector to generate an error in the Mirror FA while applying the DCELL technique is 110, this vector contributes for 16% of the total error for the topology. However vectors 001 and 010 has major contributions into propagating the pulse to the outputs. Together they represent close to 30% of the total error occurrence. On the other hand, for the scenario using TS vector 110 and 111 became the most susceptible to generate errors, and when combining both techniques vector 011 is the most sensitive. Except for the TS scenario where the critical LETth were observed for 111 vector, all critical LETth values were generated for the combination 000 in the Mirror topology. Differently, at NVT operation, using DCELL it is possible to observe that vectors 001, 010, and 101 are the most susceptible to generate errors, presenting together up to 42% of the total errors. On the other hand, with TS, the vector 001 generates most errors and when combining techniques vectors 001 and 010 are the ones that generate up to 28%. However, for all scenarios at NTV, vector 000 is the critical one, presented the lowest LETth values despite the mitigation technique at the low voltage operation.

For the Hybrid implementation applying DCELL at nominal operation, vector 100 propagated 20 errors representing up to 26% of the total error occurrence, being the most sensitive ones for this scenario. Vectors 010 and 011 also are among the most susceptible that can propagate errors for the DCELL scenario. Using TS we reduced the total errors and less errors were propagated by each vector, as shown in Figure 21. Sizing the transistors vector 011 became the critical one, propagating close to 21% of the errors observed. Combining both techniques presented the best results in total error occurrence, however vector 011 still represent to be one of the most sensitive one

Figure 21 – Error by Input Vectors at Nominal Voltage.



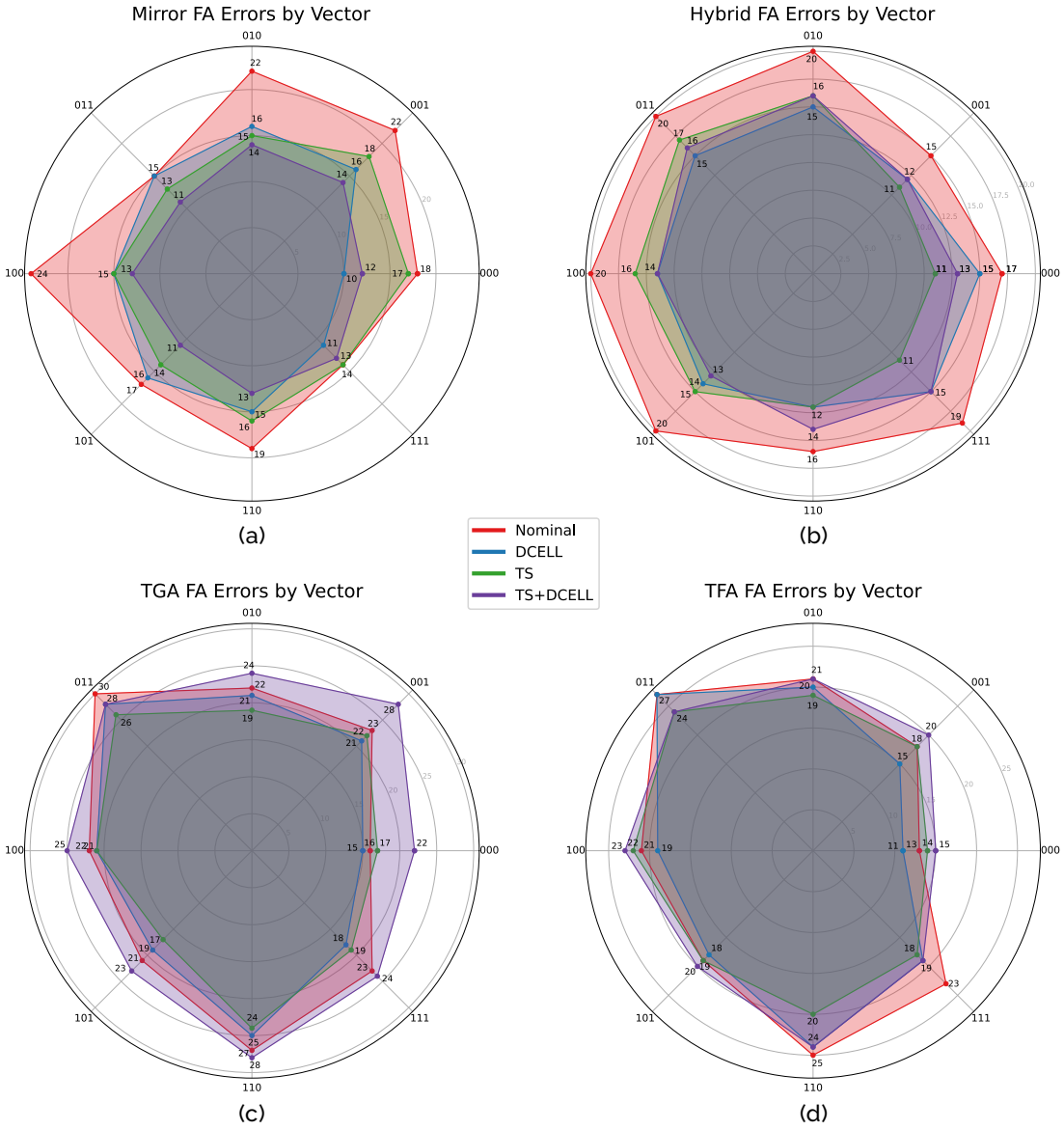
Source: The author.

along the vector 100.

At NTV, using DCELL all vectors present the same susceptibility error rate up to 13% of the total error, except for vectors 001 and 110 which show a smaller rate of close to 12% on average. When using TS at NTV for the Hybrid topology, only vector 011 presents the highest error susceptibility of almost 16%.

On average, for all scenarios vector 010 is the critical vector for the Hybrid FA operating at NTV.

Figure 22 – Error by Input Vectors at NTV.

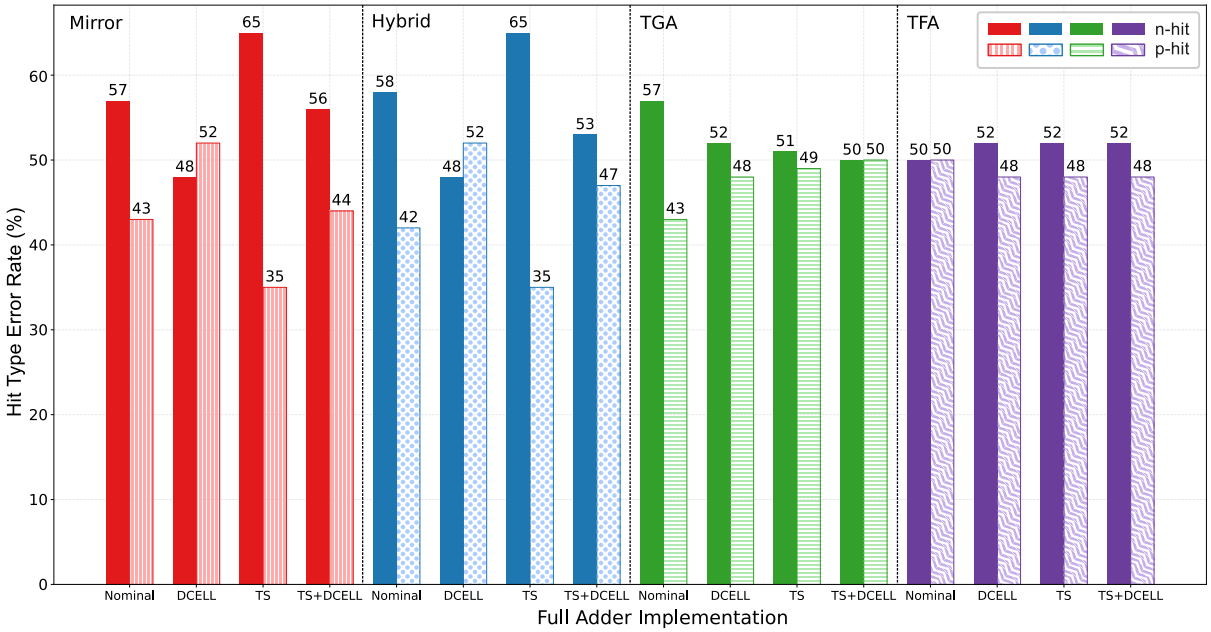


Source: The author.

6.1.3 Hit Type

Analyzing the SET hit type for all the outputs of the Mirror FA applying the DCELL technique at nominal voltage, p-hit is responsible for up to 52% of the total error occurrence, as Figure 23 shows. Despite that, n-hit generates, on average, all the lowest LETth, including the critical value for the circuit. For the TS technique, the n-hit type is responsible for most of the errors, up to 57% of all errors. When combining the techniques also pulse high-to-low is responsible for 56% of the total error. Thus, n-hit is the critical to be considered in this operational mode for Mirror FA despite the mitigation technique used.

Figure 23 – Hit type Error Rate at Nominal Voltage.



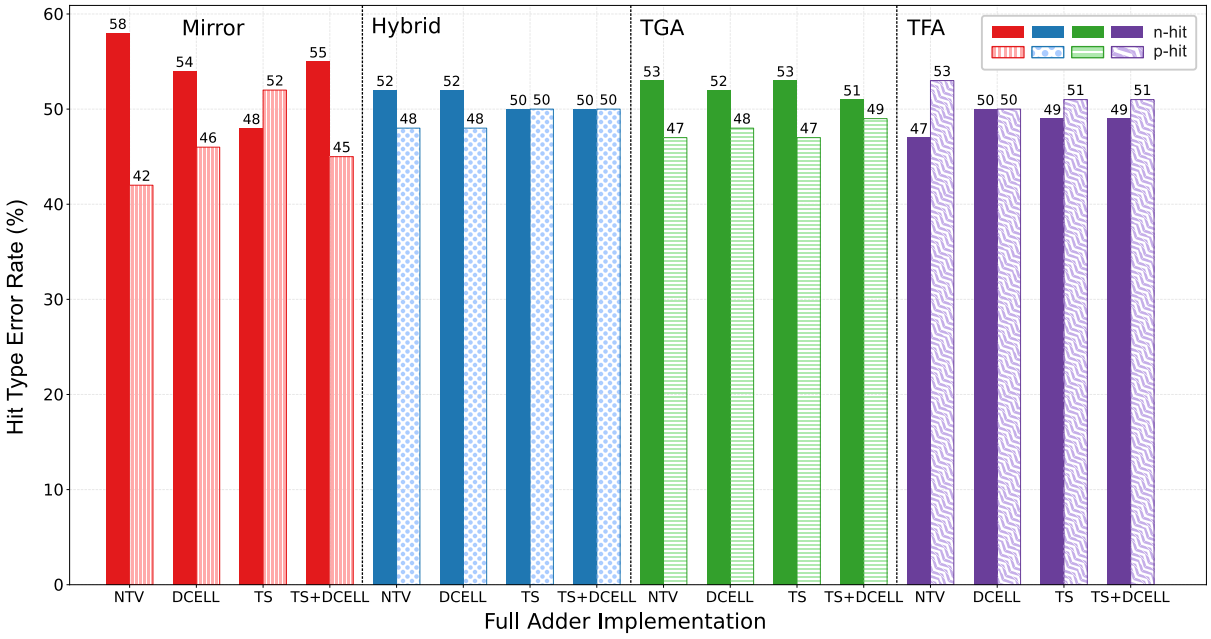
Source: The author.

In the Hybrid FA, employing DCELL results in p-hit accounting for nearly 52% of the total errors, while n-hit emerges as critical in the TS scenario, contributing to close to 65% of the total errors. This scenario exhibits the largest disparity between the two hits used in the experiments. Additionally, n-hit is responsible for generating all the lowest LETth values in the scenario with transistor sizing and DCELL. This indicates that transitions induced by negative charge collection are more prone to propagation in the evaluated topologies. Investigating the TGA topology, both hit types exhibit similar error rates, despite of the mitigation technique employed. However, when employing DCELL, n-hit shows a slight increase compared to p-hit. This trend persists when sizing the transistors, with only a 1% difference observed between the two hit types. Once again, n-hit emerges as critical for the TGA topology. Similarly to the TGA, in the TFA topology, the difference between the two hit types is minimal across all mitigation technique scenarios. When employing DCELL, n-hit leads to a mere 4% gap in the observed errors compared to pulse p-hit. This consistent trend underscores the significance of n-hit as a potential critical factor in the TFA topology.

Reducing the voltage operation alters the critical pulse dynamics across the evaluated scenarios. In the case of the Mirror FA, employing DCELL shifts n-hit to be the most susceptible pulse , responsible for 54% of errors, highlighted in 24. Conversely, with the TS technique, p-hit emerges as critical, accounting for 54% of errors. Combining DCELL and TS maintains n-hit as critical, with a 55% error rate. For the Hybrid FA, differences in error rates between hit types reduces compared to the nominal voltage implementation. DCELL technique in this topology predominantly propagates

errors from n-hit to the output. With TS and TS+DCELL implementations, both hit types contribute equally to errors, with n-hit being critical across all scenarios.

Figure 24 – Hit type Error Rate at NTV.



Source: The author.

In the TGA topology at NTV, DCELL maintains n-hit as critical, responsible for 52% of errors. Similarly, TS results for n-hit causes 53% of errors. Combining both techniques also highlights the high-to-low hit as critical for error propagation. Similar to the other topologies the n-hit can be defined as the critical one for the TGA topology. Finally, for TFA topology voltage reduction alters the critical hit behavior. With DCELL, both hit type exhibit similar error rates, each contributing 50% to total errors. However, with TS and the combined scenario, the p-hit becomes critical, accounting for 51% of errors. Notably, hit low-to-high emerges as critical, generating most errors on average across scenarios.

The results shows that the hit type dynamics are linked with the effectiveness of mitigation techniques and the impact of voltage reduction on error rates. Across various circuit topologies, different mitigation techniques, such as DCELL and TS, interact differently with hit types, influencing the critical energetic interference for error propagation.

In scenarios where DCELL is employed, n-hit consistently emerges as critical across multiple topologies. This hit type tends to propagate errors more effectively, regardless of the mitigation technique used. Conversely, the application of TS often results in a more balanced distribution of errors between the two hit types, with both high-to-low and low-to-high pulses contributing more evenly to the error count. Furthermore, the reduction in voltage operation can significantly influence the critical pulse behavior.

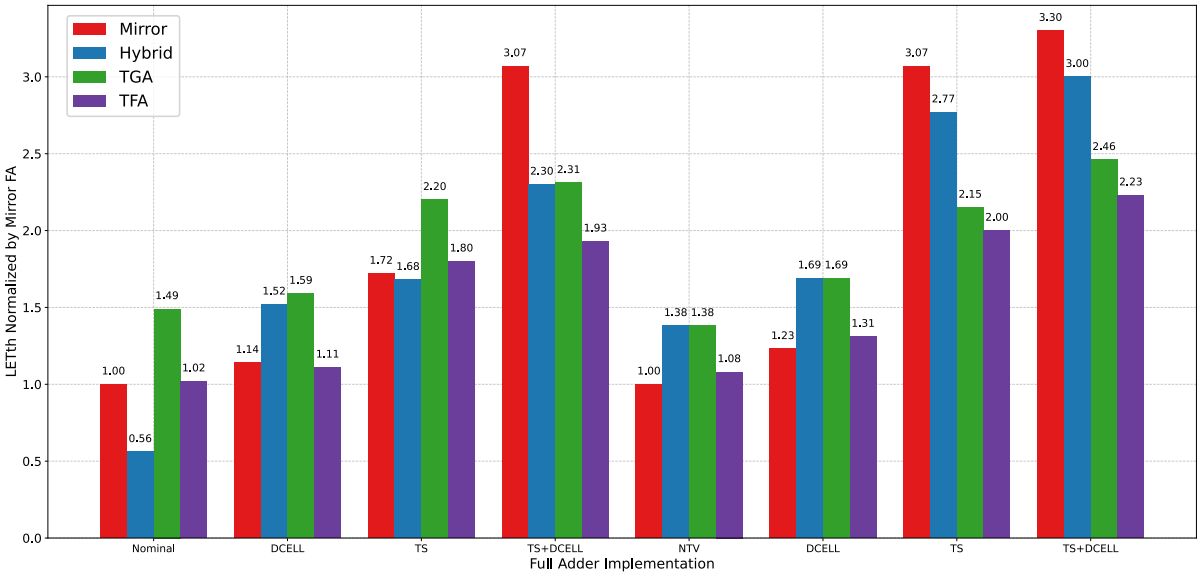
While nominal voltage settings may exhibit specific hit types as critical, voltage reduction can lead to shifts in critical hit dynamics. Some hit types may become more or less susceptible to error propagation under reduced voltage conditions, highlighting the complex interplay between voltage levels and pulse characteristics.

Overall, understanding the relationship between hit types, mitigation techniques, and voltage reduction is crucial for developing effective strategies to mitigate radiation-induced errors in integrated circuits. By identifying critical hit types and optimizing mitigation techniques accordingly, circuit designers can enhance the robustness and reliability of integrated circuits in radiation-prone environments.

6.1.4 Critical Nodes

In the investigation of critical LETth values to pinpoint the most sensitive regions at nominal voltage, we focused on the Mirror FA implementation as our reference. Analysis of the results revealed that employing the DCELL technique yielded a modest 1.14x increase in LETth. Node *j* retained its critical status, while node *g* exhibited a notable improvement in LETth, with values of 16 $MeVcm^2/mg$ and 22 $MeVcm^2/mg$, respectively. Conversely, with the TS technique, the LETth nearly doubled, with node *b* now presenting the lowest values. The most significant LETth improvements were observed with the combined application of both techniques, resulting in a 3x enhancement in cell resilience compared to our reference, particularly in the critical area of node *j*. Throughout the mitigation scenarios evaluated, node *j* consistently emerged as critical for the Mirror FA.

Figure 25 – LETth Normalized by Mirror FA at Nominal Implementation.



Source: The author.

At nominal voltage operation, the critical nodes for the Hybrid topology differ

depending on the mitigation technique employed. When using DCELL, nodes *e* and *j* emerge as critical, with a LETth of 21 $MeVcm^2/mg$, marking a 1.52x improvement compared to our reference, as depicted in Figure 25. Transistor sizing enhances circuit robustness, elevating the LETth to approximately 1.68x, with node *c* assuming critical status, boasting a LETth of 23 $MeVcm^2/mg$. The combined application of both techniques yields the most substantial improvement, enhancing the LETth by approximately 2.30x compared to our reference, as illustrated in Figure 25. Notably, critical nodes for the Hybrid full adder may vary depending on the mitigation technique utilized, yet all investigated techniques contribute to increasing the LETth.

At nominal voltage, the TGA topology demonstrates that the most sensitive nodes are the outputs *Sum* and *Cout*. These critical nodes remain unchanged when employing the DCELL technique, albeit with an increase in LETth of up to 1.59x, resulting in a LETth of 22 $MeVcm^2/mg$. Integration of the capacitive method as a mitigation strategy proves impactful, as it yields a LETth enhancement of 2.20x, raising the LETth to 31 $MeVcm^2/mg$ with the TS technique. The most significant LETth improvements are observed when combining both techniques, resulting in a 2.31x increase. Throughout all scenarios evaluated, the outputs consistently emerge as the most sensitive nodes, showcasing the lowest LETth values.

The TFA topology exhibits the smallest improvement in critical LETth when employing DCELL, with only a 1.11x increase, as depicted in Figure 25. Conversely, the TS technique demonstrates a more significant impact, boosting LETth by 1.83x, with a critical value of 26 $MeVcm^2/mg$ for node *Sum*. The most notable enhancement is achieved by combining both techniques, resulting in a 1.93x improvement in critical LETth. Despite the variations observed across scenarios, the *Sum* and *Cout* nodes consistently propagate the lowest LETth values.

Reducing the voltage operation had a significant impact on the critical LETth observed across all topologies. Similar to nominal operation, the Mirror FA at NTV serves as a comparison reference for the other topologies. In the Mirror FA at NTV operation, node *j* exhibits a minimum LETth of 1 $MeVcm^2/mg$ when employing DCELL. With sizing, the LETth increases by 3.07x, yet the lowest value is still presented by node *j*. Moreover, when applying TS+DCELL in the circuit, both node *g* and *j* exhibit the same LETth value, close to 3.30x the critical reference. Node *j* remains responsible for most of the LETth values across both voltage scenarios used.

However, for the Hybrid FA at NTV with DCELL, nearly all nodes in the circuit remain sensitive, exhibiting the same lowest LETth of 2 $MeVcm^2/mg$. Conversely, scenarios employing TS show a different behavior, with only nodes *a* and *g* being critical, and with an improvement of 2.77x in the critical value. Combining both techniques increases the LETth slightly further to 3.27 $MeVcm^2/mg$. Notably, at NTV, TS proves slightly more efficient in mitigating the number of errors for this topology.

At NTV, for the TGA topology, the implementation of DCELL resulted in a 1.68x improvement in LETth, reaching a critical value of 2 $MeVcm^2/mg$ for nodes *g*, *Sum*, and *Cout*. Sizing the transistors increased the LETth to 2.35 $MeVcm^2/mg$, marking a 2.15x enhancement, as illustrated in Figure 25. Combining these mitigation techniques further bolstered the robustness, with a slight increase of up to 2.46x in the observed LETth. Notably, the output nodes retained their critical status across all scenarios, presenting all critical LETth values.

The TFA topology at NTV exhibited a slight improvement in robustness when employing DCELL, with a 1.31x increase in LETth compared to the reference. Sizing the target devices resulted in a 2x improvement, with critical values of 2 $MeVcm^2/mg$ observed for the output nodes. The most significant enhancement for this topology was achieved by combining both techniques, yielding a 2.23x increase in LETth for the *Sum* node. These results underscore the critical nature of the output nodes in this circuit design.

In conclusion, the critical nodes in the analyzed topologies exhibit varying degrees of sensitivity under nominal and NTV voltage conditions. While the Mirror FA showcased consistent critical nodes across different scenarios, the Hybrid FA displayed fluctuations in critical node identification depending on the mitigation technique employed. On the other hand, the TGA topology maintained its critical output nodes across all scenarios, highlighting the importance of output node robustness. Finally, the TFA topology demonstrated that output nodes consistently remained critical, emphasizing their significance in determining overall circuit robustness. These findings emphasize the necessity of tailored mitigation techniques to address specific vulnerabilities in different circuit topologies under varying voltage conditions.

6.2 DISCUSSION ON THE VOLTAGE OPERATION

The adoption of mitigation techniques can reduce up to 60% the total error occurrence at nominal voltage, depending on the topology, and more than 35% at NTV in the circuits investigated. Moreover, the Hybrid topology presented, on average, 2% fewer errors than the Mirror at nominal voltage and 5% more errors than the Mirror for NTV. Among the PTL topologies at nominal voltage TFA presented 12% less errors than the TGA and up to 11% at NTV. The critical node can vary depending on the technique applied. However, in the two voltage operation, node *g* and *j* are the critical for the Mirror FA, nodes related to the *Cin* path are among the critical for the Hybrid FA. For the TGA the output nodes are the critical for both voltage domain and for TFA nodes related to the *Sum* output are the critical.

Comparing the circuits, it is possible to observe that Hybrid FA LETth is, on average, 2x more robust than the Mirror topology when using DCELL, for the two voltage operations, as shown in Figure 25. On the other hand, when using TS the

Mirror FA presented the best results in the LETth improvement, being on average 2x greater than the Hybrid implementations. The best improvement is obtained for the Mirror FA at NTV using both techniques combined with an improvement close to 3.3x in the critical LETth. Despite come improvement for the TGA and TFA in both voltage operation the LETth increase was no more tham 2.2x. Furthermore, combining both techniques presented the best improvement for all scenarios and topologies analyzed in this work, with a minimal improvement of more than 2x in the LETth.

The most susceptible vector varies depending on the technique. However, it is observed that most errors for Mirror, Hybrid and TGA are caused by the occurrence of particle collisions during a n-hit transition of the circuit, i.e. during the charge of the output capacitance. Except for the TFA, at NTV where the p-hit become to be critical one. Nonetheless, all critical LETth values observed for the topologies were generated, in general, by vectors that change the output also during a n-hit. The radiation n-hit is critical for all topologies, related to generating more errors, and, almost the critical LETth values generated in the experiments.

7 CONCLUSIONS

This work delves into the evaluation of radiation robustness in FinFET-based circuits by analyzing four common full adder topologies: Mirror FA, Hybrid FA, TGA, and TFA. Through two mitigation techniques, DCELL and Transistor Sizing, in tree different scenarios we investigate their impact on critical nodes and overall error rates under two voltage conditions. The results aim to enhance our understanding of optimizing integrated circuit designs for better reliability and robustness in radiation-prone environments.

When considering the impact of the mitigation techniques, the combination of DCELL and transistor sizing consistently yields the most substantial reduction in total errors across all topologies in the two voltage operation evaluated. This combined approach leads to a remarkable decrease in errors, showcasing its effectiveness in enhancing the robustness of the circuits. While individual techniques such as DCELL or sizing adjustments also contribute to error reduction, their impact is notably increased when utilized together. Therefore, for reducing the total error observed, the combination of DCELL and sizing adjustments emerges as the preferred technique in the context of enhancing the reliability of the analyzed topologies.

These improvements can be explained because increasing the transistor sizes can help in reducing the error susceptibility caused by ionizing radiation. By resizing transistors appropriately, the critical charge in sensitive nodes can be increased, thereby reducing the likelihood of SET occurrence. Furthermore, capacitive decoupling methods like DCELL help in stabilizing the voltage levels in critical nodes by providing additional capacitance. This helps in mitigating voltage fluctuations caused by radiation-induced charge deposition, thereby ensuring better signal integrity and reducing the likelihood of erroneous state transitions.

Across the topologies evaluated, different mitigation techniques, interact differently with pulse types, influencing the critical pulse for error propagation. Pass transistor logic-based topologies often exhibit higher sensitivity to current propagation allowing errors introduced in an internal node to easily spread to the output. Although the overall error count may be lower, these errors tend to manifest as critical LETth values, indicating their heightened impact on the system.

The results present that, with the exception of the TFA, the n-hit pulses are notably more prone to being propagated to the outputs across all topologies. The LETth can be improved by up to 3.30x, and on average, when used across the topologies. Combining mitigation techniques yields an average improvement of close to 2.74x for all topologies. Although less effective, DCELL alone can still enhance the critical LETth close to 1.48x, on average.

The critical nodes in the analyzed topologies exhibit varying degrees of sensitiv-

ity. While the Mirror FA showcased consistent critical nodes across different scenarios, the Hybrid FA displayed fluctuations in critical node identification depending on the mitigation technique employed. On the other hand, the TGA topology maintained its critical output nodes across all scenarios, highlighting the importance of output node robustness. Finally, the TFA topology demonstrated that output nodes consistently remained critical, emphasizing their significance in determining overall circuit robustness. These findings emphasize the necessity of tailored mitigation techniques to address specific vulnerabilities in different circuit topologies.

Overall, understanding the relationship between the types of hits and mitigation techniques is crucial for developing effective strategies to mitigate radiation-induced errors in integrated circuits. By identifying the critical hit type and optimizing mitigation techniques accordingly, circuit designers can enhance the robustness and reliability of integrated circuits in radiation-prone environments.

This work results in the following publication list. A preliminary evaluation have resulted in two international conferences papers published in the 2021 and 2022.

Building on the findings of this research, future work could focus on developing a comprehensive set of standard cell gates that are radiation-hardened. This set would include all necessary views: layout, schematic, abstract, and timing information. Additionally, designing an ASIC using these RHBD cells would further validate their effectiveness in real-world applications. This endeavor would not only enhance the robustness of integrated circuits against radiation-induced errors but also provide a standardized approach to implementing radiation-hardened designs in various semiconductor applications.

7.1 PUBLICATIONS

The final part of the discussions presented in this work were submitted and are under review for the Special Issue on Defect and Fault Tolerance in VLSI and Nanotechnology Systems in the IEEE Transactions on Device and Materials Reliability. Also, complementary parts of the results are submitted and under evaluation on the regular paper track and student forum track on a international conference.

- "Full Adder Circuit Optimization for SET Resilience: Decoupling Cells and Transistor Sizing Strategies", Student Forum of IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2024, under review.
- "Improving Soft Error Robustness of Full Adder Circuits with Decoupling Cell and Transistor Sizing," 2022 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI), Porto Alegre, Brazil, 2022, pp. 1-6, DOI: 10.1109/SBCCI55532.2022.9893240 (OLIVEIRA, R. N. M. et al., 2022).

- "SET Mitigation Techniques on Mirror Full Adder at 7 nm FinFET Technology" 2021 IEEE 22nd Latin American Test Symposium (LATS), Punta del Este, Uruguay, 2021, pp. 1-2, DOI: 10.1109/*LATS*53581.2021.9651889 (OLIVEIRA, R. N. M. et al., 2021).

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Appendix

APPENDIX A – SIMULATION RESULT TABLES

Table 17 – LETth for all nodes of Mirror FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Cout													
		a	b	c	d	e	f	g	h	i	j	k	l	Sum	Cout
	000	-	-	-	-	-	-	-	-	-	-	97	-	-	45
	001	-	-	-	-	-	-	-	96	-	-	67	97	-	45
	010	-	-	-	-	-	-	-	-	-	-	52	59	-	45
010	011	-	-	-	-	-	27	-	-	47	-	-	-	-	-
	100	-	-	-	-	-	-	-	-	-	-	98	-	-	45
	101	27	-	-	-	-	27	-	-	48	-	-	-	-	-
	110	51	27	-	-	-	27	-	48	-	-	-	-	-	-
	111	-	-	-	-	-	60	-	-	-	-	-	-	-	-
	000	-	-	-	-	-	46	-	89	-	-	-	-	-	-
	001	-	41	-	-	-	20	-	20	-	-	-	-	-	-
	010	-	41	-	-	-	20	-	96	-	-	-	-	-	-
101	011	83	-	-	84	53	-	-	-	-	-	-	-	-	37
	100	41	-	-	-	-	21	-	40	20	-	-	-	-	-
	101	-	-	-	-	83	-	-	-	-	-	-	-	-	37
	110	-	-	-	55	43	-	-	-	-	-	-	-	-	37
	111	-	-	-	-	80	-	-	-	-	-	-	-	-	37
		Sum													
	000	55	-	55	47	34	-	28	27						
	000	-	-	-	-	-	-	-	95	-	-	-	-	45	-
	001	-	-	-	-	26	-	20	-	-	85	53	-	-	-
	010	26	43	-	-	48	-	27	-	-	-	27	48	-	-
010	011	50	27	-	-	-	27	-	47	-	-	-	-	45	-
	100	-	-	-	-	26	-	-	-	-	-	26	-	-	-
	101	-	-	-	-	-	27	-	80	47	-	-	-	45	-
	110	26	-	66	-	-	26	-	-	47	-	-	-	45	-
	111	42	-	47	39	-	-	-	-	-	-	-	40	-	-
	000	-	-	-	42	21	-	14	-	-	14	20	40	-	-
	001	833	-	-	-	26	-	27	-	-	47	52	59	37	-
	010	-	-	-	26	26	-	27	-	-	47	97	-	37	-
101	011	82	-	39	85	53	-	20	-	-	-	71	98	-	-
	100	-	-	-	-	78	-	27	96	-	47	66	97	37	-
	101	-	-	40	-	81	-	20	-	-	-	20	20	-	-
	110	-	-	39	55	43	-	20	-	-	-	20	95	-	-
	111	-	-	19	58	26	-	19	-	-	-	27	48	37	-
Total Errors Node		10	5	6	8	15	11	10	10	5	5	15	11	8	8
Lower Value		26	27	19	26	21	20	14	20	20	14	20	20	37	37
Total Errors Rate (%)		8	4	5	6	12	9	8	8	4	4	12	9	6	6

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 18 – Total error for input vectors of Mirror FA at Nominal voltage ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	12	9
001	16	13
010	17	13
011	**20**	**16**
100	18	14
101	13	10
110	17	13
111	14	11

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Table 19 – LETth for all nodes of Hybrid FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Cout												
		a	b	c	d	e	f	g	h	i	j	Cin	Sum	Cout
010	000	-	-	-	-	-	-	-	-	-	-	-	-	45
	001	78	-	-	-	-	-	-	-	-	-	-	-	45
	010	-	-	-	-	-	-	62	-	-	64	-	-	45
	011	-	-	26	26	27	-	-	47	-	-	-	-	-
	100	-	-	-	-	-	-	-	-	-	65	-	-	45
	101	-	-	26	-	27	-	-	47	69	-	-	-	-
	110	-	-	-	49	26	-	-	-	46	-	-	-	-
	111	-	-	49	49	26	-	-	-	46	-	-	-	-
101	000	-	-	-	39	20	-	-	38	38	-	-	-	-
	001	-	-	8	39	20	-	-	94	38	-	-	-	-
	010	-	-	40	59	20	-	-	20	96	-	-	-	-
	011	-	-	12	14	-	-	-	-	-	39	-	-	36
	100	-	12	40	-	20	-	-	20	20	-	-	-	-
	-	-	13	43	-	-	-	-	-	-	39	-	-	36
	110	-	18	-	19	-	85	-	-	-	-	-	-	36
	111	-	9	18	8	-	-	-	-	-	-	-	-	36
		Sum												
010	000	51	-	-	-	-	-	-	-	-	-	-	45	-
	001	52	-	-	-	-	-	-	-	-	26	-	-	-
	010	-	-	-	-	-	29	-	59	-	28	-	-	-
	011	-	97	-	-	-	25	66	-	-	-	-	45	-
	100	-	29	-	-	-	30	-	59	54	28	-	-	-
	101	-	25	-	-	-	25	-	-	69	-	-	45	-
	110	65	-	-	-	-	-	-	-	-	-	-	45	-
	111	73	-	-	-	-	-	-	-	-	31	-	-	-
101	000	-	-	-	-	-	59	-	-	-	24	-	-	-
	001	-	-	8	-	-	51	-	-	-	-	-	36	-
	010	20	-	-	59	-	-	19	-	-	-	-	36	-
	011	28	-	12	14	-	-	28	-	-	23	-	-	-
	100	19	12	-	-	-	-	91	-	-	-	-	36	-
	101	28	13	43	-	-	-	-	-	-	23	-	-	-
	110	-	8	-	8	-	49	-	-	-	20	-	-	-
	111	-	9	18	8	-	58	-	-	-	-	-	36	-
Total Errors Node		9	11	12	12	8	9	5	8	9	12	0	8	8
Lower Value		19	8	8	8	20	25	19	20	20	20	101	36	36
Total Errors Rate (%)		8	10	11	11	7	8	5	7	8	11	0	7	7

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 20 – Total error for input vectors of Hybrid FA at Nominal voltage ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	9	8
001	12	11
010	14	13
011	**17**	**15**
100	16	14
101	16	14
110	12	11
111	15	14

Table 21 – LETth for all nodes of TGA FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Cout									
		B	b	A	d	Cin	f	g	h	Sum	Cout
010	000	-	-	-	-	-	-	-	-	-	27
	001	45	-	48	-	-	-	28	-	-	27
	010	-	-	51	-	47	-	-	-	100	28
	011	-	48	45	-	-	-	-	47	-	-
	100	46	-	-	-	47	-	-	45	100	28
	101	-	-	-	-	-	-	-	-	-	-
	110	-	54	-	46	-	-	28	-	-	-
	111	-	-	-	-	-	-	-	-	-	-
101	000	-	-	-	-	-	-	-	-	-	-
	001	-	39	-	-	-	-	-	40	-	-
	010	-	82	-	-	-	-	-	-	-	-
	011	36	80	-	37	37	-	28	89	90	**21**
	100	-	56	-	99	-	-	23	-	-	-
	101	-	-	44	-	37	-	40	90	90	**21**
	110	38	-	38	-	-	-	88	51	-	**21**
	111	-	-	38	-	-	-	88	-	-	**21**
		Sum									
010	000	45	-	48	-	47	-	28	-	28	-
	001	45	-	49	-	-	-	28	-	-	98
	010	-	47	46	-	49	-	-	46	-	49
	011	-	49	45	-	-	47	-	54	28	-
	100	46	-	-	-	49	-	-	45	-	49
	101	46	-	-	-	-	47	-	55	28	-
	110	-	54	-	46	47	-	27	-	28	-
	111	-	54	-	47	-	-	28	-	-	-
101	000	-	39	-	-	-	-	-	39	-	-
	001	-	39	-	-	38	95	-	46	**21**	-
	010	36	82	-	38	-	37	28	89	**21**	-
	011	36	80	-	37	41	-	28	-	-	40
	100	-	52	38	96	-	37	28	91	**21**	92
	101	-	56	42	-	41	-	28	-	-	40
	110	38	-	41	-	-	-	-	39	-	56
	111	38	-	41	-	38	95	-	52	**21**	54
Total Errors Node		12	16	14	8	12	6	15	16	12	16
Lower Value		36	39	38	37	37	37	22	39	21	21
Total Errors Rate (%)		9	13	11	6	9	5	12	13	9	13

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 22 – Total error for input vectors of TGA FA at Nominal voltage ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	8	6
001	15	12
010	17	13
011	**22**	**17**
100	20	16
101	15	12
110	17	13
111	13	10

Table 23 – LETth for all nodes of TFA FA considering worst fault propagation at Nominal voltage ($MeVcm^2/mg$).

Pulse	Input	Cout							
		B	b	A	Cin	e	f	Sum	Cout
010	000	-	-	-	-	-	-	-	27
	001	51	-	47	-	29	-	-	27
	010	-	-	52	47	-	-	-	28
	011	-	43	45	-	-	50	-	-
	100	47	-	-	47	-	42	-	28
	101	-	-	-	-	-	-	99	-
	110	-	53	-	-	29	-	62	-
	111	-	-	-	-	-	-	-	-
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	-	-	46	-	-
	010	-	-	-	-	-	-	-	-
	011	37	92	-	38	19	-	-	21
	100	-	68	-	-	24	-	-	-
	-	-	-	44	38	40	-	-	21
	110	37	-	38	-	-	52	-	21
	111	-	-	38	-	-	-	-	21
		Sum							
010	000	56	-	55	47	34	-	28	-
	001	51	-	49	-	29	-	-	87
	010	-	44	48	50	-	43	-	49
	011	-	43	45	-	83	47	27	100
	100	47	-	-	50	-	42	-	49
	101	46	-	-	-	84	47	27	-
	110	-	53	-	47	31	-	28	-
	111	-	48	-	-	27	-	-	-
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	37	-	58	21	-
	010	39	97	-	-	21	85	**14**	-
	011	37	92	-	43	19	-	-	42
	100	-	67	40	96	23	85	**14**	93
	101	-	65	40	43	23	-	-	42
	110	40	-	44	-	-	-	-	95
	111	37	-	41	37	-	67	21	74
Total Errors Node		12	12	14	13	15	12	10	17
Lower Value		37	43	38	37	19	42	14	21
Total Errors Rate (%)		11	11	13	12	14	11	10	16

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 24 – Total error for input vectors of TFA FA at Nominal voltage ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	6	6
001	12	11
010	13	12
011	**19**	**18**
100	17	16
101	14	13
110	14	13
111	10	10

Table 25 – LETth for all nodes of Mirror FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	Cout													
		a	b	c	d	e	f	g	h	i	j	k	l	Sum	Cout
010	000	-	-	-	-	-	-	-	-	21	-	9	14	-	4
	001	-	-	-	-	-	-	-	11	-	-	8	11	-	4
	010	-	-	-	-	-	-	-	28	-	-	7	8	-	4
	011	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	100	-	-	-	-	-	-	-	-	29	-	10	21	-	4
	101	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	110	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	111	-	-	-	-	-	-	-	-	-	-	-	-	-	-
101	000	85	-	48	-	-	3	-	7	10	-	-	-	-	-
	001	20	-	35	-	-	2	-	4	2	-	-	-	-	-
	010	48	-	36	-	-	2	-	2	25	-	-	-	-	-
	011	-	-	-	19	-	-	-	-	-	-	-	-	-	3
	100	66	-	36	41	-	2	-	44	46	-	-	-	-	-
	101	40	-	-	10	-	-	-	-	-	-	-	-	-	33
	110	11	59	-	10	-	-	-	-	-	-	-	-	-	3
	111	42	31	80	14	-	-	-	-	-	-	-	-	-	3
		Sum													
010	000	-	-	-	-	-	-	-	11	15	69	-	11	4	-
	001	-	-	78	40	-	-	2	-	-	19	8	12	-	-
	010	-	-	78	38	-	-	2	-	-	19	7	9	-	-
	011	39	41	-	-	-	2	-	11	24	44	-	-	4	-
	100	-	-	79	2	-	-	2	-	-	19	11	21	-	-
	101	2	41	-	-	-	2	-	22	24	44	-	-	4	-
	110	5	2	-	-	-	2	-	27	38	45	-	-	4	-
	111	-	-	2	5	-	-	2	-	-	-	9	-	-	-
101	000	-	-	-	-	-	-	1	-	-	1	2	4	-	-
	001	18	35	-	-	-	2	-	4	2	-	-	-	3	93
	010	20	21	-	-	-	2	-	2	46	-	-	-	3	93
	011	-	-	16	19	-	-	2	-	-	87	2	2	-	-
	100	10	21	-	41	-	2	-	44	46	-	-	-	3	92
	101	40	-	16	10	-	-	2	-	-	86	2	42	-	-
	110	21	60	15	11	-	-	2	-	-	86	25	44	-	-
	111	10	14	80	10	-	-	-	-	-	-	-	-	3	-
Total Errors Node		16	10	13	14	0	10	8	13	13	11	12	12	8	11
Lower Value		2	2	2	2	-	2	1	2	2	1	2	2	3	3
Total Errors Rate (%)		11	7	9	9	0	7	5	9	9	7	8	8	5	7

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 26 – Total error for input vectors of Mirror FA at NTV ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	18	12
001	22	15
010	22	15
011	15	10
100	**24**	**16**
101	17	11
110	19	13
111	14	9

Table 27 – LETth for all nodes of Hybrid FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	Cout												
		a	b	c	d	e	f	g	h	i	j	Cin	Sum	Cout
010	000	59	-	-	-	-	-	14	-	-	54	-	-	4
	001	**7**	-	-	-	-	-	14	-	-	-	-	-	4
	010	62	-	-	-	-	-	8	-	-	**5**	-	-	4
	011	-	-	**2**	**2**	**2**	-	-	20	32	-	-	-	-
	100	61	-	-	-	-	-	20	-	-	**5**	-	-	4
	101	-	-	**2**	39	**2**	-	-	20	10	-	-	-	-
	110	-	-	37	4	**2**	-	-	-	19	-	-	-	-
	111	-	-	4	4	**2**	-	-	97	19	-	-	-	-
101	000	-	-	74	13	**2**	-	-	3	3	-	-	-	-
	001	-	-	92	13	**2**	-	-	42	3	-	-	-	-
	010	-	-	15	9	2	-	-	**2**	43	-	-	-	-
	011	-	18	-	45	-	62	-	-	-	3	-	-	3
	100	-	44	15	26	**2**	-	-	**2**	**2**	-	-	-	-
	101	-	9	-	-	-	63	-	-	-	3	-	-	3
	110	-	14	-	56	-	6	-	-	-	-	-	-	3
	111	-	14	-	46	-	54	-	-	-	55	-	-	3
		Sum												
010	000	**5**	-	-	-	-	-	70	-	-	-	-	4	-
	001	10	-	-	-	-	60	-	43	-	**2**	-	-	-
	010	-	36	-	-	-	3	68	8	21	**2**	-	-	-
	011	-	35	-	-	-	**2**	68	-	22	-	-	4	-
	100	-	3	-	-	-	3	-	8	8	**2**	-	-	-
	101	-	**2**	-	-	-	**2**	44	-	10	-	-	4	-
	110	**7**	-	-	-	-	-	97	-	-	-	-	4	-
	111	17	94	-	-	-	42	-	63	-	3	-	-	-
101	000	45	-	66	-	-	12	94	-	-	**2**	-	-	-
	001	-	83	-	-	-	5	-	-	-	-	-	3	-
	010	**2**	61	-	10	-	-	**2**	-	-	-	-	3	-
	011	**2**	-	9	8	-	-	**2**	-	-	**2**	-	-	-
	100	**2**	44	-	19	-	-	41	-	-	-	-	3	-
	101	**2**	47	9	18	-	-	41	-	-	**2**	-	-	-
	110	68	-	30	56	-	6	-	-	-	**2**	-	-	-
	111	-	58	-	46	-	4	-	-	-	-	-	3	-
Total Errors Node		14	15	12	17	8	14	14	11	12	14	0	8	8
Lower Value		2	2	2	2	2	2	2	2	2	2	-	3	3
Total Errors Rate (%)		10	10	8	12	5	10	10	7	8	10	0	5	5

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 28 – Total error for input vectors of Hybrid FA at NTV ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	17	12
001	15	10
010	**20**	**14**
011	**20**	**14**
100	**20**	**14**
101	**20**	**14**
110	16	11
111	19	13

Table 29 – LETth for all nodes of TGA FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	Cout									
		B	b	A	d	Cin	f	g	h	Sum	Cout
010	000	-	-	67	-	13	66	-	-	16	**2**
	001	4	95	5	37	39	-	3	-	63	**2**
	010	-	-	5	-	5	38	-	73	21	**2**
	011	-	4	4	-	59	-	-	4	-	28
	100	5	-	-	-	5	38	-	4	21	**2**
	101	-	-	-	-	-	-	-	-	-	-
	110	-	6	-	5	-	-	3	98	-	-
	111	-	-	-	-	-	-	-	98	-	-
101	000	-	-	-	-	-	-	-	-		
	001	-	3	-	-	-	-	-	3	-	-
	010	-	-	-	-	-	-	-	89	-	-
	011	3	86	47	3	3	39	**2**	90	22	**2**
	100	-	17	-	-	-	-	-	90	-	-
	101	-	97	4	42	3	39	4	90	22	**2**
	110	3	86	3	37	45	-	21	4	67	**2**
	111	99	86	3	37	10	57	21	93	12	**2**
		Sum									
010	000	4	95	5	37	5	34	3	-	**2**	9
	001	4	95	5	37	85	-	3	-	-	12
	010	-	4	4	-	5	-	-	4	-	5
	011	-	4	4	-	57	4	-	5	**2**	28
	100	4	95	-	-	5	-	-	4	-	5
	101	5	-	-	-	64	**2**	-	5	**2**	-
	110	-	5	46	5	5	34	3	99	**2**	28
	111	-	6	50	5	-	-	3	98	-	-
101	000	-	3	-	-	-	-	-	3	-	-
	001	-	3	-	-	3	39	-	**2**	**2**	64
	010	3	86	52	3	47	3	**2**	89	**2**	72
	011	3	86	50	3	4	-	**2**	90	-	**2**
	100	-	8	**2**	40	48	3	**2**	90	**2**	27
	101	-	10	**2**	41	4	-	**2**	90	-	**2**
	110	3	-	**2**	-	59	-	-	3	-	4
	111	3	-	**2**	-	3	39	-	4	**2**	8
Total Errors Node		13	22	20	14	23	14	14	26	16	22
Lower Value		3	3	3	3	3	3	2	3	2	2
Total Errors Rate (%)		7	12	11	8	13	8	8	14	9	12

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 30 – Total error for input vectors of TGA FA at NTV ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	16	9
001	23	13
010	22	12
011	**30**	**16**
100	22	12
101	21	11
110	27	15
111	23	13

Table 31 – LETth for all nodes of TFA FA considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	Cout							
		B	b	A	Cin	e	f	Sum	Cout
010	000	95	-	73	48	60	-	48	**2**
	001	5	95	5	73	3	-	50	**2**
	010	-	-	5	5	75	61	62	**2**
	011	-	4	4	60	-	5	-	28
	100	5	-	-	5	78	4	63	**2**
	101	-	95	-	-	-	-	-	-
	110	45	5	55	-	3	98	73	-
	111	-	-	-	-	-	97	-	-
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	-	-	4	-	-
	010	-	93	-	-	-	99	-	-
	011	3	39	48	3	**2**	78	63	**2**
	100	-	-	5	-	-	99	-	-
	101	-	38	4	3	4	73	61	**2**
	110	3	80	3	53	56	4	56	**2**
	111	98	80	3	14	56	59	14	**2**
		Sum							
010	000	6	95	6	4	3	-	2	11
	001	5	95	5	-	3	-	-	12
	010	-	4	4	5	-	4	-	5
	011	44	4	4	59	23	5	2	28
	100	5	94	-	5	-	4	-	5
	101	4	-	49	76	23	5	2	-
	110	46	6	48	4	3	98	2	27
	111	44	5	50	-	2	97	-	94
101	000	-	-	-	-	-	-	-	-
	001	-	-	-	3	82	4	2	65
	010	3	42	55	47	2	36	**1**	79
	011	3	40	54	4	2	-	-	4
	100	-	5	4	43	2	36	**1**	28
	101	-	5	4	4	2	-	-	4
	110	3	90	5	-	-	-	-	-
	111	3	90	4	3	80	5	2	6
Total Errors Node		18	23	22	21	22	22	17	22
Lower Value		3	4	3	3	2	4	1	2
Total Errors Rate (%)		11	14	13	13	13	13	10	13

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100 MeVcm^2/mg$.

Table 32 – Total error for input vectors of TFA FA at NTV ($MeVcm^2/mg$).

Input	Total Errors Vector	Vector Errors Rate (%)
000	13	8
001	18	11
010	21	13
011	**27**	**16**
100	21	13
101	19	11
110	25	15
111	23	14

APPENDIX B – PUBLICATION

This is the IEEE format paper submitted for the 2024 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), regular paper track - currently under evaluation.

Circuit-Level SET Mitigation at Near-threshold Operation for FinFET-Based Full Adder Designs

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***Abstract*—This work investigates the radiation sensitivity on FinFET-based full adders under near-threshold voltage opration using FinFET technology models. Furthermore, we examine the impact of three circuit-level mitigation techniques against SETs for the full adders: decoupling cells (DCELLs), transistor sizing (TS), and a combined approach using both. The results underscore critical vectors, hit type and the sensitivity of internal nodes for all topologies and highlight, which vary depending on the full adder implementation. Our findings demonstrate that utilizing TS reduces in 35% the susceptibility to soft errors for the Mirror FA at low voltage operation. Moreover, when both techniques are employed together, they collectively decrease total error occurrences on average more than 40% across the circuits investigated. Also the results show that pass transistor designs are prone to propagating errors due to signal degradation. Through this analysis, coupled with critical node evaluation, we aim to elucidate the advantages and limitations of these mitigation techniques in bolstering the robustness of FinFET-based full adders operating at low voltage in radiation-prone environments.**

***Index Terms*—Full adders, FinFET devices, single-event transient effects, circuit-level mitigation techniques.**

I. Introduction

Non-destructive Single-Event Effects (SEEs), such as Single Event Transient (SET), become a significant challenge in advanced CMOS technologies, especially because of the reduction in the operating voltage achieved by technology scaling [1]. Many low power applications also exploit the voltage reduction as a way to reduce the power consumption. Reducing the voltage operation, while advantageous for low-power applications, may impose side effects such as lowering frequency operation, increasing leakage power, and increasing the sensitivity to soft errors. In near-threshold (NTV) operation, the supply voltage is set very close to or just slightly above the threshold voltage of the transistors, often referred to as "subthreshold" operation.

Several techniques can be applied at different abstraction levels to mitigate SET effects on digital circuits. At the circuit design level, prior research has investigated the efficacy of Schmitt triggers, decoupling cells, sleep transistors, transistor sizing (TS), and transistor reordering as potential solutions [2].

The Full Adder (FA) is one of the primary combinational cells of the Arithmetic and Logic Unit (ALU) and one of the most crucial component on computer systems [3]. Moreover, FA is generally part of the critical path in most systems making this digital component strongly affects the overall performance of the whole system. We observe that there is a lack of work evaluating the SET effects on FAs circuits in multigate technologies.

This work evaluates the sensitivity of full adder circuits to SET faults by comparing Mirror, Hybrid, TFA, and TGA topologies previously investigated for process variability effects in [4]. Building upon earlier evaluations [5], [6], a comparative electrical simulations identify critical points in these topologies. Then, to mitigate the radiation impact, three distinct approaches are employed at circuit level: DCELL [7], TS, and a combined strategy with both DCELL and TS.

II. Methodology

When an energetic particle strikes a transistor junction, it triggers the charge collection mechanism, accumulating charge as it travels through the depletion region [8]. The Linear Energy Transfer (LET) quantifies this collected charge, making it a key metric for evaluating robustness. In our work, we define the SET pulse as the voltage glitch occurring at the output of a logic gate, influenced by the deposited charge in any internal device. Depending on the location of the ion impact , there are two types of single-event hits: n-hit and p-hit. An n-hit causes a high-to-low transition at the sensitive node, while a p-hit results in a low-to-high transition [9].

The radiation effect of a particle striking at the junction of a device can be represented by a double exponential transient pulse. This work utilized the equation model outlined in [1]. The collection time constant was set to 200 ps, and the initially constant time was set to 10 ps [1]. The charge collection depth for the FinFET devices was specified as 21 nm [10].

The experiments involve determining the minimum current required to induce an output flip in the circuit, followed by calculating the minimum LET threshold (LETth) based on the equation in [11]. The experiment concludes when the simulation requires a LETth value exceeding 100 $MeVcm^2/mg$ (the node is considered robust in this case).

The fault simulation is carried out at the circuit level using HSPICE. The circuits were simulated using the 7 nm ASAP7 model by [12]. The near-threshold voltage for the devices was set to 0.35 V. The radiation pulse is introduced as an independent current source at the target junction of the device, represented by the circuit node in the simulation and evaluation. The current value is increased at 0.5 μA step to determine the minimum current to provoke the unexpected

behavior on one of the FA outputs. All transistors on all circuits were set to the minimum size of 1-fin to represent a critical scenario for robustness tests. Two inverters were inserted in the input signals to emulate a realistic input slope, and the load capacitance was adjusted to correspond to a fanout of 4.

III. Results

The evaluation of the radiation sensitivity begins with testing the circuits while operating at their NTV without any mitigation technique. The results of absolute LETth are available for each result table in this section. To identify critical nodes that are more susceptible to radiation-induced errors, we highlight them in red within the tables. The nodes that remains robust are denoted by a "-" in the results tables. This analysis provides a comprehensive perspective on the vulnerabilities and sensitivities parts of the topologies investigated to SETs. The results provide insights into specific sections of the circuits that are more susceptible to mitigation strategies, contributing to the advancement of more robust and resilient integrated circuits.

A. Error Rate

The total error occurrences for the Mirror FA presents a moderate amount of sensitive internal nodes. Examining the LETth results for both outputs reveals that node *c* exhibits a heightened susceptibility to SETs, as Table I shows. Node *c* is accountable for approximately 11% of all computed errors. Additionally, nodes *h*, *j*, and *Sum* emerge as prominent contributors to generating interference on the outputs.

Analyzing the Hybrid FA results from Table I, it becomes evident that nodes *a*, *b*, *d*, *f*, and *g* exhibit considerable susceptibility to error generation, each contributing at a rate close to 10%. Collectively, these nodes account for nearly 50% of the total error occurrences. In contrast, node *d* demonstrated the highest error rates, establishing it as the most susceptible nodes to error generation, representing approximately 12% of the total error occurrences observed.

Reducing the voltage operation led to a higher occurrence for the TGA FA when compared with the other topologies, as Table II shows. Node *b* emerged as the most susceptible to generating errors, exhibiting a slight 1% increase compared to nodes *h* and *Sum*. Despite this minor difference in NTV operation, nodes *h* and *Sum* can be considered the most susceptible to generating errors. Additionally, nodes *Cout* and *e* should be included in the critical set for this topology due to their increased sensitivity under reduced voltage conditions.

The TFA exhibited a significant deterioration in error rates, as outlined in Table II. This substantial rise in the total error renders the TFA topology the most sensitive among our FAs set. Notably, node *e* emerged as the most susceptible to propagate SET, contributing 14% to the total errors. Additionally, nodes *b* and the output *Cout* played critical roles, each contributing 13% to the overall errors. This heightened vulnerability of specific nodes emphasizes the importance of targeted mitigation strategies for enhancing the robustness of the TFA under reduced voltage operations.

B. Input Vectors

In the examination of input vector combinations for the Mirror FA, it becomes evident that vectors 100 holds the highest susceptibility to error generation, as Table I shows. Additionally, vectors 001 and 010 contribute significantly to error propagation, collectively representing over 46% of the total SET occurrences. Conversely, the vector 000 attains the lowest LETth results, designating it as the critical input combination for the Mirror topology.

Turning attention to the Hybrid FA, input vectors 010, 011, 100, and 101 share a common error rate occurrence of 14%, signifying their heightened susceptibility to generating errors in this topology outputs. These vectors also correspond to the generation of the lowest LETth values, establishing them as the most sensitive ones for this topology. On the other hand the input vector 000 stands out with the lowest error rate, constituting a mere 8% of the total error occurrences.

For the TGA topology, the analysis in Table II reveals that 16% of the errors occur during the 011 input combi-

TABLE I: LETth for all nodes of Mirror and Hybrid FAs considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	Mirror														Hybrid												
		a	b	c	d	e	f	g	h	i	j	k	l	S	C	a	b	c	d	e	f	g	h	i	j	Cin	S	C
010	000	-	-	-	-	-	-	-	11	21	69	9	14	-	4	59	-	-	-	-	-	70	-	-	54	-	4	4
	001	-	-	78	40	-	-	2	11	-	19	8	12	-	4	10	-	-	-	-	60	14	43	-	**2**	-	-	4
	010	-	-	78	38	-	-	2	28	-	19	7	9	-	4	62	36	-	-	-	3	68	8	21	5	-	-	4
	011	39	41	-	-	-	2	-	11	24	44	-	-	4	-	-	35	**2**	**2**	**2**	**2**	68	20	32	-	-	4	-
	100	-	-	79	2	-	-	2	-	29	19	11	21	-	4	61	3	-	-	-	3	20	8	8	5	-	-	4
	101	2	41	-	-	-	2	-	22	24	44	-	-	4	-	-	**2**	**2**	39	**2**	**2**	44	20	10	-	-	4	-
	110	5	2	-	-	-	2	-	27	38	45	-	-	4	-	7	-	37	4	**2**	-	97	-	19	-	-	4	-
	111	-	-	2	5	-	-	2	-	-	-	9	-	-	-	17	94	4	4	**2**	42	-	97	19	3	-	-	-
101	000	85	-	48	-	-	3	**1**	7	10	**1**	2	4	-	-	45	-	74	13	**2**	12	94	3	3	**2**	-	-	-
	001	20	35	35	-	-	2	-	4	2	-	-	-	3	93	-	83	92	13	**2**	5	-	42	3	-	-	3	-
	010	48	21	36	-	-	2	-	2	46	-	-	-	3	93	**2**	61	15	10	**2**	-	**2**	**2**	43	-	-	3	-
	011	-	-	16	19	-	-	2	-	-	87	2	2	-	3	**2**	18	9	45	-	62	**2**	-	-	3	-	-	3
	100	66	21	36	41	-	2	-	44	46	-	-	-	3	92	**2**	44	15	26	**2**	-	41	**2**	**2**	-	-	3	-
	101	40	-	16	10	-	-	2	-	-	86	2	42	-	3	**2**	47	9	18	-	63	41	-	-	3	-	-	3
	110	21	60	15	11	-	-	2	-	-	86	25	44	-	3	68	14	30	56	-	6	-	-	-	**2**	-	-	3
	111	42	31	80	14	-	-	-	-	-	-	-	-	3	3	-	58	-	46	-	54	-	-	-	55	-	3	3

*Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100MeVcm^2/mg$.

TABLE II: LETth for all nodes of TGA and TFA full adders considering worst fault propagation at NTV ($MeVcm^2/mg$).

Pulse	Input	TGA										TFA							
		B	b	A	d	Cin	f	g	h	S	C	B	b	A	Cin	e	f	S	C
010	000	4	95	5	37	5	34	3	-	**2**	**2**	6	95	6	4	3	-	2	2
	001	4	95	5	37	39	-	3	-	63	**2**	5	95	5	73	3	-	50	2
	010	-	4	4	-	5	38	-	4	21	**2**	-	4	4	5	75	4	62	2
	011	-	4	4	-	57	4	-	4	**2**	28	44	4	4	59	23	5	2	28
	100	4	95	-	-	5	38	-	4	21	**2**	5	94	-	5	78	4	63	2
	101	5	-	-	-	64	4	-	5	**2**	-	4	95	49	76	23	5	2	-
	110	-	5	46	5	5	34	3	98	**2**	28	45	5	48	4	3	98	2	27
	111	-	6	50	5	-	-	3	98	-	-	44	5	50	-	2	97	-	94
101	000	-	3	-	-	-	-	-	3	-	-	-	-	-	-	-	-	-	-
	001	-	3	-	-	3	39	-	3	**2**	64	-	-	-	3	82	4	2	65
	010	3	86	52	3	47	3	**2**	89	**2**	72	3	42	55	47	2	36	**1**	79
	011	3	86	47	3	3	39	**2**	90	22	**2**	3	39	48	3	2	78	63	2
	100	-	10	4	41	3	39	**2**	90	22	4	-	5	4	43	2	36	**1**	28
	101	**2**	47	9	18	-	63	41	-	-	3	-	5	4	3	2	73	61	2
	110	3	86	3	37	45	-	21	3	67	**2**	3	80	3	53	56	4	56	2
	111	3	86	3	37	3	39	21	4	**2**	**2**	3	80	3	3	56	5	2	2

**Robust results are indicated by (-) on the table, representing the cases where the LETth values are over $100MeVcm^2/mg$.

nation, making this vector the most sensitive. However, it is noteworthy that several other vectors, including 001, 010, 011, 100, 101, and 111, exhibit the lowest LETth value of 2 $MeVcm^2/mg$. This suggests that nearly all input vectors are susceptible to propagating errors, depending on the specific node impacted by the radiation particle. Similar to the Hybrid and Mirror topologies, vector 000 demonstrates the lowest error rate.

The TFA topology experiences a significant impact when operating at NTV with a few robust nodes, as illustrated in Table II. Input vectors 010 and 100 exhibit a critical LETth of only 1 $MeVcm^2/mg$. Despite these two critical input combinations, vector 011 generates up to 21% of the total errors observed, establishing itself as the most sensitive input vector for the topology.

C. Type of SEE hit

In the evaluation of SET pulse types, the Mirror Full Adder maintains the n-hit as the critical pulse, constituting up to 58% of the total observed SET episodes for the combined Sum and Cout outputs. Additionally, this pulse type consistently generates the lowest LETth values on average for both outputs.

For the Hybrid FA, the radiation n-hit exhibits a slightly higher error rate when compared with pulse p-hit. Notably, the n-hit is responsible for the critical LETth values, both in terms of generating the highest error rate and holding the lowest LETth values on average. Specifically, 58% of errors in the Hybrid FA occur during the pulse n-hit modelation.

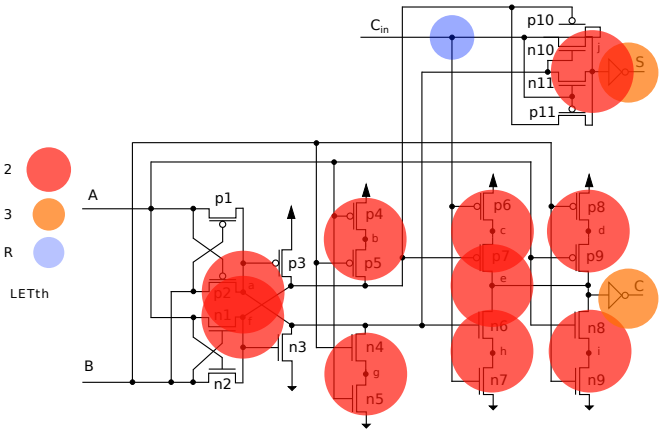
In the TGA topology, the n-hit continued to exhibit the highest susceptibility, contributing to 53% of the total error occurrence. Interestingly, both pulse types generated critical LETth values, particularly when the particle strike model was applied to the *Sum* node. This indicates that the *Sum* node is sensitive to both n-hit and p-hit in this topology.

In contrast to the other topologies, errors generated by the p-hit significantly increase for the TFA topology at NTV, accounting for nearly 53% of the total errors observed. However, it is noteworthy that for this FA the n-hit is responsible for generating all the critical LETth values during the simulations.

D. Critical Nodes

In the context of the Mirror FA, [5] highlight that nodes *g* and *j* stand out for exhibiting the lowest LETth values, rendering them particularly sensitive to SETs. Additionally, dropping the voltage operation resulted in a substantial 14 times worsening in the LETth values observed for this two critical nodes, decreasing it from 14 $MeVcm^2/mg$ in the nominal to 1 $MeVcm^2/mg$ in NTV operation. These observation aligns with the nominal operation, emphasizing that mitigating techniques applied to these internal nodes could prove more effective in enhancing the overall robustness of the Mirror FA against SETs.

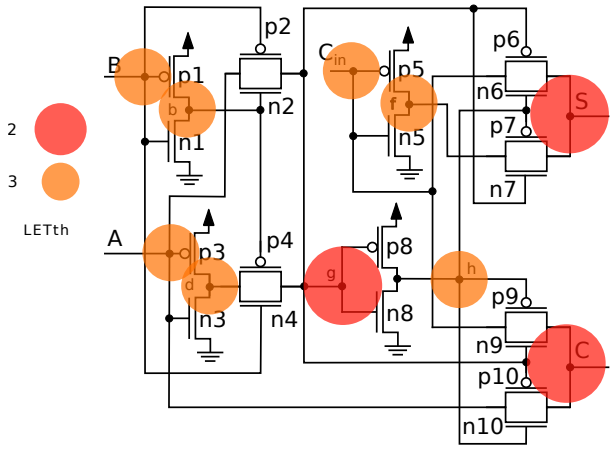
Fig. 1: Hybrid full adder critical nodes at NTV.



Shifting focus to the Hybrid FA, it is noteworthy that almost all nodes share a critical LETth value of 2 $MeVcm^2/mg$ with the exceptions of nodes *Sum*, *Cout*, and *Cin*. Fig. 1 illustrates the critical nodes, with node *Cin* presenting the highest LETth value and emerging as the less critical one for this topology. Comparing with the previous results at nominal voltage operation we could elect nodes *b*, *c*, and *d* possible candidates to apply mitigation techniques in order to reduce SET for this topology at both nominal and NTV operation.

The internal nodes of the Hybrid FA, as observed in the Mirror FA, display an increased vulnerability and sensitivity to error generation. The utilization of a combination of complementary and PTL in its construction suggests that this may not be the most suitable technique for architectures intended to operate in noisy environments. Another noteworthy aspect for this topology is that the node *Cin* remained unaffected by the reduction in voltage operation, maintaining a LETth value above $100 MeVcm^2/mg$.

Fig. 2: TGA full adder critical nodes at NTV.

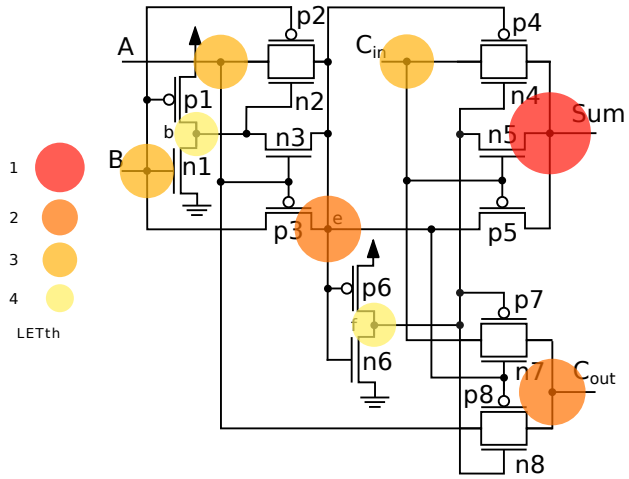


Upon analyzing the TGA topology, a notably more aggressive reduction in the critical LETth is observed, reaching 2 $MeVcm^2/mg$ when operating at reduced voltage. This signifies a substantial increase in sensitivity for the critical nodes at NTV. Remarkably, the critical nodes identified as *Sum* and *Cout* at the low voltage operation. Additionally, node *g* emerged as another critical node, exhibiting the same critical LETth value in this scenario, as Fig. 2 shows. This heightened sensitivity in critical nodes underscores the impact of reduced voltage on the vulnerability of the TGA topology to radiation-induced effects.

In the case of the TFA topology, the critical node *Sum* maintained its status unchanged throughout the reduction in voltage operation. Interestingly, the simulation results reveal a 14x decrease in the lowest observed LETth for the *Sum* output. This indicates a heightened sensitivity of the *Sum* node to radiation-induced effects when operating at NTV. Furthermore, the previously moderate node *Cout* has now emerged as one of the critical nodes, exhibiting a LETth of only 2 $MeVcm^2/mg$ at reduced voltage, highlighted in Fig. 3.

This significant reduction in LETth for *Cout* underscores its increased susceptibility to SETs under NTV conditions. The observation that all nodes in this topology present LETth values of no more than 4 $MeVcm^2/mg$ highlights the overall sensitivity of the TFA architecture when operating at NTV. This sensitivity underscores the importance of carefully considering mitigation strategies to enhance radiation resilience in such scenarios.

Fig. 3: TFA full adder critical nodes at NTV.



IV. SET Mitigation Techniques

The previous evaluation shows the SET sensibility of the FA considered in this work, even adopting a multigate technology. Thus, mitigation techniques must be explored in the design to reach more elevated levels of SET robustness. This study delves into the application of TS and DCELL, both independently and in combination, targeting the most sensitive nodes within these circuits. Sizing technique increases every device within each circuit from 1-fin to 3-fin.

A. Error Rate

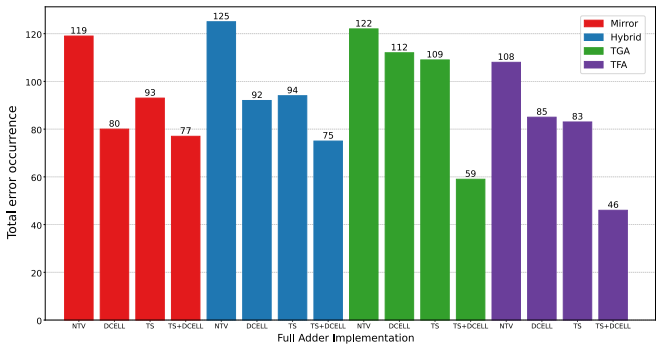
Reducing the voltage operation amplifies the sensitivity of the circuits, as discussed in Section III, underscoring the need for effective mitigation techniques. In the case of the Mirror FA, the application of DCELL results in a reduction of total errors by up to 32%, as presented in Figure 4. The TS technique exhibits a more modest decrease of nearly 22% in the error. The most promising results are achieved by combining both techniques, yielding a reduction of up to 35%.

For the Hybrid FA at NTV, there is an increase close to 33% in the total error occurrence compared to nominal values without mitigation techniques. The application of DCELL on the target nodes for this topology results in a 26% decrease in the total error count, while sizing the transistors reduces it by almost 25%. The most favorable outcomes are observed when combining both techniques, achieving a total reduction of 40% in the error count.

The TGA topology at NTV presented an expressive increase of almost 39% in the total number of errors compared to its implementation at nominal voltage. The use of DCELL for this topology reduced the total error occurrence by only 8%. Similarly, the use of TS reduced the errors by close to 11%. The best outcome for the TGA was achieved by combining both techniques, resulting in an expressive reduction of close to 52% in the propagated errors.

For the TFA topology at NTV, the observed errors were 54% larger than its implementation at nominal voltage, making it the critical topology when comparing to switching to lower voltage operation. The usage of DCELL helps to reduce the

Fig. 4: Total error for all topologies at NTV.



errors by up to 21%, while sizing the transistors yields similar results with a reduction of 23%. Following the same trend as previous topologies, the best results were found when combining both techniques, with a significant reduction of up to 44%. Despite the voltage reduction potentially increasing the number of propagated errors, the results show that the use of mitigation techniques still can help improve sensitivity while preserving the potential reduction in power consumption that working at NTV can provide.

B. Input Vectors

For the Mirror FA using DCELL it is possible to observe that vectors 011 and 101 are the most susceptible to generate errors, presenting together up to 28% of the total errors. On the other hand, with TS, the vector 000 generates most errors and when combining techniques vectors 001 and 100 are the ones that generate up to 32%. However, for all scenarios at NTV, vector 000 is the critical one, presented the lowest LETth values despite the mitigation technique applied at the low voltage operation.

At NTV, using DCELL on the Hybrid topology all vectors present similar error rate close to 13% of the total error, except for vectors 001 and 110 which show a smaller rate of almost 11%, on average. When using TS only vector 011 presents the highest susceptibility of almost 16%. Combining both techniques drops the critical node sensitivity to 15% for the vector 011.

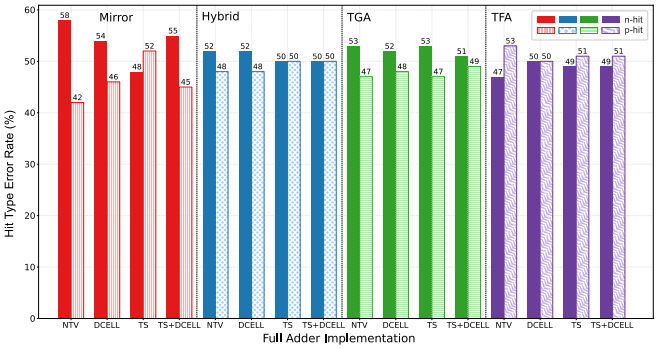
The TGA topology indicates that vectors 010, 011, and 110 have higher error rates. However, when implementing TS for the topology, only vector 110 maintained the highest error susceptibility of almost 16%. When combining both techniques the critical vector became 011 being alone responsible for close to 11% of the total error observed.

Lastly, the results for TFA topology shows that when using DCELL technique the node more prone to propagate errors is the 011 presenting 16% of the total error observed. Applying the TS for the this topology, vectors 010 and 100 present the highest error susceptibility of almost 15%. Combining techniques did not improve the sensitive vectors, keeping 010 and 100 the critical.

C. Type of SEE hit

Reducing the voltage operation alters the critical hit dynamics across the evaluated scenarios. In the case of the Mirror FA, employing DCELL the most susceptible is the n-hit, responsible for 54% of errors, highlighted in 5. Conversely, with the TS technique, the p-hit emerges as critical, accounting for 54% of errors. Combining DCELL and TS maintains n-hit as critical, with a 55% error rate. For the Hybrid FA, differences in error rates between pulse types reduces compared to the nominal voltage implementation. DCELL technique in this topology predominantly propagates errors from n-hit to the output. With TS and TS+DCELL implementations, both pulse types contribute equally to errors, with n-hit being critical across all scenarios.

Fig. 5: Error rate for n-hit and p-hit at NTV.



In the TGA topology at NTV, DCELL maintains the n-hit as critical, responsible for 52% of errors. Similarly, TS results in n-hit causing 53% of errors. Combining both techniques also highlights n-hit as critical for error propagation. Similar to the other topologies the pulse high-to-low can be defined as the critical one for the TGA topology. Finally, for TFA topology voltage reduction alters the critical pulse behavior. With DCELL, both pulses exhibit similar error rates, each contributing 50% to total errors. However, with TS and the combined scenario, the p-hit becomes critical, accounting for 51% of errors. Notably, the p-hit emerges as critical, generating most errors on average across scenarios.

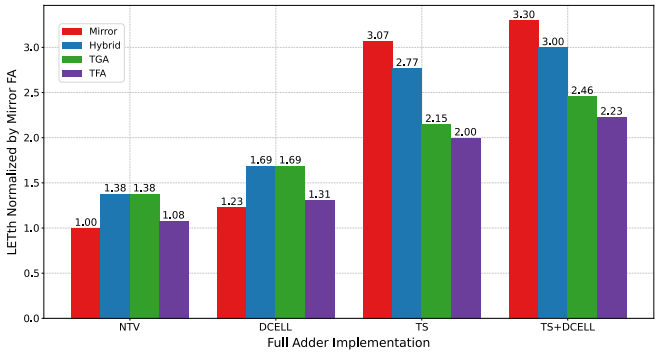
The results shows that the pulse type dynamics are linked with the effectiveness of mitigation techniques and the impact of voltage reduction on error rates. Across various circuit topologies, different mitigation techniques, such as DCELL and TS, interact differently with pulse types, influencing the critical pulse for error propagation.

D. Critical Nodes

Reducing the voltage operation had a significant impact on the critical LETth observed across all topologies. The Mirror FA at NTV serves as a comparison reference for the other topologies. For the Mirror FA in the reduced voltage operation, node *j* exhibits a minimum LETth of 1 $MeVcm^2/mg$ when employing DCELL. With sizing, the LETth increases by 3.07x, yet the lowest value is still presented by node *j*. Moreover,

when applying TS+DCELL in the circuit, both node *g* and *j* exhibit the same LETth value, close to 3.30x the critical reference. Node *j* remains responsible for most of the LETth values across both voltage scenarios used.

Fig. 6: LETth normalized by Mirror FA at NTV.



However, for the Hybrid FA at NTV with DCELL, nearly all nodes in the circuit remain sensitive, exhibiting the same lowest LETth of 2 $MeVcm^2/mg$. Conversely, scenarios employing TS show a different behavior, with only nodes *a* and *g* being critical, and with an improvement of 2.77x in the critical value. Combining both techniques increases the LETth slightly further to 3.27 $MeVcm^2/mg$. Notably, at NTV, TS proves slightly more efficient in mitigating the number of errors for this topology.

At NTV, for the TGA topology, the implementation of DCELL resulted in a 1.68x improvement in LETth, reaching a critical value of 2 $MeVcm^2/mg$ for nodes *g*, *Sum*, and *Cout*. Sizing the transistors increased the LETth to 2.35 $MeVcm^2/mg$, marking a 2.15x enhancement, as illustrated in Figure 6. Combining these mitigation techniques provided a slight increase of close to 2.46x in the observed LETth. Notably, the output nodes retained their critical status across all scenarios, presenting all critical LETth values.

The TFA topology at NTV exhibited a slight improvement in robustness when employing DCELL, with a 1.31x increase in LETth compared to the reference. Sizing the target devices resulted in a 2x improvement, with critical values of 2 $MeVcm^2/mg$ observed for the output nodes. The most significant enhancement for this topology was achieved by combining both techniques, yielding a 2.23x increase in LETth for the *Sum* node.

V. Conclusion

Considering the impact of the mitigation techniques employed, it becomes evident that a combination of DCELL and sizing adjustments consistently yields the most substantial reduction in total errors for all FAs investigated. Across the topologies evaluated, different mitigation techniques, interact differently with pulse types, influencing the critical pulse for error propagation. Pass transistor logic-based topologies often exhibit higher sensitivity to current propagation allowing errors introduced an internal node to easily spread to the output. Although the overall error count may be lower, these errors tend to manifest as critical LETth values, indicating their heightened impact on the system.

The results present that, with the exception of the TFA, the n-hit pulses are notably more prone to being collected and propagated to the outputs across all topologies. The LETth can be improved by up to 3.30x, and on average, when used across the topologis. Combining mitigation techniques yields an average improvement of close to 2.74x for all topologies. Although less effective, DCELL alone can still enhance the critical LETth close to 1.48x, on average.

Overall, understanding the relationship between pulse types, mitigation techniques, and voltage reduction is crucial for developing effective strategies to mitigate radiation-induced errors in integrated circuits in the firsts design stages.

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