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Victor Sabiá Pereira Carpes

DESIGN-ORIENTED MOSFET MODELLING APPLIED TO AN ULTRA-LOW-POWER SELF-BIASED DC CURRENT SOURCE

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Orientador: Prof. Márcio Cherem Schneider, Dr.

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Este Trabalho de Conclusão de Curso foi julgado adequado para obtenção do Título de "Bacharel em Engenharia Eletrônica" e aprovado em sua forma final pelo Curso de Graduação em Engenharia Eletrônica.

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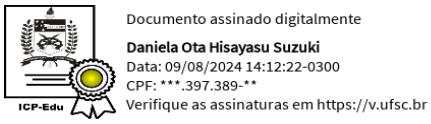

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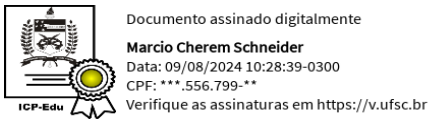
Coordenadora do Curso

Banca Examinadora:



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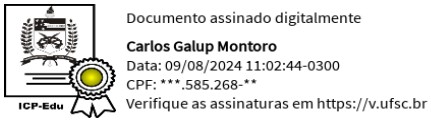

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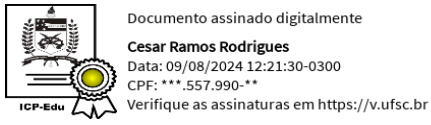

Prof. Cesar Ramos Rodrigues, Dr.
Avaliador
UFSC/CTC/EEL

This work is dedicated to my family, for the support and encouragement they gave me during my academic journey, both in person in Brazil and remotely during my exchange in France.

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"There's real poetry in the real world.
Science is the poetry of reality."
(Richard Dawkins, 2007)

RESUMO

Este trabalho de conclusão de curso apresenta os estudos realizados durante um projeto de iniciação científica entre setembro de 2021 e agosto de 2022 no Laboratório de Circuitos Integrados (LCI) em Florianópolis e os estudos realizados entre outubro de 2023 e janeiro de 2024 no laboratório TIMA em Grenoble. O trabalho consiste de uma visão geral da modelagem com base física de transistores de efeito de campo metal-óxido-semicondutor (MOSFETs) usando o modelo *Advanced Compact MOSFET* (ACM), a partir do qual é projetada uma fonte de corrente auto-polarizada (SBCS) de ultra baixa potência visando 1 pA para dispositivos vestíveis. O circuito final foi implementado em simulação usando a ferramenta *Virtuoso Layout Suite* e o kit de design de processo (PDK) da tecnologia *bulk* CMOS de 180 nm da *Taiwan Semiconductor Manufacturing Company* (TSMC). O circuito final apresenta, para uma tensão de saída fixa em 1,8 V, uma corrente de saída de 1,45 pA, um consumo máximo de 184 pW e uma regulação de linha média variando entre 3,82 %/V e 4,68 %/V para diferentes tensões de saída. A sensibilidade térmica média do circuito na faixa de temperatura segura para contato prolongado com a pele é de 0,53 %/°C.

Palavras-chave: Modelagem MOSFET. Tecnologia CMOS. Eletrônica de baixa potência.

ABSTRACT

This undergraduate thesis presents the studies done during an undergraduate research project between September 2021 and August 2022 at the Integrated Circuits Laboratory (LCI) in Florianópolis and the studies done between October 2023 and January 2024 at the TIMA laboratory in Grenoble. The work consists of an overview of the physics-based modelling of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) using the Advanced Compact MOSFET (ACM) model, from which an ultra-low-power Self-Biased Current Source (SBCS) targeting 1 pA for wearable devices is designed. The final circuit was implemented via simulation using the Virtuoso Layout Suite and the Process Design Kit (PDK) for the 180 nm bulk CMOS node from Taiwan Semiconductor Manufacturing Company (TSMC). The finalised circuit shows, for an output voltage fixed at 1.8 V, an output current of 1.45 pA, a maximum power consumption of 184 pW, and a line regulation varying between 3.82 %/V and 4.68 %/V for different output voltages. The circuit's average thermal sensibility on the safe temperature range for prolonged skin contact is 0.53 %/°C.

Keywords: MOSFET modelling. CMOS technology. Low-power electronics.

RÉSUMÉ

Ce projet de fin d'études présente les études réalisées lors d'un projet d'initiation scientifique entre septembre 2021 et août 2022 au Laboratoire de Circuits Intégrés (LCI) à Florianópolis, ainsi que les études réalisées entre octobre 2023 et janvier 2024 au laboratoire TIMA à Grenoble. Le travail consiste en une vue d'ensemble de la modélisation basée sur la physique des transistors à effet de champ métal-oxyde-semiconducteur (MOSFETs) en utilisant le modèle *Advanced Compact MOSFET* (ACM), à partir de laquelle est conçue une source de courant auto-polarisée (SBCS) ultra-basse consommation visant 1 pA pour les appareils portables. Le circuit final a été implémenté par simulation en utilisant l'outil *Virtuoso Layout Suite* et le kit de conception de processus (PDK) pour le nœud *bulk* CMOS de 180 nm de *Taiwan Semiconductor Manufacturing Company* (TSMC). Le circuit finalisé présente, pour une tension de sortie fixée à 1,8 V, un courant de sortie de 1,45 pA, une consommation de puissance maximale de 184 pW et une régulation de ligne variant entre 3,82 %/V et 4,68 %/V pour différentes tensions de sortie. La sensibilité thermique moyenne du circuit dans la plage de température sûre pour un contact prolongé avec la peau est de 0,53 %/°C.

Mots-clés : Modélisation MOSFET. Technologie CMOS. Électronique de faible puissance.

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LIST OF ABBREVIATIONS AND ACRONYMS

3PM	Three-Parameter Model
4PM	Four-Parameter Model
5PM	Five-Parameter Model
7PM	Seven-Parameter Model
ACM	Advanced Compact MOSFET
BRAFITEC	Brazil-France Engineering and Technology Program
CAPES	Coordination of Superior Level Staff Improvement Foundation
CMOS	Complementary Metal–Oxide–Semiconductor
DIBL	Drain-Induced Barrier Lowering
EEL	Electrical and Electronic Engineering Department
FDSOI	Fully Depleted Silicon On Insulator
Grenoble INP	Grenoble Institute of Technology
KDE	Kernel Density Estimation
LCI	Integrated Circuits Laboratory
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-channel MOSFET
PDF	Probability Density Function
PDK	Process Design Kit
PIBIC	Institutional Undergraduate Research Scholarship Program
PMOS	P-channel MOSFET
Phelma	National School of Engineering in Physics, Applied Physics, Electronics & Materials Science
SBCS	Self-Biased Current Source
SCM	Self Cascode MOSFET
TIMA	Techniques of Informatics and Microelectronics for integrated systems Architecture
TSMC	Taiwan Semiconductor Manufacturing Company
UCCM	Unified Charge-Control Model
UFSC	Federal University of Santa Catarina
UGA	Grenoble Alpes University
UICM	Unified Current-Control Model
VFCM	Voltage-Follower Current Mirror
ZTC	Zero Temperature Coefficient

LIST OF SYMBOLS

C_{ox}	Oxide capacitance per unit area
F_i	UICM auxiliary function
F_q	UCCM auxiliary function
I_D	Drain current
I_G	Gate current
I_X	Core's reference current
I_f	Forward current
I_r	Reverse current
I_s	Specific current
I_{Dsat}	Saturated drain current
I_{sh}	Sheet specific current defined as $I_{sh} = I_s/S$
L	Gate length
M_0	Unit transistor
Q_D	Charge density at the drain
Q_S	Charge density at the source
Q_t	Thermal charge density defined as $Q_t = -nC_{ox}\phi_t$
Q_{Dsat}	Saturated charge density at the drain
S	Transistor aspect ratio defined as $S = W/L$
V_D	Drain voltage
V_G	Gate voltage
V_P	Pinch-off voltage
V_S	Source voltage
V_X	Core's reference voltage
V_{T0}	Threshold voltage
V_{dd}	Power supply voltage
V_{out}	Output voltage
W	Gate width
α	Ratio between the inversion levels of the transistors in a SCM
μ	Carrier mobility
ϕ_t	Thermal voltage
σ	DIBL factor
ϑ	Transconductance-to-current ratio normalised by its maximum value defined as $\vartheta = (g_m/I_D) \,/\, (g_m/I_D)_{max}$
ζ	Velocity saturation factor
g_m	Gate transconductance
i_f	Forward inversion level defined as $i_f = I_f/I_s$
i_r	Reverse inversion level defined as $i_r = I_r/I_s$

n	Sub-threshold slope factor
q_D	Normalised charge density at the drain defined as $q_D = Q_D/Q_t$
q_S	Normalised charge density at the source defined as $q_S = Q_S/Q_t$
q_{Dsat}	Normalised saturated charge density at the drain defined as $q_{Dsat} = Q_{Dsat}/Q_t$
v_{sat}	Saturation velocity of the carriers

CONTENTS

1 INTRODUCTION

When talking about integrated circuits, current sources and mirrors are fundamental blocks, responsible for biasing other blocks on the chip. With the advent of wearable devices and other smart connected devices power-limited by a battery and/or reduced cooling systems, it is paramount to have robust design methodologies for ultra-low-power current sources.

Something that goes hand-in-hand with the development of such methodologies is the design-oriented modelling of MOSFET devices. Those models provide reduced sets of DC parameters, usually less than ten, instead of the tens of parameters employed by the compact models used in industry-standard simulation tools. This reduced set of parameters is more manageable for designers and allows them to develop the intuition of how each parameter influences the behaviour of the used transistors and, thus, the performance of the designed circuit. Among those models, the one adopted for this work is the Advanced Compact MOSFET (ACM) model.

1.1 PREVIOUS WORKS

The ACM model has multiple versions with differing numbers of parameters. The simplest of them is the Three-Parameter Model (3PM), developed in [1]. This version is more suitable for long-channel devices and has its three parameters extremely tied to physical properties of the device. To account for the Drain-Induced Barrier Lowering (DIBL) effect, the Four-Parameter Model (4PM) includes another parameter. This version is discussed in [2]. A more accurate version is the Seven-Parameter Model (7PM), that accounts for the DIBL, mobility lowering, velocity saturation and channel length modulation effects. This version, discussed in [3] and [4], is more accurate than the others at shorter channel lengths, but some of the parameters are more related to fitting than to the physics of the device. As a compromise, the Five-Parameter Model (5PM) has the three main parameters of the 3PM and another two to account for the DIBL and velocity saturation effects. This version is proposed in [5]. On the design aspect of the work, a Self-Biased Current Source (SBCS) topology is proposed and designed in [6] using the 3PM.

1.2 OBJECTIVES

The objectives of this work are as follows:

- Overview of the ACM model trough the detailing of some of its versions;
- Detailing of the characterisation process (extraction of model parameters);
- Detailing of a SBCS design methodology using the analytical ACM equations;

- Application of such methodology for ultra-low-power circuitry design aimed at wearable devices.

1.3 METHODOLOGY

This work focuses on two main topics, those being the design-oriented mathematical modelling of MOSFET devices and the design of an ultra-low-power current source targeting 1 pA using the described model. The modelling aspect will be presented in an as-is fashion. For the physics-based derivation of the model, refer to [1]. For the design aspect, the analytical design equations will be fully derived from the model equations and the results will be compared with simulation results. All used components come from the PDK for TSMC's 180 nm bulk CMOS node [7].

1.3.1 Work Organisation

This work consists of four chapters, the first being this one, and the last (chapter 4) being the closing of the work. The bulk of the work is contained in chapters 2 and 3, which discuss the two main pillars of this work.

Chapter 2 will discus the design-oriented modelling of MOSFET devices. Sections 2.1 and 2.2 will describe all parameters and equations for the 3PM, 4PM and 5PM and detail the process trough which the parameters for the 3PM (the chosen model for the design part) can be extracted.

Chapter 3 will derive the design equations for an ultra-low-power current source using the 3PM discussed in chapter 2. Section 3.1 will present the Self Cascode MOSFET (SCM) structure, the fundamental block of the current source, and derive its characteristic equation from the model. Sections 3.2 and 3.3 will use said characteristic equation to size all the relevant transistors to implement a current reference targeting 20 pA and implement this reference core without ideal components, respectively. Section 3.4 will present a current reducing stage to reach the 1 pA target and perform simulations to assess the performance of the completed circuit.

To finish, chapter 4 will conclude the work and propose future work on the subject.

1.3.2 Software Tools Used

Throughout the development of this work, multiple software tools were utilised. All simulation were executed with the Virtuoso Layout Suite [8]. The parameter extraction and the sizing of the transistors were all done automatically by Python [9] scripts using the NumPy [10] and SciPy [11] packages to numerically implement the equations derived in chapters 2 and 3. Those scripts can be found in appendix A. All circuit diagrams were generated using XCircuit [12]. Simulation results were exported from the simulator as

`.csv` files from which another Python script analysed the results using NumPy and SciPy and plotted all curves using the Matplotlib [13] package.

2 MOSFET MODELLING

In this chapter different versions of the ACM model will be described and the parameter extraction process will be detailed. Section 2.1 will describe the parameters and equations for the 3PM, 4PM and 5PM. Section 2.2 will describe the extraction process for the 3PM.

2.1 MODEL PARAMETERS AND EQUATIONS

The presentation of the models will begin with the 3PM and modify it adding one parameter at a time to get the 4PM and then the 5PM. All the following equations assume that the bulk is connected to ground and constitute a mapping $(V_G, V_S, V_D) \mapsto I_D$ for the device in DC operation. Similarly, all equations presented are for an N-channel MOSFET (NMOS), but can be easily modified to apply for an P-channel MOSFET (PMOS).

2.1.1 The Three-Parameter Model

The three parameters of the 3PM are as follows:

- I_s: specific current;
- V_{T0}: threshold voltage;
- n: sub-threshold slope factor.

The specific current can be expressed in terms of technological and geometric parameters according to eq. (2.1).

$$I_s = \mu_n C_{ox} n \frac{{\phi_t}^2}{2} \frac{W}{L} \tag{2.1}$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and W and L are the gate width and length respectively.

Alternatively, if we intend to work with multiple transistors in the same technology but with different sizes, W and L can be added as parameters and I_s can be substituted by the sheet specific current I_{sh} using eq. (2.2).

$$I_{sh} = \mu_n C_{ox} n \frac{{\phi_t}^2}{2} = \frac{I_s}{S} \tag{2.2}$$

where $S = W/L$ is the transistor's aspect ratio.

The drain current I_D is going to be decomposed into two components, a forward component I_f that depends only on V_G and V_S, and a reverse component I_r that depends only on V_G and V_D.[1] Those components make up the drain current according to eq. (2.3).

$$I_D = I_f - I_r = I_s \left(i_f - i_r\right) = I_{sh} S \left(i_f - i_r\right) \tag{2.3}$$

where $i_f = I_f/I_s$ and $i_r = I_r/I_s$ are called the forward and reverse inversion levels respectively.

The relation between the inversion levels and the terminal voltages is given by the Unified Current-Control Model (UICM) shown in eq. (2.4).

$$V_P - V_S = \phi_t F_i(i_f) \tag{2.4a}$$

$$V_P - V_D = \phi_t F_i(i_r) \tag{2.4b}$$

where V_P is the pinch-off voltage defined in eq. (2.5) and F_i is the UICM auxiliary function defined in eq. (2.6).

$$V_P = \frac{V_G - V_{T0}}{n} \tag{2.5}$$

$$F_i(x) = \sqrt{1+x} + \ln\Big(\sqrt{1+x} - 1\Big) - 2 \tag{2.6}$$

The $(V_G, V_S, V_D) \mapsto I_D$ mapping characteristic for the 3PM is defined by eqs. (2.3) to (2.5).[2]

As an alternative, instead of formulating the model in terms of currents, we could use charge densities instead. This alternative formulation facilitates the inclusion of higher order effects. This formulation uses the normalised charge densities at source and drain defined in eq. (2.7).

$$q_S = \frac{Q_S}{Q_t} = -\frac{Q_S}{nC_{ox}\phi_t} \tag{2.7a}$$

$$q_D = \frac{Q_D}{Q_t} = -\frac{Q_D}{nC_{ox}\phi_t} \tag{2.7b}$$

where $Q_t = -nC_{ox}\phi_t$ is the thermal charge.

Those charge densities relate to the inversion levels from the previous model formulation according to eq. (2.8).

$$q_S = \sqrt{1+i_f} - 1 \tag{2.8a}$$

$$q_D = \sqrt{1+i_r} - 1 \tag{2.8b}$$

Substituting eq. (2.8) into eq. (2.3) yields eq. (2.9).

$$I_D = I_s\,(q_S + q_D + 2)\,(q_S - q_D) \tag{2.9}$$

In this alternative formulation, instead of using the UICM, we have to use the Unified Charge-Control Model (UCCM) shown in eq. (2.10).

$$V_P - V_S = \phi_t F_q(q_S) \tag{2.10a}$$

$$V_P - V_D = \phi_t F_q(q_D) \tag{2.10b}$$

where F_q is the UCCM auxiliary function defined in eq. (2.11).

$$F_q(x) = x - 1 + \ln(x) \tag{2.11}$$

Like before, the 3PM's $(V_G, V_S, V_D) \mapsto I_D$ mapping is defined by eqs. (2.5), (2.9) and (2.10).[3,4]

2.1.2 The Four-Parameter Model

The 4PM modifies the 3PM by including the σ parameter to take the DIBL effect into account. This effect can be interpreted as a lowering of the threshold voltage with increases of V_D and/or V_S. This is done by replacing V_{T0} by $V_{T0} - \sigma\,(V_D + V_S)$ in eq. (2.5), yielding eq. (2.12).

$$V_P = \frac{V_G - V_{T0} + \sigma\,(V_D + V_S)}{n} \tag{2.12}$$

All other equations remain the same as in the 3PM, that is to say, the 4PM's $(V_G, V_S, V_D) \mapsto I_D$ mapping is defined by eqs. (2.9), (2.10) and (2.12).[5]

2.1.3 The Five-Parameter Model

To account for the velocity saturation effect, the 5PM adds the ζ parameter to the 4PM. This parameter is defined by eq. (2.13).

$$\zeta = \frac{\mu_n \phi_t}{L v_{sat}} \tag{2.13}$$

where v_{sat} is the carrier saturation velocity.

The first way in which ζ affects the model is by dividing eq. (2.9) by a factor that depends on q_S and q_D, yielding eq. (2.14).

$$I_D = I_s \frac{(q_S + q_D + 2)\,(q_S - q_D)}{1 + \zeta\,|q_S - q_D|} \tag{2.14}$$

The saturated drain current I_{Dsat} relates to the saturated charge density at the drain Q_{Dsat} according to eq. (2.15).

$$I_{Dsat} = -W v_{sat} Q_{Dsat} \tag{2.15}$$

By using eqs. (2.14) and (2.15), the normalised saturated charge density at the drain $q_{Dsat} = Q_{Dsat}/Q_t$ can be calculated with eq. (2.16).

$$q_{Dsat} = q_S + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2 q_S}{\zeta}} \tag{2.16}$$

The second way in which ζ affects the model is by modifying eq. (2.10), yielding an extended version of the UCCM shown in eqs. (2.17) and (2.18).

$$V_P - V_S = \phi_t F_q(q_S) \tag{2.17}$$

$$\frac{V_D - V_S}{\phi_t} = F_q(q_S - q_{Dsat}) - F_q(q_D - q_{Dsat}) \tag{2.18}$$

The $(V_G, V_S, V_D) \mapsto I_D$ mapping of the 5PM is, thus, composed of eqs. (2.12), (2.14), (2.15), (2.17) and (2.18).[6]

2.2 PARAMETER EXTRACTION PROCESS

This section will describe the process trough which the 3PM parameters can be extracted. When not specified, the temperature is assumed to be 26.85 °C. For this specific version of the model, the extraction can be done from a single curve from a common-source configuration, as shown in fig. 1. More specifically, the extraction process is done using the $I_D \times V_G$ curve for a fixed $V_D = \phi_t/2$.

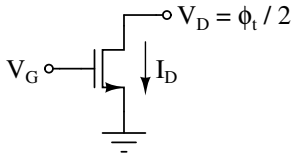


Figure 1 – Common-source configuration used for the extraction process.

2.2.1 Specific Current and Threshold Voltage Extraction

The extraction process of I_s and V_{T0} shown here comes from [14], where it is called the g_m/I_D procedure.

If we apply the conditions $V_S = 0$ and $V_D = \phi_t/2$ to eq. (2.10), we get eq. (2.19).

$$V_P = \phi_t F_q(q_S) \tag{2.19a}$$

$$V_P - \frac{\phi_t}{2} = \phi_t F_q(q_D) \tag{2.19b}$$

It can be shown from the 3PM equations that the gate transconductance g_m is given by eq. (2.20).

$$g_m = \frac{2I_s}{n\phi_t}(q_S - q_D) \tag{2.20}$$

By dividing eq. (2.20) by eq. (2.9) we get the transconductance-to-current ratio expressed in eq. (2.21).

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t(q_S + q_D + 2)} \tag{2.21}$$

Let's define a new quantity ϑ which is this g_m/I_D ratio normalised to its maximum value $(g_m/I_D)_{max} = 1/n\phi_t$ as shown in eq. (2.22).

$$\vartheta = \frac{g_m/I_D}{(g_m/I_D)_{max}} = \frac{2}{q_S + q_D + 2} \tag{2.22}$$

The principle of the method consists of sweeping V_G to find the point where $V_G = V_{T0}$. At this point, eq. (2.5) tells us that $V_P = 0$. Substituting this into eq. (2.19) yields eq. (2.23).

$$0 = F_q(q_S) \quad \Rightarrow \quad q_S = {F_q}^{-1}(0) = 1 \tag{2.23a}$$

$$-\frac{1}{2} = F_q(q_D) \quad \Rightarrow \quad q_D = {F_q}^{-1}\left(-\frac{1}{2}\right) \approx 0.766 \tag{2.23b}$$

Substituting eq. (2.23) into eqs. (2.9) and (2.22) we get $I_D \approx 0.881 \cdot I_s$ and $\vartheta \approx 0.531$ respectively.

The extraction process for I_s and V_{T0} is as follows. Sweep V_G and measure I_D, plot the $\vartheta \times V_G$ curve and find the point where $\vartheta = 0.531$. At this point, we have $V_{T0} = V_G$ and $I_s = 1.136 \cdot I_D$. An example of a $\vartheta \times V_G$ curve can be seen in fig. 2.

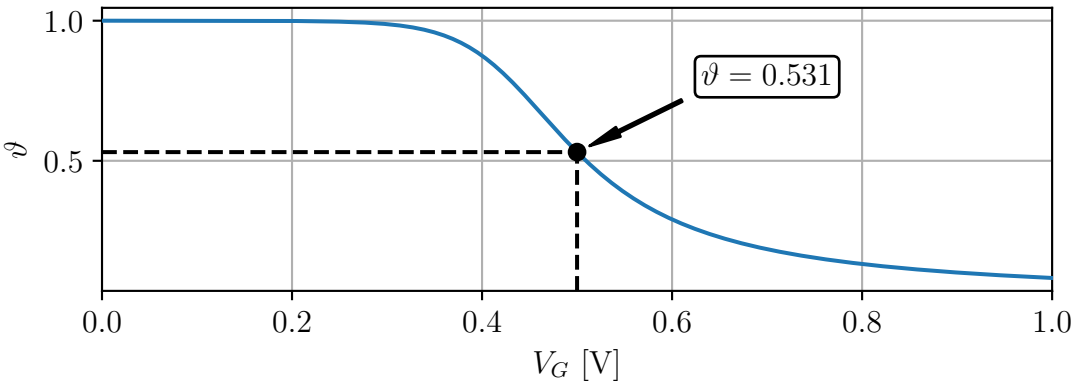


Figure 2 – Example plot of $\vartheta \times V_G$ generated by the 3PM equations with $I_s = 1\,\mu\text{A}$, $V_{T0} = 500\,\text{mV}$, $n = 1.5$ and $\phi_t = 25.85\,\text{mV}$.

To actually plot ϑ, we need a way of expressing it in terms of only measurable quantities, in this case, V_G and I_D. Recalling that g_m is the derivative of I_D with respect to V_G, we can rewrite eq. (2.21) as eq. (2.24).

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{d}{dV_G}\ln|I_D| \tag{2.24}$$

Substituting eq. (2.24) into eq. (2.22) yields eq. (2.25).

$$\vartheta = \frac{\frac{d}{dV_G}\ln|I_D|}{\max\left(\frac{d}{dV_G}\ln|I_D|\right)} \tag{2.25}$$

2.2.2 Sub-Threshold Slope Factor Extraction

As the name suggests, the sub-threshold slope factor is related to the slope of the $I_D \times V_G$ curve for $V_G < V_{T0}$. More specifically, it's the slope of said curve when traced in log scale.

The $I_D \times V_G$ relation can be approximated in the sub-threshold region by eq. (2.26).

$$I_D \approx \lambda e^{\frac{V_G}{n\phi_t}} \tag{2.26}$$

where λ is some proportionality constant. If we take the log of both sides, we get the linear relation between $\log_{10}(I_D)$ and V_G shown in eq. (2.27).

$$\log_{10}(I_D) = \log_{10}(\lambda) + \frac{\log_{10}(e)}{n\phi_t} \cdot V_G \tag{2.27}$$

This relation can be seen in fig. 3 which shows a clear relation between the slope of the curve and n.

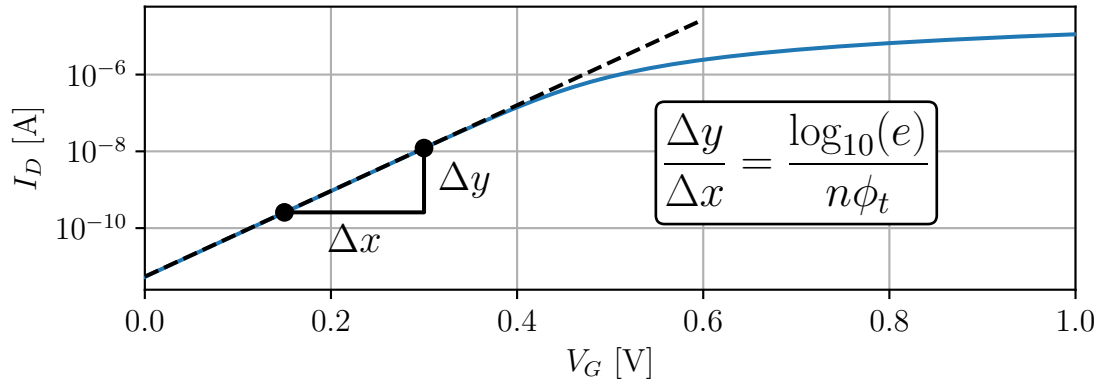


Figure 3 – Example plot of $I_D \times V_G$ in log scale generated by the 3PM equations with $I_s = 1\,\mu A$, $V_{T0} = 500\,mV$, $n = 1.5$ and $\phi_t = 25.85\,mV$.

If we choose two points (V_{G1}, I_{D1}) and (V_{G2}, I_{D2}) in the sub-threshold region, we can calculate the slope, from which we can get an expression for n, shown in eq. (2.28).

$$n = \frac{V_{G2} - V_{G1}}{\phi_t \ln\left(I_{D2}/I_{D1}\right)} \tag{2.28}$$

To guarantee that the linear extrapolation is accurate, we need to choose two points that are far bellow V_{T0}. A good rule of thumb is choosing a pair of gate voltages that are, at least, 5 to 10 thermal voltages bellow V_{T0}.

If we apply this procedure to the same curve used on the g_m/I_D procedure, we can extract all parameters from a single simple-to-measure curve.

2.2.3 Extracted Parameters for the Unit Transistor

The entire process described throughout this section was implemented in a Python script (shown in appendix A) that was used to characterise the unit transistor M_0 with dimensions $W = 220\,nm$ and $L = 19.995\,\mu m$.[7] The extraction results are displayed in table 1.

W	L	I_s	I_{sh}	V_{T0}	n
220 nm	19.995 µm	1.4376 nA	130.66 nA	363.2 mV	1.4684

Table 1 – Results of the extraction process for the unit transistor.

3 CURRENT SOURCE DESIGN

The design of the current source will be presented as follows. A theoretical analysis of the SCM structure will be presented in section 3.1. Sections 3.2 and 3.3 will describe how to, in principle, use two SCMs to generate a current reference of 20 pA (the core of the source) and implement it using a Voltage-Follower Current Mirror (VFCM) structure. Finally, section 3.4 presents a current reducing stage to reduce the core's current down to the desired 1 pA. All sections present simulation results when appropriate.

3.1 THEORETICAL ANALYSIS OF THE SCM STRUCTURE

The SCM structure consists of two transistors connected as depicted in fig. 4. The objective of this analysis is to find the expression for the $I_X \mapsto V_X$ mapping. For this analysis, both M_1 and M_2 are assumed to be associations of the same M_0 unit transistor. That is to say, they both share the same I_{sh}, V_{T0} and n extracted in section 2.2.

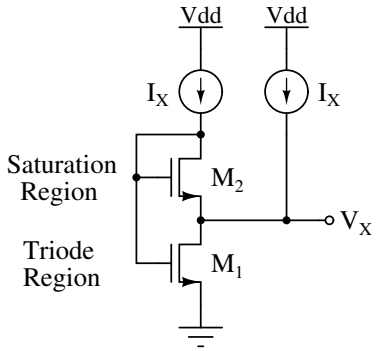


Figure 4 – SCM structure.

Since M_2 is saturated, we can assume that $i_{f2} \gg i_{r2}$ and $i_{f2} - i_{r2} \approx i_{f2}$. Furthermore, since $V_{G1} = V_{G2}$ and $V_{D1} = V_{S2}$, we have $i_{r1} = i_{f2}$. By applying eq. (2.3) to M_1 and M_2 we get eq. (3.1).

$$2I_X = I_{sh}S_1\Big(i_{f1} - \overbrace{i_{r1}}^{i_{f2}}\Big) = I_{sh}S_1\left(i_{f1} - i_{f2}\right) \tag{3.1a}$$

$$I_X = I_{sh}S_2\Big(\underbrace{i_{f2} - i_{r2}}_{i_{f2}}\Big) = I_{sh}S_2 i_{f2} \tag{3.1b}$$

By dividing eq. (3.1a) by eq. (3.1b) we get eq. (3.2).

$$2 = \frac{S_1}{S_2 i_{f2}}\left(i_{f1} - i_{f2}\right) \tag{3.2}$$

By using some algebra we can get eq. (3.3).

$$\alpha_{12} = \frac{i_{f1}}{i_{f2}} = 1 + 2\,\frac{S_2}{S_1} \tag{3.3}$$

This shows that the ratio of the inversion levels of M_1 and M_2 depends exclusively on the geometrical characteristics of the circuit. This means that if we impose i_{f2}, i_{f1} will be also be implicitly imposed. For this reason, we will say that i_{f2} is the overall inversion level of the SCM and we will substitute $i_{f1} = \alpha_{12} i_{f2}$ on eqs. (3.4) to (3.6).

If we apply eq. (2.4a) to M_1 and M_2 we get eq. (3.4).

$$V_P = \phi_t F_i(\alpha_{12} i_{f2}) \tag{3.4a}$$

$$V_P - V_X = \phi_t F_i(i_{f2}) \tag{3.4b}$$

Subtracting eq. (3.4b) from eq. (3.4a) yields eq. (3.5).

$$V_X = \phi_t \left[F_i(\alpha_{12} i_{f2}) - F_i(i_{f2}) \right] \tag{3.5}$$

By using eq. (3.1b) with eq. (3.5) we can write the expression for the $I_X \mapsto V_X$ mapping shown in eq. (3.6).

$$V_X(I_X) = \phi_t \left[F_i\left(\frac{\alpha_{12} I_X}{I_{sh} S_2}\right) - F_i\left(\frac{I_X}{I_{sh} S_2}\right) \right] \tag{3.6}$$

Something that has to be noted is that eq. (3.6) is a bijection. This is corroborated by fig. 5, which shows an example plot of eq. (3.6).

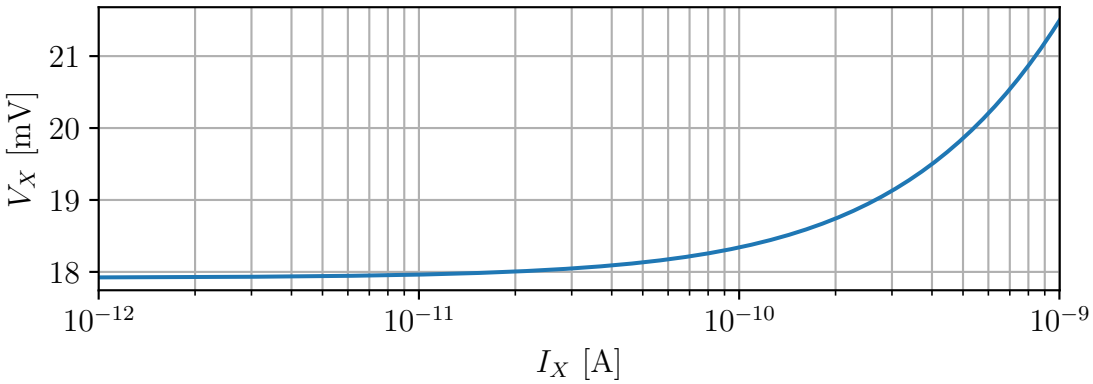


Figure 5 – Plot of eq. (3.6) with $I_{sh} = 150\,\text{nA}$, $\alpha_{12} = 2$, $S_2 = 0.01$ and $\phi_t = 25.85\,\text{mV}$.

3.2 DESIGN OF THE SOURCE'S CORE

The core of the current source consists of a reference current generator targeting 20 pA. For the core we need two SCM structures with different characteristics (and hence different graphs for the $I_X \mapsto V_X$ function). Due to both structures having a bijective nature, their graphs cannot have more than one intersection point. The idea is to design both SCMs (SCM_{12}, with transistors M_1 and M_2, and SCM_{34}, with transistors M_3 and M_4) such that this intersection point is the desired operating point and, thus, forcing them to have the same I_X and V_X. This section will detail how to design both SCMs and, after that, section 3.3 will present how to impose the same current and voltage upon them.

3.2.1 Design Equations

Since we have more degrees of freedom than equations, let's impose a couple of initial design conditions. Let's put SCM_{12} in moderate inversion with $i_{f2} = 10$ and SCM_{34} in weak inversion with $i_{f4} = 0.01$.[8] Furthermore, we will also impose $\alpha_{12} = 2$ and the target current is $I_X = 20\,\mathrm{pA}$.

We can use eq. (3.1b) applied to SCM_{12} to calculate S_2 according to eq. (3.7).

$$S_2 = \frac{I_X}{I_{sh} i_{f2}} \approx 1.5307 \times 10^{-5} \tag{3.7}$$

Using eq. (3.3) applied to SCM_{12}, we can get eq. (3.8).

$$S_1 = \frac{2S_2}{\alpha_{12} - 1} \approx 3.0613 \times 10^{-5} \tag{3.8}$$

If we apply eq. (3.5) to SCM_{12} we can calculate V_X according to eq. (3.9).

$$V_X = \phi_t \left[F_i(\alpha_{12} i_{f2}) - F_i(i_{f2}) \right] \approx 43.998\,\mathrm{mV} \tag{3.9}$$

Since both SCMs share the same V_X, we can apply eq. (3.5) to SCM_{34} to get eq. (3.10).

$$\alpha_{34} = \frac{1}{i_{f4}} F_i^{-1}\left(\frac{V_X}{\phi_t} + F_i(i_{f4}) \right) \approx 5.4246 \tag{3.10}$$

Now that we have α_{34}, we can apply eqs. (3.1b) and (3.3) to SCM_{34} to get eqs. (3.11) and (3.12) respectively.

$$S_4 = \frac{I_X}{I_{sh} i_{f4}} \approx 1.5307 \times 10^{-2} \tag{3.11}$$

$$S_3 = \frac{2S_4}{\alpha_{34} - 1} \approx 6.9188 \times 10^{-3} \tag{3.12}$$

All the relevant design parameters have been calculated using eqs. (3.7) to (3.12) in a Python script (see appendix A) and can be seen in table 2.

SCM_{12}				
S_1	S_2	i_{f1}	i_{f2}	α_{12}
3.0613×10^{-5}	1.5307×10^{-5}	20	10	2
SCM_{34}				
S_3	S_4	i_{f3}	i_{f4}	α_{34}
6.9188×10^{-3}	1.5307×10^{-2}	0.054 246	0.01	5.4246

Table 2 – Design parameters for the designed SBCS core.

If we trace the curves of both SCMs (shown in fig. 6), we can see that the intersection point is exactly the one intended. This shouldn't be surprising, considering that those curves were traced using the same equations used to design the SCMs.

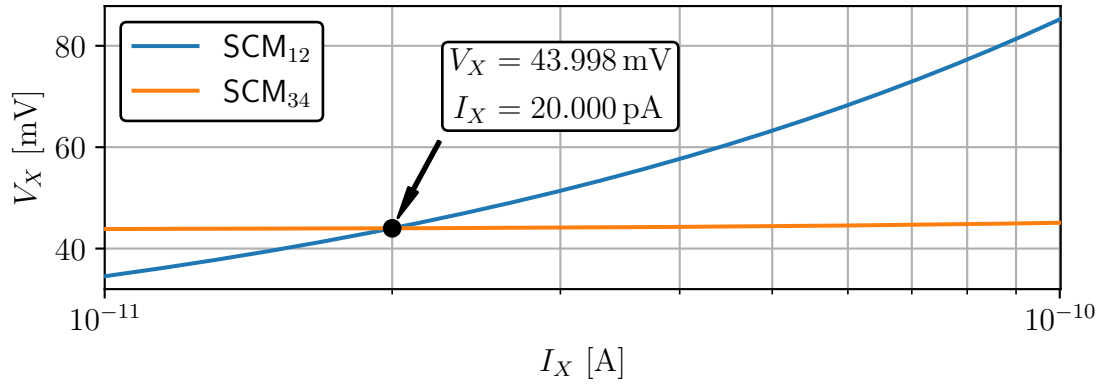


Figure 6 – Theoretical curves for SCM_{12} and SCM_{34}. The highlighted point is the intended operating point.

3.2.2 Associations of Unit Transistors

To achieve a given aspect ratio using M_0, we could make a $m \times n$ matrix as depicted in fig. 7.

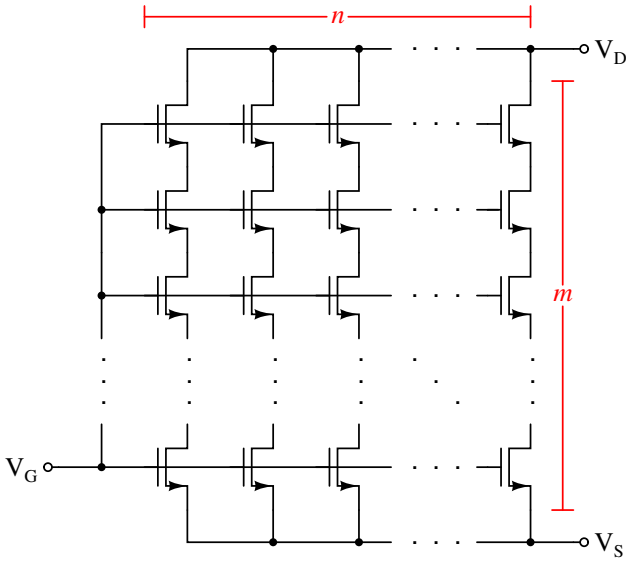


Figure 7 – Matrix of unit transistors.

The equivalent aspect ratio of such matrix would be given by eq. (3.13). By using such matrix we can achieve an equivalent aspect ratio S equal to any positive rational multiple of S_0, which is the aspect ratio of M_0.

$$S = \frac{n}{m} S_0, \quad m, n \in \mathbb{N}^* \tag{3.13}$$

When choosing the values for m and n, bigger values offer higher accuracy and less susceptibility to mismatch, but at the cost of taking up more space on the die. To achieve the desired aspect ratios for M_1, M_2, M_3 and M_4, m and n where chose to minimise the aspect ratio error while respecting the condition $m \times n \leq 1000$ per association. The found values can be seen in table 3.

	M_1	M_2	M_3	M_4
$m \times n$	359×1	719×1	35×22	23×32
Desired S	3.0613×10^{-5}	1.5307×10^{-5}	6.9188×10^{-3}	1.5307×10^{-2}
Achieved S	3.0648×10^{-5}	1.5303×10^{-5}	6.916×10^{-3}	1.5308×10^{-2}
Error	0.114 815 %	0.024 427 %	0.040 721 %	0.010 347 %

Table 3 – Calculated aspect ratios, achieved aspect ratios and their relative error.

Transistors M_1 and M_2 have quite large values for their equivalent L. This can be problematic when it comes to leakage current trough the gate. The ratio $I_G/I_D \propto L^2$,[9] usually negligible for short channel devices, gets bigger and bigger with L. Since the circuit is not going to be physically fabricated, and due to time constraints, this problem (that didn't manifest itself in simulation) was not directly addressed in this work.

3.2.3 SCM Simulations

To verify the operating point of the designed pair of SCMs, they both have been implemented in Virtuoso with the associations described in section 3.2.2 and their $I_X \times V_X$ curves were extracted using ideal current sources. Those curves and their intersection point can be seen in fig. 8.

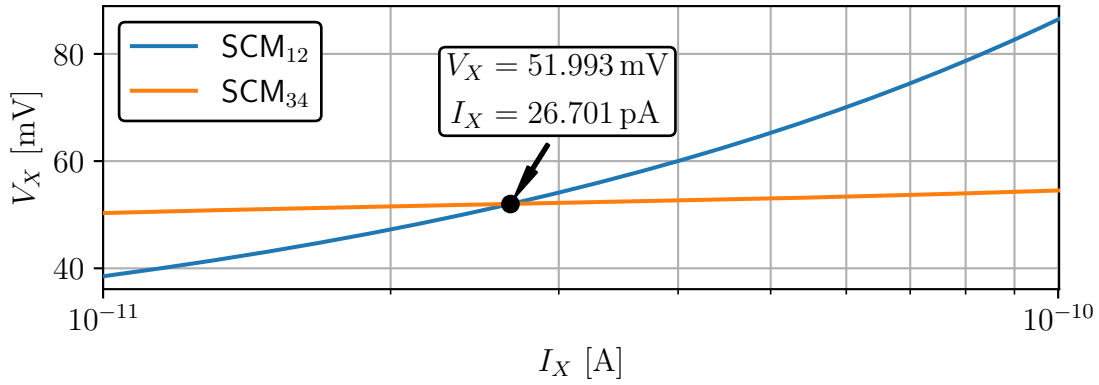


Figure 8 – Simulated curves for SCM_{12} and SCM_{34}. The highlighted point is the actual operating point.

We can see that, when implemented with the associations, V_X and I_X were 18.2 % and 33.5 % higher than expected. The value of V_X is mostly unimportant, but it's good it didn't change enough to remove M_2 and M_4 from the saturation region. More interestingly, the change in I_X was quite high. This discrepancy is most likely due to the substrate leakage that is not taken into account by the 3PM.[10] To get closer to the design target of 20 pA, a trimming was realised on M_3 by altering its matrix size. The found values for $m \times n$ were 29×22. The simulated curve of this trimmed pair of SCMs can be seen in fig. 9. The achieved values of V_X and I_X after trimming differ from the theoretical values by 6.34 % and 3.01 % respectively.

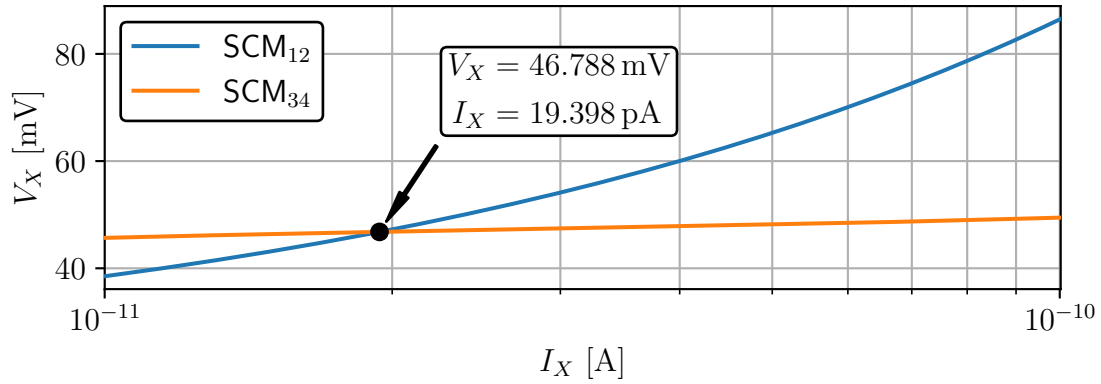


Figure 9 – Simulated curves for SCM_{12} and SCM_{34} after trimming. The highlighted point is the actual operating point.

3.3 COMPLETE SBCS CORE

The principle of operation of the SBCS is having two different SCMs structures with the same current and voltage. To do so, we will use a VFCM structure, which can be seen in fig. 10.

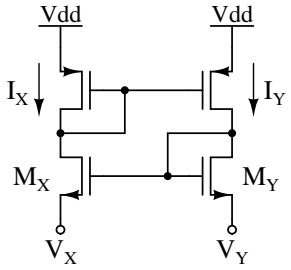


Figure 10 – VFCM structure.

If we assume that both M_X and M_Y are saturated, we have eq. (3.14).

$$I_X \approx I_{sX} i_{fX} \tag{3.14a}$$

$$I_Y \approx I_{sY} i_{fY} \tag{3.14b}$$

By having both PMOS transistors identical to each other, they form a $1:1$ current mirror and we can assume that $I_X \approx I_Y$. Furthermore, by having $M_X = M_Y$, we can also assume that $i_{fX} \approx i_{fY}$.

If we apply eq. (2.4) to M_X and M_Y, we get eq. (3.15).

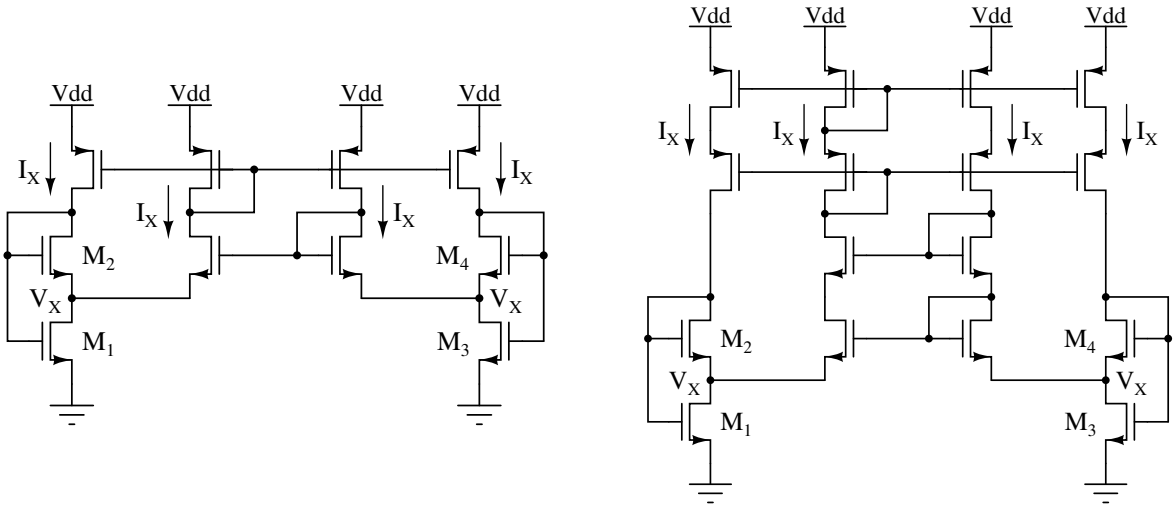
$$V_X = V_{PX} - \phi_t F_i\left(i_{fX}\right) \tag{3.15a}$$

$$V_Y = V_{PY} - \phi_t F_i\left(i_{fY}\right) \tag{3.15b}$$

Since both transistors are identical and share the same gate voltage, we have $V_{PX} = V_{PY}$. Substituting this and $i_{fX} \approx i_{fX}$ into eq. (3.15), we get $V_X \approx V_Y$. With those conditions, the VFCM structure provides a way of forcing both SCMs to operate in the

intersection point of their characteristic curves. For this work, all transistors used in the VFCM and all other current mirrors are 2×2 matrices of transistors with $W = 1\,\mu m$ and $L = 19.995\,\mu m$. The use of matrices instead of single transistors was done so to reduce the influence of component mismatch.

Connecting the VFCM to SCM_{12} and SCM_{34} we get the simple SBCS core shown in fig. 11a. To improve the accuracy of the PMOS current mirrors, the topology can be modified by using cascoded mirrors, as shown in fig. 11b. This modified topology was the one chosen for the rest of this work.



(a) SBCS core implemented using simple current mirrors.

(b) SBCS core implemented using cascoded current mirrors.

Figure 11 – SBCS core implemented with different types of current mirrors.

3.3.1 SBCS Core Simulations

Having completed the design of the core, we can start simulating its behaviour for different conditions.

The first type of simulation is a line regulation simulation. This consists of analysing how the reference current I_X varies with a changing power supply. The graph of such simulation can be seen in fig. 12.

From this plot we can observe a few things. The first is the nominal condition, that is to say, what is I_X if the power supply stays constant at the nominal 1.8 V. In this case, the nominal current is 20.3 pA, not far off from the expected 19.4 pA. The second thing we can gather is the average sensitivity[11] with the power supply. The average sensitivity through the range $700\,mV \leq V_{dd} \leq 1.8\,V$ is 4.17 %/V.

Similarly, we can analyse how sensitive the circuit is to temperature changes. Figure 13 shows the plot of I_X for a fixed power supply of 1.8 V with the temperature varying from 0 °C to 100 °C.

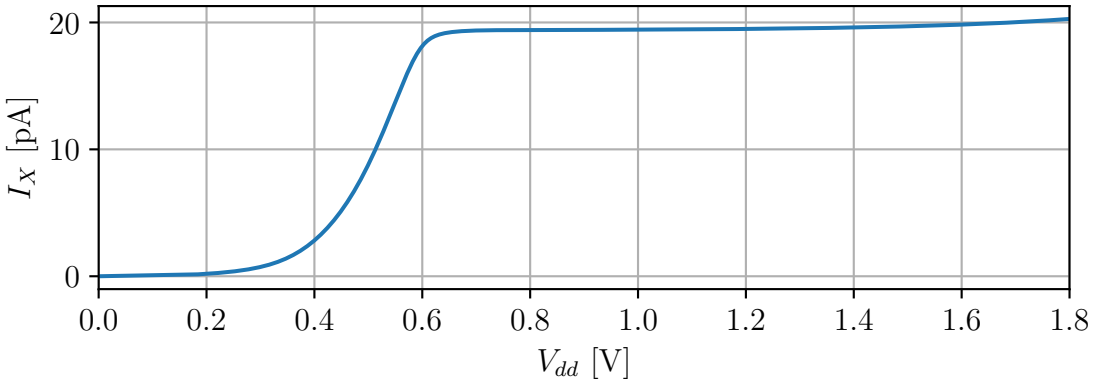


Figure 12 – Line regulation simulation for the designed SBCS core.

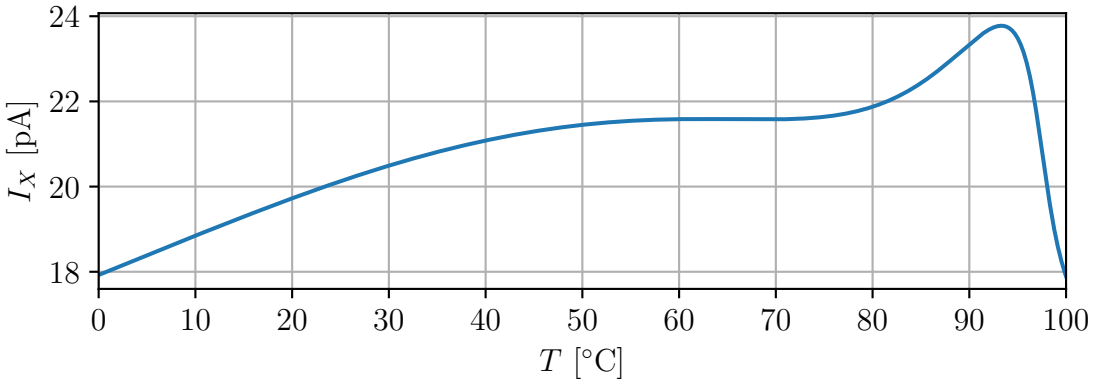


Figure 13 – Temperature simulation for the designed SBCS core.

We see an interesting behaviour. Up to around 30 °C, the current is linear-like. From 30 °C to 70 °C, the current starts to saturate, with a Zero Temperature Coefficient (ZTC) point at around 60 °C. From 70 °C to 93 °C, the current ramps up again, with another ZTC point at 93 °C. More interesting than the other regions of operation, from 93 °C onwards we see a drastic drop in current with the rising temperature. The current gets reduced to close to the value at 0 °C. If we calculate the average thermal sensitivity on the full range, we get a value of $-0.002\,\%/°C$. This value is very close to zero and negative because the end current is slightly less than the start current. As the intended application of the circuit is that of wearable devices, it is not reasonable to expect it to operate at extremely cold or hot temperatures such as 0 °C or 100 °C, so this sensitivity does not reflect the actual operating temperature range of the device.

According to [15], a rule of thumb for safe temperatures for prolonged skin contact are those comprised between 10 °C and 45 °C. For this range, the average thermal sensitivity is $0.35\,\%/°C$.

3.4 FULL CURRENT SOURCE

Having designed a working core that generates a nominal current reference of 20.3 pA, we need to find a way of reducing this current to the targeted 1 pA range. To do so, we will employ a current mirror.

3.4.1 Current Reducing Stage

Since the core generates a current of roughly 20 pA, we will use a 20 : 1 current mirror. The chosen topology is presented in [16] and is reproduced in fig. 14.

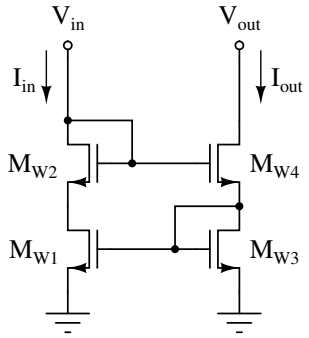


Figure 14 – Current reducing stage implemented with a four-transistor improved Wilson current mirror.

The transistors M_{W1} and M_{W2} are composed of five transistors with dimensions $W = 1\,\mu m$ and $L = 19.995\,\mu m$ in parallel, resulting in an aspect ratio of $S_{W1(2)} = {}^{5W}/_{L}$. The transistors M_{W3} and M_{W4} are composed of four transistors with the same dimensions in series, resulting in an aspect ratio of $S_{W3(4)} = {}^{W}/_{4L}$. This results on the desired ratio of ${}^{I_{out}}/_{I_{in}} = {}^{S_{W3(4)}}/_{S_{W1(2)}} = {}^{1}/_{20}$. Adding this mirror to the core from fig. 11b results in the complete SBCS shown in fig. 15.

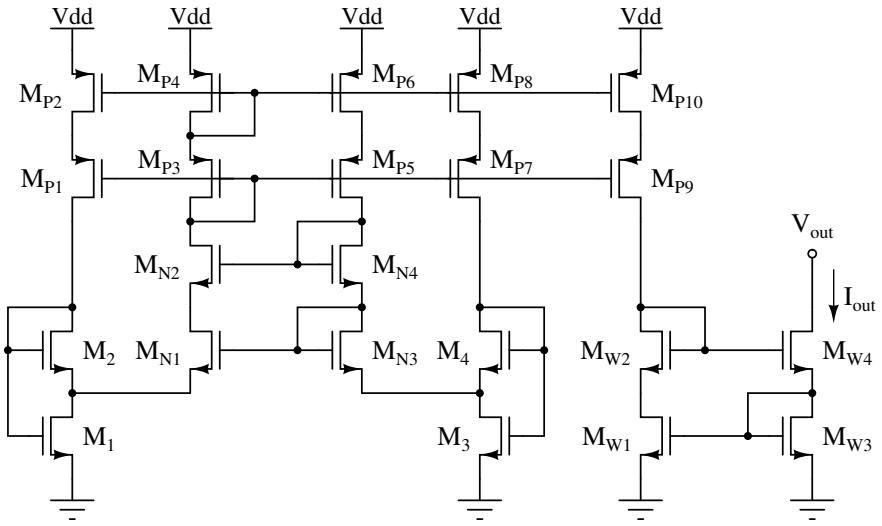


Figure 15 – Complete current source implemented by adding the current reducing stage from fig. 14 to the output of the SBCS core from fig. 11b.

Table 4 shows the dimensions of all transistors on the circuit as well as an estimation of the inversion levels for the nominal case $V_{dd} = V_{out} = 1.8\,\mathrm{V}$.[12]

	W	L	i_f
M_1	220 nm	$359 \times 19.995\,\mu\mathrm{m}$	3.82
M_2	220 nm	$719 \times 19.995\,\mu\mathrm{m}$	2.08
M_3	22×220 nm	$29 \times 19.995\,\mu\mathrm{m}$	3.74×10^{-2}
M_4	32×220 nm	$23 \times 19.995\,\mu\mathrm{m}$	5.91×10^{-3}
M_{N1}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	1.16×10^{-3}
M_{N2}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	4.91×10^{-4}
M_{N3}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	1.18×10^{-3}
M_{N4}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	5.14×10^{-4}
M_{P1}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	6.85×10^{-3}
M_{P2}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	8.01×10^{-3}
M_{P3}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	6.91×10^{-3}
M_{P4}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	8.01×10^{-3}
M_{P5}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	6.84×10^{-3}
M_{P6}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	8.01×10^{-3}
M_{P7}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	6.83×10^{-3}
M_{P8}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	8.01×10^{-3}
M_{P9}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	6.83×10^{-3}
M_{P10}	$2 \times 1\,\mu\mathrm{m}$	$2 \times 19.995\,\mu\mathrm{m}$	8.01×10^{-3}
M_{W1}	$5 \times 1\,\mu\mathrm{m}$	$19.995\,\mu\mathrm{m}$	3.55×10^{-4}
M_{W2}	$5 \times 1\,\mu\mathrm{m}$	$19.995\,\mu\mathrm{m}$	2.49×10^{-4}
M_{W3}	$1\,\mu\mathrm{m}$	$4 \times 19.995\,\mu\mathrm{m}$	4.08×10^{-4}
M_{W4}	$1\,\mu\mathrm{m}$	$4 \times 19.995\,\mu\mathrm{m}$	2.58×10^{-4}

Table 4 – Dimensions and estimated inversion levels of all transistors on the circuit for nominal conditions.

3.4.2 Full Source Simulations

Just like was done for the core, we need to analyse the behaviour of the complete source. The first simulation is the line regulation, but this time, there's a difference. The output current I_{out} is going to depend on the voltage at the output node V_{out}. For this reason, a parametric simulation was executed to asses the line regulation for different fixed values of V_{out}. The plots resulting of such simulation can be seen in fig. 16.

We can see that all curves follow a similar shape, differing from each other essentially by vertical shifts. For the nominal case ($V_{dd} = V_{out} = 1.8\,\mathrm{V}$), the output current was $I_{out} = 1.45\,\mathrm{pA}$, with a total power consumption of 184 pW. On the operating range of

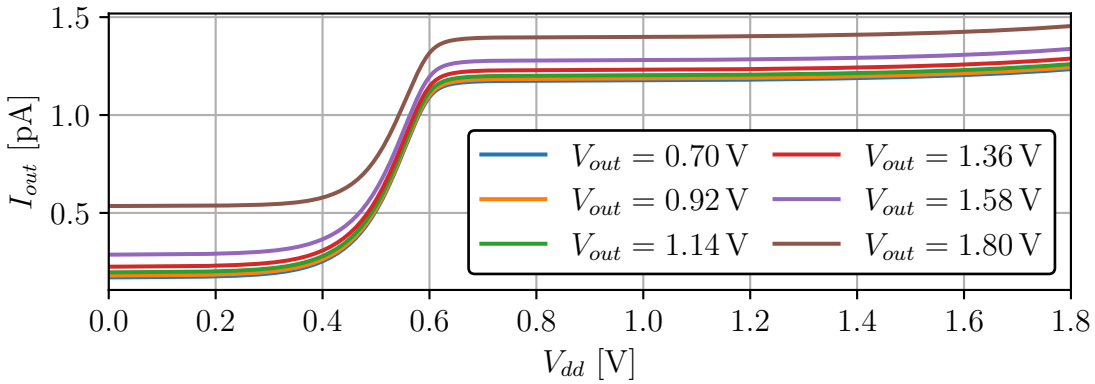


Figure 16 – Line regulation simulation for the full source for different output voltages.

$700\,\mathrm{mV} \leq V_{dd} \leq 1.8\,\mathrm{V}$, the average line regulation varied from $3.82\,\%/\mathrm{V}$ to $4.68\,\%/\mathrm{V}$ for the different output voltages listed in fig. 16.

Let's analyse the thermal sensitivity of the complete source. For this simulation, we keep the power supply fixed at the nominal $1.8\,\mathrm{V}$ and the output voltage fixed at the same value. The plot of such simulation is shown in fig. 17.

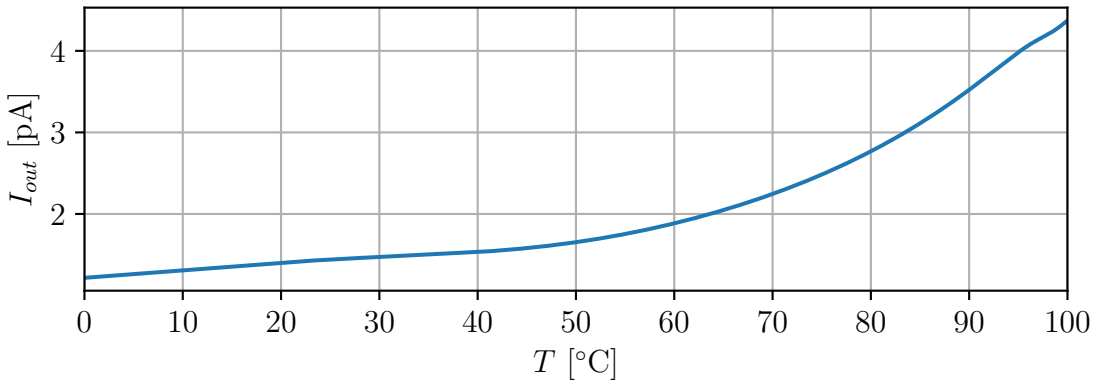


Figure 17 – Temperature simulation for the full source.

The shape of the curve not at all like the one on fig. 13. The curve is now monotonically increasing and shows no ZTC points. From $50\,^{\circ}\mathrm{C}$ onwards, the current climbs exponentially. We can see a slight decrease in the slope at $95\,^{\circ}\mathrm{C}$ due to the current drop showed in fig. 13. The thermal sensitivity on the full range is $1.28\,\%/^{\circ}\mathrm{C}$. Luckily, the temperature range where the current varies the most is outside the skin-safe range. On this range, the sensitivity is $0.53\,\%/^{\circ}\mathrm{C}$, a much smaller value.

The last thing to simulate is the dispersion caused by component mismatch. This can be verified by running a Monte Carlo simulation where the parameters of each transistor are sampled from statistical distributions defined on the PDK.

To evaluate the dispersion of I_{out} due to mismatch, a Monte Carlo simulation was run with 1000 iterations where every transistor in the complete circuit (those used to implement the SCMs as well as the VFCM and the current mirrors) vary according to the

PDK statistical models.[13] Figure 18 shows a density histogram of I_{out} as well as a Kernel Density Estimation (KDE) for the output current's Probability Density Function (PDF).

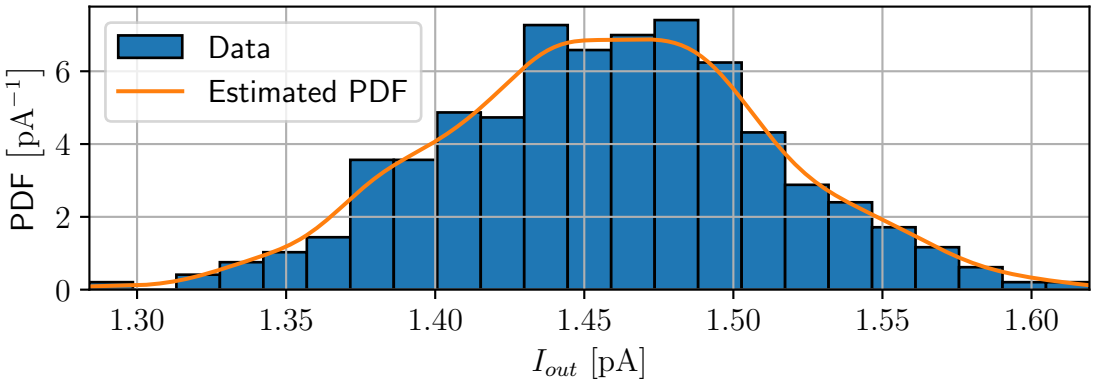


Figure 18 – Probability distribution of I_{out} due to component mismatch.

Due to the large number of transistors and iterations used, we expect the distribution to approximate a normal distribution, which is more-or-less what we see in the plots in fig. 18. The calculated mean was $\mu = 1.46\,\text{pA}$, consistent with the nominal simulations. The standard deviation was $\sigma = 55.3\,\text{fA}$, or in percentual terms, $\sigma/\mu = 3.79\,\%$. This relatively low value is due to the large matrices used, since the effect of mismatch is inversely proportional to the total area of each matrix [17]. Still, for a high-precision source, this value could be made smaller without using even more silicon surface.

One possible way of reducing this mismatch is having a post-fabrication trimming system. This could be done by using a current mirror with a controllable current ratio. One such mirror is the one presented in [18] that controls the ratio by biasing the body of the transistors. The disadvantage of this strategy in bulk CMOS nodes (which is the case for this project) is the need for a separate well to isolate the mirror's body terminals from the rest of the circuit. It would also need a way of controlling the body voltage in a way that is trimmable post fabrication. Another option is the digitally programmable mirror proposed in [19]. This strategy consists of switching certain current paths on and off to divert current to or from the output. While the proposed technique is to have a digital control system that switches those paths, a measurement post fabrication could determine the ideal digital inputs for a given fabricated circuit with it's mismatches and process variations and use laser trimming to permanently fix those digital pins to either ground or V_{dd}.

Another way of increasing the precision is by using a new technology. The technology used in this project was the now-discontinued 180 nm bulk CMOS node from TSMC, an old technology. To have a high precision current source, the circuit could be implemented on a newer technology such as the Fully Depleted Silicon On Insulator (FDSOI) process, known for it's extremely low component mismatch and process variations. Such technology would also bring other advantages. One of them is the free access to the body terminal of

individual transistors, making the implementation of the current mirror from [18] easier. More information relating to the FDSOI technology can be found in [20] and [21].

3.5 THE DESIGN SPACE

In this work, multiple choices were imposed for the design of the current source. Some of those choices are as follows:

- Choice of technological process;
- Choice of topology;
- Choice of initial conditions for i_{f2}, i_{f4} and α_{12};
- Choice of core reference I_X and current reducing stage ratio;

The set of final designs resulting from all combinations of all possible choices constitute the design space. Multiple points in the design space may respect the set specifications, each one posing different advantages and disadvantages. For example, if the the core reference I_X and reducing stage ratio were chosen as 100 pA and 100 : 1 instead of 20 pA and 20 : 1, the resulting output would still be around 1 pA but the core would have around 50 % less transistors, and thus less leakage current. The disadvantage is that the power consumption would be increased by about five times.

To achieve an optimal design, designers have to search the design space for points whose advantages align with their objectives. Due to time and practicality constraints, such exploration was not fully done in this work

4 FINAL CONSIDERATIONS

As was already mentioned multiple times, this work is divided into two main pillars: modelling and design.

Concerning the first one, this work achieved what it set out to do. The main versions of the ACM model have been presented in enough detail for usage during hand calculations and also implementation for simulation software (see notes 4 to 6). The extraction process for the utilised version was also presented as well as an automatic extraction tool (see appendix A). In the modelling aspect, the objectives were achieved.

Regarding the second pillar, the original objectives were also achieved, but this part left the possibility for further improvements of the design, having not started with concrete specifications for the thermal sensitivity and line regulation. While the achieved values are not terrible, the design process didn't even take those aspects into account. The circuit showed low susceptibility to mismatch and possible strategies to further reduce such susceptibility were presented.

All-in-all, all the objectives stated in section 1.2 ended up being achieved throughout the development of the work.

4.1 FUTURE WORKS

After the conclusion of this undergraduate thesis, multiple avenues of research present themselves as possible continuations of this work. A non-exhaustive list of such avenues is as follows:

- Application of the design methodology using a more advanced technology such as the 28 nm FDSOI node for reduced statistical dispersion;
- In-depth exploration of the dull design space;
- Further discussion of post-fabrication trimming techniques;
- Exploration of thermal sensitivity compensation techniques;
- Layouting of the developed current source.

NOTES

1 - To preserve the device's symmetry, both I_f and I_r depend on V_G in the same way and I_f depends in V_S in the same way that I_r depends in V_D. That is to say, if V_D and V_S are swapped, so are I_f and I_r. If stated mathematically, the same function $f(x, y)$ defines $I_f = f(V_G, V_S)$ and $I_r = f(V_G, V_D)$.

2 - To actually calculate the inversion levels using eq. (2.4), we need an expression for the inverse of eq. (2.6). This expression is shown in eq. (N.1).

$$F_i{}^{-1}(x) = \left[W_0\left(e^{x+1}\right) + 2\right] W_0\left(e^{x+1}\right) \tag{N.1}$$

where W_0 is the principal branch of the Lambert W function, a computationally tricky function to evaluate that raises concern for the use of the ACM model for simulation. Those concerns are addressed in [2] by using algorithm 443 [22], an algorithm that approximates $W_0(x)$ in a single iteration.

3 - Just like described in note 2, we need an expression for the inverse of eq. (2.11) to calculate the charge densities from eq. (2.10). This expression is shown in eq. (N.2).

$$F_q{}^{-1}(x) = W_0\left(e^{x+1}\right) \tag{N.2}$$

4 - Expressed as pseudo-code, the charge based formulation of the 3PM can be seen in algo. 1.

Algorithm 1 : I-V characteristics for the 3PM.

Function `DrainCurrent3PM(`V_G, V_S, V_D`):`

$V_P \leftarrow \frac{V_G - V_{T0}}{n}$
$X \leftarrow \exp\left(1 + \frac{V_P - V_S}{\phi_t}\right)$
$q_S \leftarrow W_0(X)$
$Y \leftarrow \exp\left(1 + \frac{V_P - V_D}{\phi_t}\right)$
$q_D \leftarrow W_0(Y)$
$I_D \leftarrow I_s \left(q_S + q_D + 2\right)\left(q_S - q_D\right)$
return I_D

5 - Expressed as pseudo-code, the 4PM can be seen in algo. 2.

Algorithm 2 : I-V characteristics for the 4PM.

Function `DrainCurrent4PM(`V_G, V_S, V_D`):`

$V_P \leftarrow \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}$
$X \leftarrow \exp\left(1 + \frac{V_P - V_S}{\phi_t}\right)$
$q_S \leftarrow W_0(X)$
$Y \leftarrow \exp\left(1 + \frac{V_P - V_D}{\phi_t}\right)$
$q_D \leftarrow W_0(Y)$
$I_D \leftarrow I_s \left(q_S + q_D + 2\right)\left(q_S - q_D\right)$
return I_D

6 - The presented model clearly treats the drain and the source differently, breaking the device's symmetry. To re-establish the symmetry, we can work with the terminal-agnostic q_1, q_2 and q_{sat}. q_S and q_D are equal to either q_1 or q_2 depending on whether V_D is greater than V_S. The pseudo-code that implements the 5PM with the re-established symmetry can be seen in algo. 3.

Algorithm 3 : I-V characteristics for the 5PM.

Function `DrainCurrent5PM(`V_G, V_S, V_D`):`

$V_X \leftarrow \min(V_S, V_D)$
$V_Y \leftarrow \mathrm{abs}(V_D - V_S)$
$V_P \leftarrow \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}$
$X \leftarrow \exp\left(1 + \frac{V_P - V_X}{\phi_t}\right)$
$q_1 \leftarrow W_0(X)$
$q_{sat} \leftarrow q_1 + 1 + \frac{1}{\zeta} - \sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_1}{\zeta}}$
$Y \leftarrow (q_1 - q_{sat}) \exp(q_1 - q_{sat}) \exp\left(-\frac{V_Y}{\phi_t}\right)$
$q_2 \leftarrow W_0(Y) + q_{sat}$
if $V_D \geq V_S$ **then**
  $q_S \leftarrow q_1$
  $q_D \leftarrow q_2$
else
  $q_S \leftarrow q_2$
  $q_D \leftarrow q_1$
$I_D \leftarrow I_s \left(q_S + q_D + 2\right)\left(q_S - q_D\right)$
return I_D

7 - Those dimensions are the extreme values allowed by the PDK. That is to say, the chosen dimensions were $W = W_{min} = 220\,\mathrm{nm}$ and $L = L_{max} = 19.995\,\mu\mathrm{m}$, resulting in an aspect ratio of $S_0 = S_{min} = 1.100\,28 \times 10^{-2}$. Those dimensions were chosen after trial and

error to achieve associations (shown in section 3.2.2) that do not have absurd numbers of transistors.

8 - Those values have to be different to guarantee that there's no more than one intersection point, but the reason they differ that much (3 orders of magnitude) is to reduce the design's sensitivity to variability on the values of components. We can see from fig. 5 that the slope of the curve increases with I_X and consequently, with the inversion level of the SCM. If both curves have the same slope at the intersection, they are tangent to each other and any small vertical shifts in any of the curves results in a huge change in the I_X value of the intersection point. If the slopes are drastically different, vertical shifts can change V_X but I_X remains mostly unaffected. Since we are interested in the current and not the voltage, this property is desirable.

9 - The drain current is proportional to the aspect ratio ($I_D \propto W/L$) while the gate current is proportional to the gate area ($I_G \propto WL$). Their ratio is, thus, proportional to the gate length squared ($I_G/I_D \propto L^2$).

10 - Something that has to be noted is that this "error" is a discrepancy between the ACM and the model used by TSMC's PDK. This discrepancy is sure to exist when compared to a real physical device, but no such measurements were carried out during the development of this work.

11 - The concept of average sensitivity is going to be used throughout the rest of the work, so it's worth precisely defining what is meant whenever this concept is invoked. Suppose we want to calculate the average sensitivity of a function $f(x)$ with respect to its independent variable $x \in (a, b)$. To do so, we need to analyse the local sensitivity defined in eq. (N.3).

$$\delta_f(x) = \frac{1}{f(x)} \frac{df(x)}{dx} = \frac{f'(x)}{f(x)} \tag{N.3}$$

Since we are interested in the average sensitivity, we need to calculate the average value of $\delta_f(x)$ on the domain $x \in (a, b)$. This calculation is done in eq. (N.4).

$$\overline{\delta_f} = \frac{1}{b-a} \int_a^b \delta_f(x)\, dx = \frac{1}{b-a} \int_a^b \frac{f'(x)}{f(x)}\, dx \tag{N.4}$$

If we adopt the substitution $u = f(x)$, we can solve the integral in eq. (N.4) and get a result that, when expressed as a percentage, becomes eq. (N.5).

$$\overline{\delta_f} = \frac{100\,\%}{b-a} \ln\left|\frac{f(b)}{f(a)}\right| \tag{N.5}$$

Whenever the concept of average sensitivity is invoked throughout the work, it is calculated according to eq. (N.5).

12 - The inversion levels were estimated by characterising every transistor using the methods described in section 2.2 and using the 3PM equations with the gate and source voltages at the nominal condition. In the case of transistor matrices, the model parameters where extracted by treating the entire matrix as an equivalent transistor.

13 - This simulation does not take process variations into account, only component mismatch.

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APPENDIX A – CHARACTERISATION AND DESIGN SCRIPTS

The following python script implements the extraction process described in section 2.2 using a `.csv` file with the needed measurement data.

```python
import numpy as np
from scipy.constants import elementary_charge as q
from scipy.constants import Boltzmann as kb
from vspc_tools import round_eng, round_fix  # available at https://github.com/victorscarpes/vspc_tools but only in portuguese, sorry for the non speakers ;p


def extractor_3pm(filename: str, W: float, L: float, T: float = 300) -> tuple[float, float, float, float]:
    phi_t = kb*T/q

    VG, ID = np.loadtxt(filename, delimiter=',', skiprows=1, unpack=True)

    ln_ID = np.log(ID)
    gm_ID = np.gradient(ln_ID, VG)
    gm_ID_max = np.max(gm_ID)
    theta = gm_ID/gm_ID_max
    Vt0_index = np.absolute(theta - 0.5310323912).argmin()
    Vt0 = VG[Vt0_index]
    Is = 1.13589136*ID[Vt0_index]
    Ish = Is*(L/W)

    Vg1 = Vt0/10
    Vg2 = Vt0/100
    dVg = Vg2 - Vg1

    Vg1_index = np.absolute(VG-Vg1).argmin()
    Vg2_index = np.absolute(VG-Vg2).argmin()

    n = (1/phi_t)*dVg/np.log(ID[Vg2_index]/ID[Vg1_index])

    return (Is, Ish, Vt0, n)


if __name__ == "__main__":
    ##############################################
    ############# INPUT PARAMETERS #############
    ##############################################

    # Define the path for the IDxVG curve used for extraction
    filename = "python/data/ish_extraction/IDxVG.csv"
```

```
40
41      # Define the gate width of the transistor under characterization (in meters)
42      W = 220e-9
43
44      # Define the gate length of the transistor under characterization (in meters)
45      L = 19.995e-6
46
47      # Define the characterization temperature (in Kelvin)
48      T = 300
49
50      # Define the number of significant digits for the printed output
51      precision = 5
52
53      ##############################################
54      ##############################################
55      ##############################################
56
57      Is, Ish, Vt0, n = extractor_3pm(filename=filename, W=W, L=L)
58      print(f"Is = {round_eng(Is, 'A', precision, '.')}")
59      print(f"Ish = {round_eng(Ish, 'A', precision, '.')}")
60      print(f"Vt0 = {round_eng(Vt0, 'V', precision, '.')}")
61      print(f"n = {round_fix(n, '', precision, '.')}")
```

By importing the previous script, the following script extracts the I_{sh} from the unit transistor and uses it with the equations presented in section 3.2.1 to calculate all the design parameters for the SBCS core. It then calculates the needed associations of the unit transistor shown in section 3.2.2.

```
1  from scipy.special import lambertw as W0
2  import numpy as np
3  from vspc_tools import round_fix, round_sci, round_eng  # available at
   ↪ https://github.com/victorscarpes/vspc_tools but only in portuguese, sorry for the
   ↪ non speakers ;p
4  from scipy.constants import elementary_charge as q
5  from scipy.constants import Boltzmann as kb
6  from extractor import extractor_3pm
7
8  ##############################################
9  ############## INPUT PARAMETERS ##############
10 ##############################################
11
12
13 # Define the path for the IDxVG curve used for extraction
14 filename = 'python/data/ish_extraction/IDxVG.csv'
15
16 # Define the operating temperature (in Kelvin)
17 T = 300
```

```
18
19  # Define the desired core's current (in amperes)
20  I_X = 20e-12
21
22  # Define the inversion level of SCM_12
23  i_f2 = 10
24
25  # Define the inversion level of SCM_34
26  i_f4 = 0.01
27
28  # Define the inversion level ratio for SCM_12
29  alpha_12 = 2
30
31  # Define the gate width of the transistor under characterization (in meters)
32  W = 220e-9
33
34  # Define the gate length of the transistor under characterization (in meters)
35  L = 19.995e-6
36
37  # Define the number of significant digits for the printed output
38  precision = 5
39
40  ##############################################
41  ##############################################
42  ##############################################
43
44
45  def ratio_sorter(S1: float,
46                   S2: float,
47                   S3: float,
48                   S4: float,
49                   L: float,
50                   W: float,
51                   max_term: int = 1000,
52                   max_list: int = 4):
53
54      ratio_list_s1 = []
55      ratio_list_s2 = []
56      ratio_list_s3 = []
57      ratio_list_s4 = []
58
59      S0 = W/L
60
61      for m in range(1, max_term+1):
62          for n in range(1, max_term+1):
63
64              area = n * m
```

```
            value = (n/m)*S0

            error_s1 = 100*abs((S1-value)/S1)
            error_s2 = 100*abs((S2-value)/S2)
            error_s3 = 100*abs((S3-value)/S3)
            error_s4 = 100*abs((S4-value)/S4)

            if area <= max_term:
                ratio_list_s1.append((error_s1, area, value, n, m))
                ratio_list_s2.append((error_s2, area, value, n, m))
                ratio_list_s3.append((error_s3, area, value, n, m))
                ratio_list_s4.append((error_s4, area, value, n, m))

    ratio_list_s1.sort()
    ratio_list_s2.sort()
    ratio_list_s3.sort()
    ratio_list_s4.sort()

    ratio_list_s1 = ratio_list_s1[:max_list]
    ratio_list_s2 = ratio_list_s2[:max_list]
    ratio_list_s3 = ratio_list_s3[:max_list]
    ratio_list_s4 = ratio_list_s4[:max_list]

    line_spacer = "×"+20*"-"+"×"+20*"-"+"×"+20*"-"+"×"+20*"-"+"×"+20*"-"+"×"

    print("Possible arrays for M1:")
    print(line_spacer)
    print(f"|{'Value':^20}|{'Error (%)':^20}|{'# of
    ↪  transistors':^20}|{'m':^20}|{'n':^20}|")
    for error, area, value, n, m in ratio_list_s1:
        print(line_spacer)
        print(f"|{np.format_float_scientific(value,
        ↪  10):^20}|{np.format_float_positional(error,
        ↪  10):^20}|{area:^20}|{m:^20}|{n:^20}|")
    print(line_spacer)

    print("\nPossible arrays for M2:")
    print(line_spacer)
    print(f"|{'Value':^20}|{'Error (%)':^20}|{'# of
    ↪  transistors':^20}|{'m':^20}|{'n':^20}|")
    for error, area, value, n, m in ratio_list_s2:
        print(line_spacer)
        print(f"|{np.format_float_scientific(value,
        ↪  10):^20}|{np.format_float_positional(error,
        ↪  10):^20}|{area:^20}|{m:^20}|{n:^20}|")
    print(line_spacer)

```

```
106     print("\nPossible arrays for M3:")
107     print(line_spacer)
108     print(f"|{'Value':^20}|{'Error (%)':^20}|{'# of
        ↪  transistors':^20}|{'m':^20}|{'n':^20}|")
109     for error, area, value, n, m in ratio_list_s3:
110         print(line_spacer)
111         print(f"|{np.format_float_scientific(value,
            ↪  10):^20}|{np.format_float_positional(error,
            ↪  10):^20}|{area:^20}|{m:^20}|{n:^20}|")
112     print(line_spacer)
113 
114     print("\nPossible arrays for M4:")
115     print(line_spacer)
116     print(f"|{'Value':^20}|{'Error (%)':^20}|{'# of
        ↪  transistors':^20}|{'m':^20}|{'n':^20}|")
117     for error, area, value, n, m in ratio_list_s4:
118         print(line_spacer)
119         print(f"|{np.format_float_scientific(value,
            ↪  10):^20}|{np.format_float_positional(error,
            ↪  10):^20}|{area:^20}|{m:^20}|{n:^20}|")
120     print(line_spacer)
121 
122 
123 phi_t = kb*T/q
124 
125 I_S, I_SH, Vt0, n = extractor_3pm(filename=filename, W=W, L=L, T=T)
126 
127 
128 def Fi(x):
129     return np.sqrt(1+x)-2+np.log(np.sqrt(1+x)-1)
130 
131 
132 def Fi_inv(x):
133     return (W0(np.exp(x+1))*(W0(np.exp(x+1))+2)).real
134 
135 
136 S_2 = (I_X)/(I_SH*i_f2)
137 S_1 = (S_2*2)/(alpha_12-1)
138 
139 V_x = phi_t*(Fi(alpha_12*i_f2)-Fi(i_f2))
140 
141 alpha_34 = Fi_inv(V_x/phi_t + Fi(i_f4))/i_f4
142 
143 S_4 = (I_X)/(I_SH*i_f4)
144 S_3 = (S_4*2)/(alpha_34-1)
145 
146 i_f3 = alpha_34*i_f4
```

```
147 i_f1 = alpha_12*i_f2
148
149 if __name__ == "__main__":
150     print("Inversion levels of the associations")
151     print(f"if1 = {round_fix(i_f1, '', precision, '.')}")
152     print(f"if2 = {round_fix(i_f2, '', precision, '.')}")
153     print(f"if3 = {round_fix(i_f3, '', precision, '.')}")
154     print(f"if4 = {round_fix(i_f4, '', precision, '.')}\n")
155
156     print("SCMs' inversion level ratios")
157     print(f"alpha_12 = {round_fix(alpha_12, '', precision, '.')}")
158     print(f"alpha_34 = {round_fix(alpha_34, '', precision, '.')}\n")
159
160     print("Aspect ratios")
161     print(f"S1 = {round_sci(S_1, '', precision, '.')}")
162     print(f"S2 = {round_sci(S_2, '', precision, '.')}")
163     print(f"S3 = {round_sci(S_3, '', precision, '.')}")
164     print(f"S4 = {round_sci(S_4, '', precision, '.')}\n")
165
166     print("Volage at node X")
167     print(f"Vx = {round_eng(V_x, 'V', precision, '.')}\n")
168
169     ratio_sorter(S_1, S_2, S_3, S_4, L, W)
```