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Ícaro de Almeida Albuquerque

DESIGN OF A THREE-PHASE T-TYPE INTERLEAVED CONVERTER

Florianópolis
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Ícaro de Almeida Albuquerque

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Dissertação submetida ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina para a obtenção do título de Mestre em Engenharia Elétrica
Supervisor: Prof. Telles Brunelli Lazzarin, Dr.
Co-supervisor: Prof. Gierri Waltrich, Dr.

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O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Prof. Joabel Moia, Dr.
Instituto Federal de Santa Catarina

Eng. Julio Cesar Dias, Dr.
Universidade Federal de Santa Catarina

Prof[a]. Jéssika Melo de Andrade, Dra.
Universidade Federal de Santa Catarina

Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de Mestre em Engenharia Elétrica.

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Prof. Telles Brunelli Lazzarin, Dr.
Orientador

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Prof. Telles Brunelli Lazzarin, Dr.
Coordenador do Programa

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Maio de 2024.

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"Não há limite para a técnica. Há sempre espaço para melhorias."
Yagyu Sekishusai

Resumo

O presente trabalho propõe o conversor trifásico *T-Type* intercalado (*interleaved*) empregando transformadores de interfase como uma solução para aplicações de conversores CC-CA bidirecionais, tais como em microrredes ou em carregadores de veículos elétricos. Nesse sentido, primeiramente é realizada uma análise matemática detalhada do conversor de modo a caracterizá-lo para um número qualquer de módulos em paralelo. Realiza-se a descrição de um método numérico para obtenção das formas de onda comutadas das correntes de modo comum e de circulação entre os módulos, que é validada por meio de *software* de simulação. Em relação ao projeto do conversor, uma metodologia visando otimização é proposta com o objetivo de reduzir as perdas nos dispositivos semicondutores e nos elementos magnéticos. A rotina de otimização é baseada no algoritmo Enxame de Partículas (PSO, do inglês *Particle Swarm Optimization*) e retorna as variáveis construtivas dos magnéticos para uma dada condição de operação. Portanto, para uma aplicação de 10 kW em uma rede trifásica a três fios de 220 V / 60 Hz, o algoritmo proposto foi aplicado e os magnéticos resultantes foram construídos e avaliados através de testes experimentais. A eficiência do conversor foi verificada experimentalmente para diferentes estratégias de modulação, obtendo 98% de eficiência em toda faixa de operação nominal. Em se tratando do controle, um modelo dinâmico médio é proposto para o conversor considerando as dinâmicas do laço de travamento de fase (PLL, do inglês *Phase-Locked Loop*), o qual foi baseado no PLL de eixo de referência síncrono (SRF-PLL), e das demais malhas de controle, perfazendo um modelo em malha fechada completo do conversor. Tal modelo foi utilizado para ajuste do controle e avaliação preliminar de estabilidade. A validação das estratégias de controle propostas foi realizada através de *software* de simulação. As análises realizadas apontam que o conversor trifásico *T-Type interleaved* é capaz de prover características de conversores multiníveis utilizando módulos de três níveis aplicando a técnica de intercalamento, de modo a apresentar alta eficiência e potencial para projetos compactos.

Palavras-chave: Conversor CA-CC bidirecional; *T-Type interleaved*; Projeto otimizado; Modelo dinâmico médio em malha fechada; Estratégias de modulação.

Abstract

This work proposes a three-phase T-Type interleaved converter employing interphase transformers as a solution for applications requiring bidirectional AC-DC converters, such as microgrids and electric vehicle chargers. In this scenario, the converter is analytically characterized for any number of interleaved modules. The analysis introduces a numerical model to assess the converter's switched common mode and circulating currents, which is validated through comparison with simulation software. Regarding the design of the converter, an optimal method is proposed to minimize losses in switching devices and magnetic elements. The algorithm is based on Particle Swarm Optimization (PSO) and returns the constructive parameters of the magnetic elements for a given operational condition. Therefore, for an application of 10 kW in a 220 V / 60 Hz mains, the proposed method was employed, and the resulting magnetic elements were built and validated through experimental testing. The converter's efficiency was evaluated for different modulation schemes, obtaining 98% efficiency over the rated power range. Concerning the control strategy, an average dynamic model was proposed, considering the dynamics of the Phase-Locked Loop (PLL) based on the SRF-PLL, and all proposed control loops, resulting in a complete closed-loop model of the converter. The model was utilized for controller tuning and preliminary assessment of the converter's stability. The proposed control strategy's validation was performed in simulation software. The analysis of the T-Type interleaved converter concludes that this converter can feature multilevel characteristics by employing the interleaving of three-level modules, resulting in high efficiency and potentially compact designs.

Key-words: Bidirectional AC-DC converter; T-Type interleaved; Optimal design; Average dynamic closed-loop model; Modulation strategies.

Resumo Expandido

Introdução

Desde o final do século XX, desafios significativos, como a crescente preocupação ambiental, a redução da dependência de combustíveis fósseis e a necessidade de diversificar a matriz energética através da integração de fontes de energia renováveis têm estado em pauta e motivam soluções inovadoras. Nesse contexto, tecnologias emergentes como microrredes e veículos elétricos têm se destacado como focos de pesquisa, visando proporcionar flexibilidade, confiabilidade e eficiência na conversão de energia dentro do sistema elétrico. No entanto, a implementação dessas tecnologias exige uma infraestrutura específica para sua integração ao sistema elétrico existente. Nesse sentido, conversores bidirecionais CA-CC são fundamentais para garantir a interface necessária a essa integração.

A literatura apresenta diversas soluções para conversores trifásicos CA-CC bidirecionais que atendem às demandas apresentadas, como o conversor de dois níveis, o *Active Neutral Point Clamped* (ANPC) e o *T-Type*. Devido às limitações tecnológicas dos semicondutores, para aumentar o nível de potência desses conversores, são propostas algumas alternativas na literatura, como o uso de semicondutores em paralelo ou o paralelismo de conversores. No caso do paralelismo de conversores, pode-se empregar a defasagem dos sinais de comutação entre os módulos, conhecida como técnica de intercalamento (*interleaving*). Os principais benefícios do intercalamento incluem o cancelamento de harmônicos, o que permite a redução do volume dos elementos passivos nos filtros.

Portanto, a aplicação da técnica de intercalamento a um conversor CA-CC bidirecional pode melhorar significativamente o desempenho do conversor, reduzindo a necessidade de filtros volumosos devido ao aumento do número de níveis de tensão, além de permitir um aumento do nível de potência do sistema. Dessa forma, o presente trabalho se dedica ao estudo da aplicação da técnica de intercalamento ao conversor trifásico *T-Type*, propondo uma metodologia de projeto do filtro e uma estratégia de controle adequada.

Objetivos

O objetivo principal do presente trabalho é apresentar um estudo exploratório do conversor *T-Type* intercalado. A análise do conversor é realizada de forma generalizada para um número qualquer de módulos intercalados com o intuito de avaliar o efeito deste parâmetro na performance do conversor. Os objetivos específicos deste trabalho são:

- Realizar a análise estática do conversor *T-Type* intercalado;
- Desenvolver uma metodologia de projeto ótimo em eficiência dos elementos passivos do filtro;
- Desenvolver uma estratégia de controle apropriada para o conversor proposto;
- Avaliar o efeito de diferentes modulações na eficiência do conversor *T-Type* interleaved.

Metodologia

A pesquisa focou-se na análise detalhada do conversor proposto, com o objetivo de derivar equações analíticas que descrevessem seu funcionamento. Em seguida, desenvolveu-se um algoritmo para simulação numérica do conversor, aplicável a um conjunto qualquer de parâmetros. O modelo comutado proposto foi então utilizado na metodologia de projeto ótimo do conversor, baseada no desenvolvimento de um modelo de perdas e na minimização dessas perdas por meio de um algoritmo de enxame de partículas (PSO).

Para o modelo dedicado ao controle do conversor, partiu-se das equações derivadas da análise estática do dispositivo, utilizando o operador de valor médio quase instantâneo para criar um modelo médio do conversor. Os controladores foram integrados ao modelo, permitindo a simulação das variáveis de estado médias do conversor. O modelo em malha fechada foi empregado como uma ferramenta de análise dinâmica no projeto dos controladores adequados.

Finalmente, montou-se um protótipo de 10 kW do conversor para validar as análises propostas. As modulações consideradas para o conversor foram testadas em toda a faixa de potência, a fim de obter uma curva de eficiência para cada modulação.

Resultados e Discussão

O modelo de perdas proposto mostrou-se coerente com os resultados experimentais obtidos para todas as modulações estudadas, havendo apenas uma perda de fidelidade abaixo de 40% de carga. Toda as modulações estudadas apresentaram uma eficiência acima de 98% na faixa de potência avaliada. Além disso, o modelo térmico empregado apresentou alta fidelidade para o indutor acoplado de núcleo toroidal mas muito baixa performance ao avaliar a temperatura dos transformadores de interfase. Em relação ao controle, as simulações realizadas em *software* de simulação apresentaram resultados satisfatórios para diferentes modos de operação, de modo a validar a estratégia proposta.

Considerações Finais

Haja vista os resultados obtidos, considera-se que os objetivos propostos foram logrados. No entanto, diante da análise crítica dos resultados, evidencia-se a possibilidade de melhora. Nesse sentido, são sugeridos os seguintes trabalhos futuros:

- Desenvolver um modelo de perdas para os semicondutores e elementos magnéticos mais preciso para maior fidelidade com os resultados experimentais;
- Projetar um filtro de EMI para cumprimento das normas relacionadas;
- Implementar um modelo de perdas adequado ao núcleo E;
- Implementar uma técnica de modelagem capaz de retirar a variação temporal do modelo sem truncar seu comportamento dinâmico com o intuito de avaliar a estabilidade do conversor;
- Estudar e implementar uma estratégia de anti-ilhamento, a qual é obrigatória em aplicações conectadas à rede;
- Validar a estratégia de controle proposta experimentalmente.

Palavras-chave: Conversor CA-CC bidirecional; *T-Type interleaved*; Projeto otimizado; Modelo dinâmico médio em malha fechada; Estratégias de modulação.

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List of abbreviations and acronyms

AC	Alternating Current
ANPC	Active Neutral Point Clamped
AWG	American Wire Gauge
BESS	Battery Energy Storage System
CHB	Cascaded H-Bridge
DC	Direct Current
DPWM	Discontinuous Pulse Width Modulation
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
G2V	Grid-To-Vehicle
GSE	Generalized Steinmetz Equation
HUT	Hold-Up Time
IEA	International Energy Agency
IT	Interphase Transformer
iGSE	Improved Generalized Steinmetz Equation
i^2GSE	Improved Improved Generalized Steinmetz Equation
MAFSRF-PLL	Moving Average Filter Synchronous Reference Frame Phase-Locked Loop
MMC	Modular Multilevel Converter

PCC	Point of Common Coupling
PD-PWM	Phase Disposition Pulse Width Modulation
PCB	Printed Circuit Board
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse Width Modulation
PI	Proportional-Integral
PLL	Phase-Locked Loop
PSO	Particle Swarm Optimization
rms	Root Mean Square
SCR	Short Circuit Ratio
SMES	Superconducting Magnetic Energy Storage
SPWM	Sinusoidal Pulse Width Modulation
SST	Solid-State Transformer
SVM	Space Vector Modulation
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
STHI	Sinusoidal Third Harmonic Injection
V2G	Vehicle-To-Grid
VSI	Voltage Source Inverter

List of symbols

n	Number of interleaved modules
C_b	DC-link capacitance
$S_{xj,i}$	Switching device with $x \in \{a, b, c\}$, $j \in \{1, 2, 3, 4\}$ and $i \in \{1, \ldots, n\}$
$v_{i,xo}$	Terminal voltage of a switching module with $i \in \{1, \ldots, n\}$
φ	Angle shift between adjacent carriers in a interleaved converter
T_x	Interphase transformer with $x \in \{a, b, c\}$
i_p	Current in the upper branch of the DC-link
i_o	Current in the central branch of the DC-link
i_n	Current in the lower branch of the DC-link
v_{dck}	Voltage of DC-link capacitor with $k \in \{1, 2\}$
i_{dc}	Load current
P_r	Rated power of the DC-link power source
x_i	Treminal of phase branch with $x \in \{a, b, c\}$ and $i \in \{1, \ldots, n\}$
L_m	Mains series inductance
R_m	Mains series resistance
i_p	Current in the upper branch of the DC-link
$v_{i,x}$	Voltage across the i-th winding of T_x, with $x \in \{a, b, c\}$ and $i \in \{1, \ldots, n\}$
$\mathbf{v}_{n,x}$	Voltage vector of $v_{i,x}$
$i_{i,x}$	Current across the i-th winding of T_x, with $x \in \{a, b, c\}$ and $i \in \{1, \ldots, n\}$
$\mathbf{i}_{n,x}$	Current vector of $i_{i,x}$
L_{ij}	Mutual inductances in T_x between the i-th and j-th windings
$\mathbf{L}_w$	Mutual inductances matrix of any T_x

r_w	Equivalent series resistance of each winding in T_x
$\mathbf{R}_w$	Equivalent series resistance of any T_x
D_t	Differential operator over time, defined as $D_t : SC(\mathbb{R}) \to C^\infty(\mathbb{R})$, where $SC(\mathbb{R}) = \{f : \mathbb{R} \to \mathbb{R};\ f \text{ is continuous except in a finite group}\}$, which translates to $D_t f(t) = f'(t)$
$\mathbf{T}_L$	Lunze's Transformation matrix
$\mathbf{y}_{sm,am,x}$	Vector of subtractive and additive mode components in phase x
$\mathbf{L}_{sm}$	Subtractive mode equivalent matrix of any T_x
L_{sm}	Equivalent subtractive inductance of any T_x
L_{am}	Equivalent additive inductance of any T_x
v_{xo}	Terminal voltage of T_x with respect of the DC-link central point o
v_x	Mains phase voltage with $x \in \{a, b, c\}$
V_p	Mains phase voltage peak value
θ_x	Angle of mains voltage with $x \in \{a, b, c\}$
v_{cm}	Common mode voltage of the converter
L_b	Boost inductor
$m_{i,x}$	Modulation signal with $x \in \{a, b, c\}$ and $i \in \{1, \ldots, n\}$
$\theta(x)$	Saturation function defined in Equation 2.15
$\overline{\theta}(x)$	Logical inverse of $\theta(x)$
M_T	Dynamic average value operator $M_T : SC(\mathbb{R}) \to C^\infty(\mathbb{R})$
v_{dc}	DC-link voltage
Δv_{dc}	DC-link unbalance voltage
ϕ	Phase shift between mains voltage and converter output voltage
M	Modulation index
$\mathbf{T}_{dm}$	Differential mode transformation matrix
L_s	Self inductance of T_x
$n_{lvl,max}$	Maximum level count of a T-Type interleaved converter
$n_{lvl,ef}$	Effective level count of a T-Type interleaved converter
v_{lvl}	Voltage at a given level in the converter output
i_{C1}	Current at the top DC-link capacitor

i_{C2}	Current at the bottom DC-link capacitor
$C_{b,min}$	Minimum DC-link capacitance
$V_{dc,min}$	Minimum DC-link voltage
Δt	Discharge time for DC-link capacitance calculation using hold-up time
$m_{cm,svm}$	Common mode component in the SVM modulation scheme
$m_{cm,sthi}$	Common mode component in the STHI modulation scheme
$m_{cm,dpwm}$	Common mode component in the DPWM modulation scheme
V_{rms}	Rms value of the mains phase voltage
f_m	Mains frequency
f_s	Switching frequency
$N_{t,Lb}$	Number of turns in a boost inductor winding
A_L	Inverse of the reluctance of a iron powder toroidal core
$H_{max,Lb}$	Maximum magnetic field allowed in the boost inductor
l_c	Magnetic path length
J_w	Current density
n_p	Number of paralleled wires
A_w	Cross section area of a wire
k_w	Utilization factor
W_c	Window area of the core
$\mathfrak{R}$	Reluctance
g	Air gap length
μ_0	Vacuum magnetic permeability and $\mu_0 = 4\pi.10^{-7}$ N.A^{-2}
μ_r	Relative magnetic permeability
μ_{eff}	Effective magnetic permeability
$N_{t,Ls}$	Number of turns in a winding o T_x
$B_{max,Ls}$	Maximum magnetic flux density
n_l	number of layer in winding
r_{awg}	Radius of a given AWG wire
w_h	Window height in double E core

P_c	Conduction losses in switching device
$R_{ds,on}$	Drain-source resistance of semiconductor device during on state
$I_{s,rms}$	Rms value of drain-source current of semiconductor device
i_{Sxj}	Current in semiconductor device with $x \in \{a, b, c\}$ and $j \in \{1, 2, 3, 4\}$
$i_{Sxj,sw,on}$	Current in semiconductor device with $x \in \{a, b, c\}$ and $j \in \{1, 2, 3, 4\}$ in the off-to-on state transition
$i_{Sxj,sw,off}$	Current in semiconductor device with $x \in \{a, b, c\}$ and $j \in \{1, 2, 3, 4\}$ in the on-to-off state transition
$E_{on,total}$	Total energy spent in the on state
$E_{off,total}$	Total energy spent in the off state
P_skin	Power losses due to skin effect
$F_r(f)$	Ratio between AC and DC resistance for a frequency f
R_{dc}	DC resistance of wire
ξ	Effective wire diameter due to skin effect
R_w	Thermal resistance between copper windings and copper coil surface
$R_{cw,cd}$	Thermal resistance between winding and core through conduction
$R_{cw,r}$	Thermal resistance between winding and core through radiation
$R_{wa,cv}$	Thermal resistance between winding and ambient through convection
$R_{wa,r}$	Thermal resistance between winding and ambient through radiation
$R_{ca,cv}$	Thermal resistance between core and ambient through convection
$R_{ca,r}$	Thermal resistance between core and ambient through radiation
T_w	Temperature of the winding
T_c	Temperature of the core
T_∞	Room temperature
C_1	Filter capacitance
C_2	Damping branch capacitance
R_d	Damping branch resistance
L_1	Equivalent boost inductance
f_{res}	Resonance frequency of the filter
$\mathbf{T}_P$	Park's Transformation matrix

Contents

Chapter

1 Introduction

The 20th century saw significant technological advancements that reshaped society. Notably, Power Electronics emerged as a field aimed at refining power processing methods and advancing process electrification [1]. The rapid advancement in Power Electronics is closely linked to the swift development of semiconductor devices, which form the foundation of this field. Additionally, the progress in control theories, integrated circuits, sensors, and passive components further accelerated the rise of Power Electronics.

The challenges faced by a field of study often drive innovative solutions. In the case of Power Electronics, initial demands were focused on industrial applications, particularly electric motors and their drives [1, 2, 3]. However, since the late 20th century, growing concerns about climate change and the need to reduce dependence on fossil fuels have entailed the diversification of energy sources [4]. Consequently, the integration of renewable power sources such as solar and wind into the existing grid has presented new challenges for Power Electronics, specifically in providing efficient power interfaces between these energy sources and the existing grid.

In this context, the widespread integration of distributed renewable power sources into the grid has introduced the concept of microgrids. These are hybrid networks connected to the grid, consisting of renewable power sources and Energy Storage Systems (ESS). Their purpose is to enhance the reliability of power services in the event of faults by operating independently, known as islanded mode, ensuring uninterrupted energy transfer from local power sources to local loads [5].

Due to the dependency of microgrid power generation on renewable energy sources, the instantaneous power generated lacks precise control. This type of energy sources are non-dispatchable, meaning that their output fluctuates due to weather intermittency, making it challenging to match the fluctuations on power demand [6]. Consequently, the integration of ESS within microgrids becomes indispensable. These systems facilitate seamless transitions between grid-connected and islanded modes and enhance dynamic response during load connection and disconnection events [7]. Examples of ESS include batteries, supercapacitors, flywheels, and superconducting magnetic energy storage (SMES)

[8].

Microgrids can be classified based on the arrangement of AC and DC buses. Six architectures have been identified and thoroughly discussed in [6]: AC-microgrid, DC-microgrid, hybrid AC-DC microgrid, AC-microgrid with DC storage, DC-zonal microgrid, and solid-state transformer (SST) based microgrid. Figure 1.1 illustrates the first three and primary architectures of microgrids in relation to the main grid and the point of common coupling (PCC) [6].

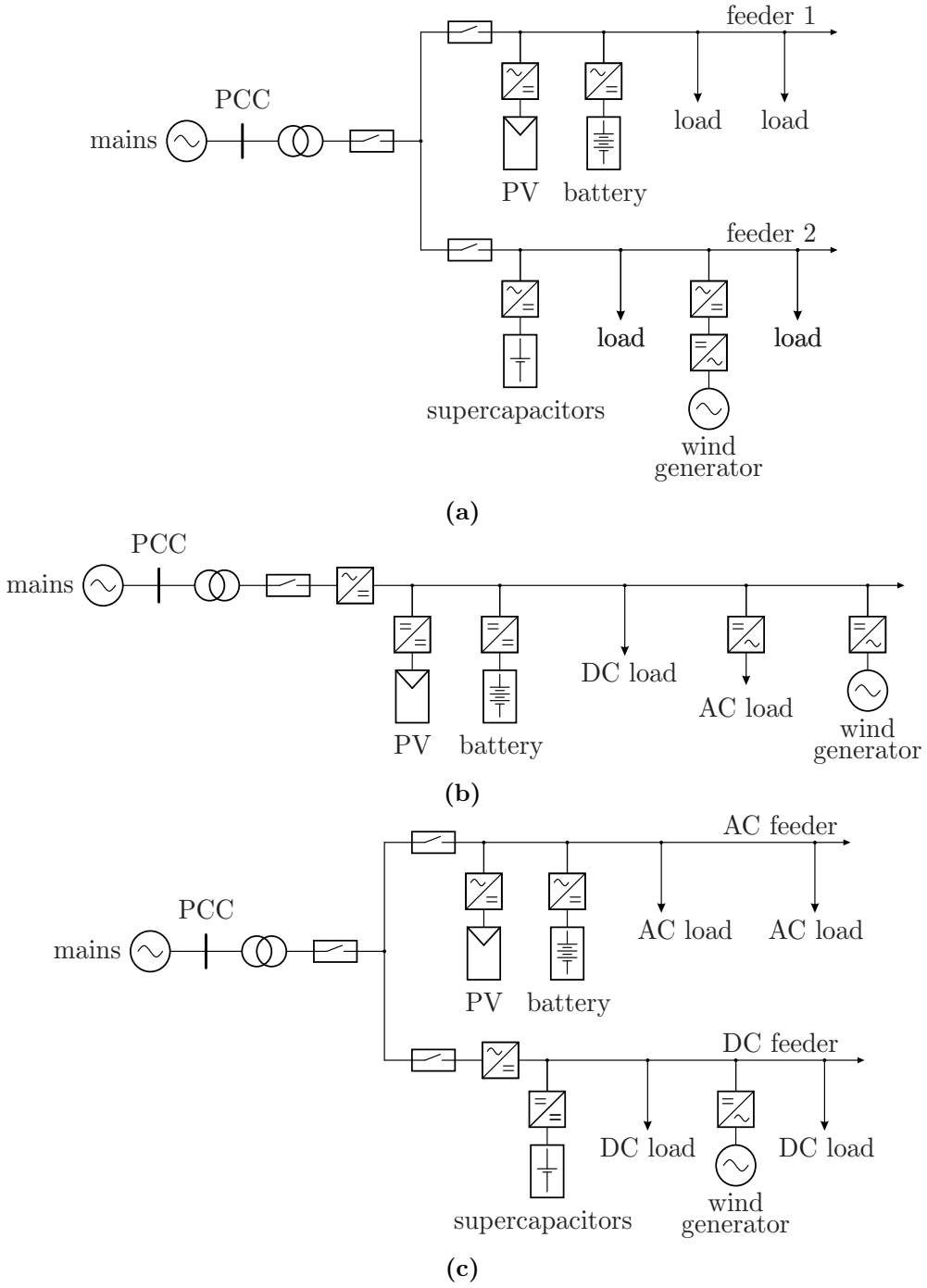


Figure 1.1 – Diagram of AC microgrid (a), DC microgrid (b) and hybrid AC-DC microgrid (c).

Source: Adapted from [6].

Nowadays, the electrification of the transportation sector is the major challenge imposed to the Power Electronics, driven by the growing accessibility of hybrid and electric vehicles (EV). This trend created the demand for specialized converters dedicated to battery recharging. These converters can be integrated within the vehicle, constituting the on-board charger, or located externally at off-board charging stations [9].

Conventionally, EV charging operated only in a unidirectional mode, with the grid supplying energy to the EV battery and the reverse operation was not possible due to charger characteristics. This operation mode is defined in literature as Grid-To-Vehicle (G2V). However, this approach of charging could lead to uncoordinated power flow in the grid, which could cause fluctuations and concentrate power demands at specific times, specially in the evening [10]. The International Energy Agency (IEA) predicted that the demand for EV charging by 2030 can reach approximately 1000 TWh, primarily driven by the Chinese, American, European, Indian, and Japanese markets [11]. In response to this scenario and considering the substantial idle time of vehicles in urban areas, there has been exploration of utilizing the extensive battery reserves of EVs for secondary applications, particularly during grid-connected periods [12].

In this context, integrating EVs into the grid as a virtual power plant holds potential for stabilizing electrical energy demand. This localized form of compensation mitigates stress on transmission lines from the grid's perspective and enhances the overall efficiency of electrical service. Considering the dispatchable nature of EV batteries, optimal utilization can occur during critical moments to mitigate peak demand through a process known as peak-shaving. This concept of using the EV to provide energy to the grid is defined as Vehicle-To-Grid (V2G). The integration of the EVs as power sources is categorized accordingly to the dependency of the grid and application as: stand-alone, grid-connected, transition and grid-supported; which are discussed in detail in [12].

Residential charging of electric vehicles (EVs) necessitates on-board chargers capable of direct connection to the AC bus in any home. As a result, these converters are typically limited in rated power to a range of 11-21 kW. Due to this power limitation, on-board chargers are classified as slow chargers. Conversely, off-board chargers, designed for fast charging, are rated at much higher power levels ranging from 21-400 kW. Fast charging requires direct access to the EV battery pack and is typically facilitated at charging stations known as clusters or aggregators [12, 13]. Figure 1.2 illustrates the differences between on-board and off-board charging modes, specifying the connection from a home outlet to the on-board charger before the battery ESS (BESS) and the direct connection to the BESS in the off-board charging mode.

The integration of the concepts of microgrids and EVs as power sources is significantly influenced by regulatory standards, which establish essential requirements for products to enter the market. However, due to the volatile nature of grid infrastructure across different regions, parameters such as voltage level, frequency, and communication

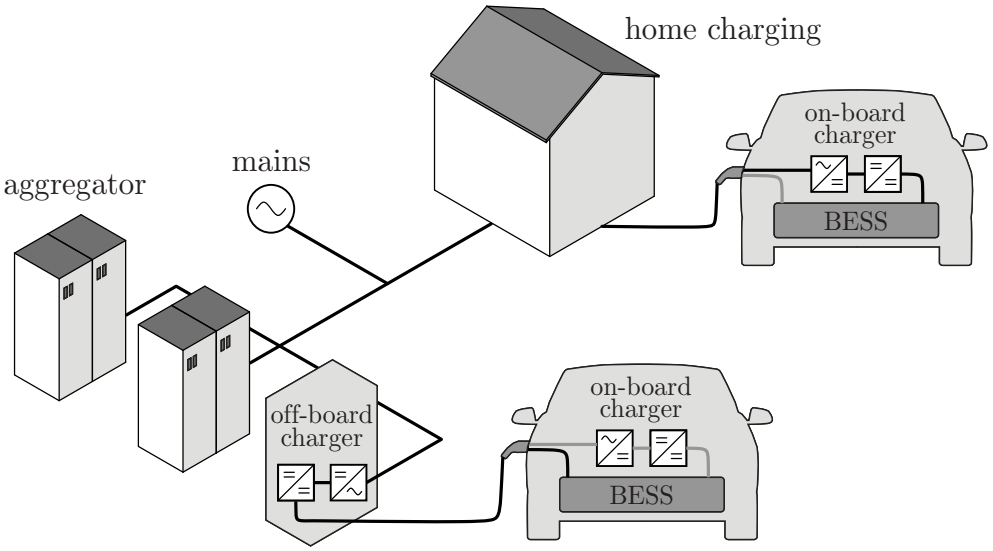


Figure 1.2 – Comparison between on-board and off-board charging of EVs.

Source: Adapted from [13].

protocols vary, resulting in a heterogeneous standards environment. Consequently, finding a universal solution to implementation challenges becomes impractical. On the hardware side, however, the successful deployment of microgrids and V2G systems relies mostly on the availability of efficient and reliable power electronics converters capable of bidirectional power flow. In this regard, the present work is focused on the analysis of a solution for the bidirectional three-phase AC-DC converter.

A wide variety of topologies are available for bidirectional power flow, as illustrated in Figure 1.3. However, this work focuses exclusively on the voltage source category, and therefore, the exploration of other converter categories is beyond the scope of this study.

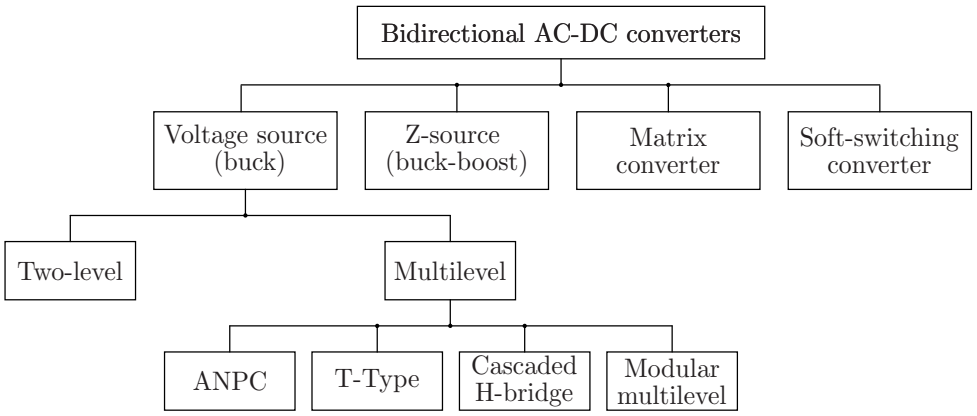


Figure 1.3 – Comparison betwenn on-board and off-board charging of EVs.

Source: Adapted from [14].

In this context, the prevalent choice for most applications is the two-level voltage source inverter (VSI), also known as B6, due its simplicity and reliability. With only six semiconductor devices, this topology proves to be cost-effective. However, drawbacks arise

from limitations in grid and DC-link voltage. During operation stages, semiconductors are required to block the entire DC-link voltage. Additionally, managing the differential and common mode voltages in the AC-side require bulky filters to comply with Electromagnetic Compatibility (EMC) standards [14]. The two-level VSI is illustrated in Figure 1.4a.

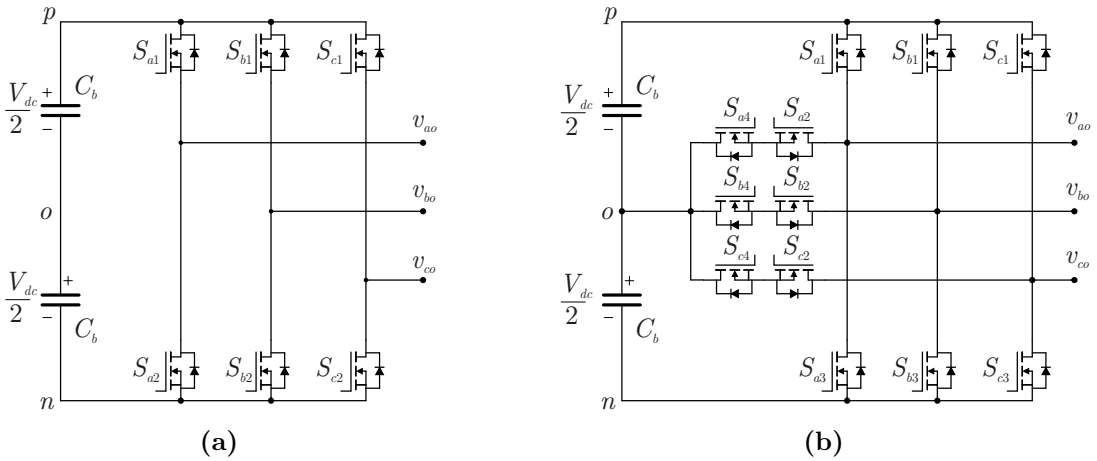


Figure 1.4 – Two-level voltage source (a) and T-Type (b).

To address the limitations of the two-level VSI, multilevel topologies have been developed. Illustrated in Figure 1.4b, the T-Type converter, a bidirectional variation of the Vienna rectifier proposed in [15], exemplifies a three-level VSI. This topology builds upon the two-level VSI by integrating bidirectional switches that connect the output phase to the central point of the DC-link. The increased number of levels enhances the profiles of both differential and common mode voltage, allowing for the utilization of smaller filters on the AC side. However, a limitation of this topology is its voltage rating, which remains constrained by the structure of the two-level VSI [16, 17].

In higher voltage applications, stackable topologies are employed to distribute voltage stress among semiconductor devices. Examples of such converters are depicted in Figure 1.5, including the Active Neutral Point Clamped (ANPC), which originates from the substitution of diodes for active switching devices in the conventional NPC, the Cascaded H-Bridge (CHB), and Modular Multilevel Converter (MMC). These converters, designed for higher voltage ratings, significantly reduce total harmonic distortion (THD) in both voltage and current on the AC side compared to other topologies, thereby requiring the use of smaller filters. However, challenges arise in implementing complex control strategies, achieving voltage balancing, and ensuring power sharing among the modules in these topologies [18, 19].

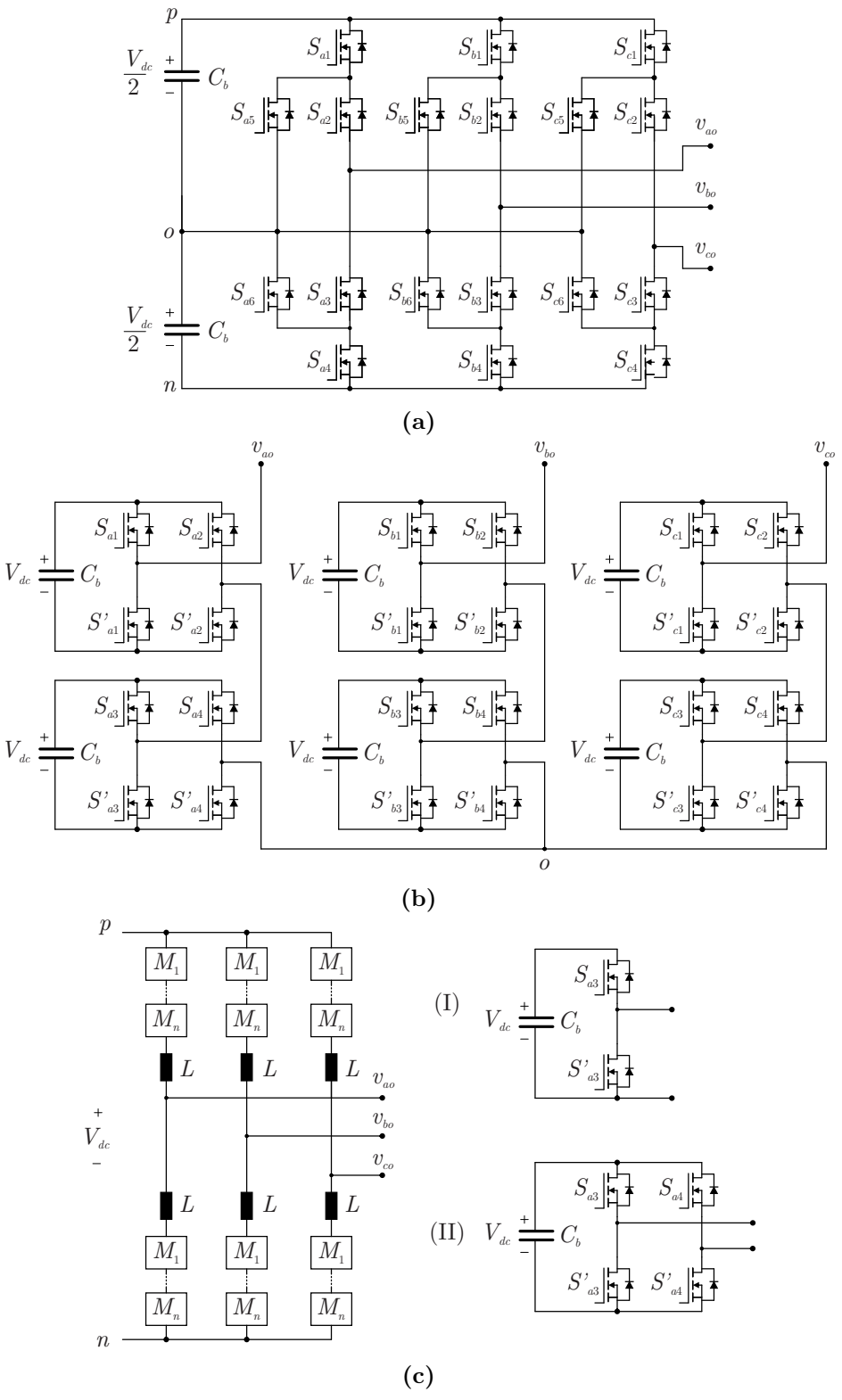


Figure 1.5 – Multilevel converters: ANPC (a), CHB (b) and MMC (c), with the commonly used half-bridge (I) and full-bridge (II) modules.

To enhance the power rating of the lower voltage topologies, multiphase or interleaved converters have been proposed as an alternative to employing parallel semiconductor devices in the classic topologies [20]. This approach involves parallelism of independent power stages operating at the same switching frequency but with delayed gating signals

among the modules [21]. The major benefits of this strategy include equal current and power sharing among modules and harmonic cancellation, leading to reduced size of passive components in filters [22]. Typically, interleaving architecture employs inductors for each module, resulting in a high count of magnetic elements. Some studies [22, 23] utilize single interphase transformers for interleaving, using the magnetic coupling to mitigate circulating currents that are natural in the parallelism of converters. This strategy also reduces the number of magnetic elements employed, when more than two converters are interleaved.

All things considered, this study focuses on developing a solution for a bidirectional AC-DC converter intended for low grid voltage applications, utilizing an interleaved multilevel topology to integrate the advantages of both multilevel capability and interleaving technique. Among multilevel alternatives, the T-Type converter will serve as the base switching module. Interleaving will be achieved through interphase transformers, adopting a generalized approach with n interleaved modules. It will be demonstrated that despite the base module being three-level, interleaving can increase the number of levels in the converter output. The drawback that can be pointed to the proposed solution is associated with implementation and design complexities.

1.1 WORK STRUCTURE

The thesis is structured into five chapters to provide a comprehensive understanding of the specific topics discussed. Chapter 2 focuses on the static analysis of the T-Type interleaved converter, covering aspects such as the basic switching module of the T-Type converter, features of interleaving, simple switched models for observing relevant waveforms, and modulation techniques.

Chapter 3 introduces power loss models for the T-Type interleaved converter and discusses the optimization process using Particle Swarm Optimization (PSO) for designing efficient magnetic elements based on operational parameters. Additionally, a thermal model is presented to evaluate the temperature rise of the magnetic elements. This chapter concludes with the presentation of constraints and final components considered for designing the mains interface filter.

In Chapter 4, a control-oriented model of the converter is proposed using a dynamic-average value in state space method. A closed-loop model is also suggested to assess the dynamic performance of the converter and to tune the controllers within the proposed control strategy. The validation of these models and control techniques is conducted through simulation software.

Lastly, Chapter 5 describes a prototype developed to experimentally validate the proposed power loss and switched-level models used in converter design. Furthermore, an efficiency analysis of the studied modulation techniques is performed.

1.2 OBJECTIVES AND CONTRIBUTIONS

The present work has the main objective of presenting a study on the T-Type interleaved converter. The performed study is conducted in generalized approach concerning the number of interleaved modules in order to analyze the effect of this parameter in the converter's performance. It is also an objective of this work to present tools and methods to design an optimal converter and its control strategy.

Therefore, the contributions of this work are:

- Static analysis of the T-Type interleaved converter with any number of modules;
- Switched-level model to asses the T-Type converter's waveforms of interest for a given set of parameters;
- Optimal design method of boost inductor and interphase transformers in the T-Type converter mains interface filter;
- Control-oriented model and closed-loop model of the converter;
- Efficiency analysis of modulation strategies applied to the T-Type interleaved converter.

Chapter

2 Interleaved T-Type Converter analysis

2.1 INTRODUCTION

This chapter is dedicated to the analysis of the T-Type interleaved converter, developing both quantitative and qualitative insights into its operation. Beginning with an overview of the fundamental switching module, the T-Type converter, and its operational stages, the analysis proceeds with a mathematical characterization of the interleaved T-Type converter for an arbitrary number of modules, alongside an exploration of its rectifier with Power Factor Correction (PFC) operation. Various aspects such as current oscillation on boost inductors, current and voltage oscillation in DC-link capacitors, modulation strategies and harmonic profile are thoroughly addressed. To support the analysis, a numerical model is developed in MATLAB®, which is validated through comparison with PLECS® simulations.

2.2 T-TYPE INTERLEAVED CONVERTER

2.2.1 Basic switching module

The basic switching module of T-Type interleaved converter is the three level T-Type converter, whose structure is shown in Figure 2.1. The DC-link consists of two capacitors with C_b capacitance, from where derives the module's three-level capability. The T-Type converter is based on the two-level voltage source inverter (VSI), comprising the switches $S_{x1,i}$ and $S_{x3,i}$, along with bidirectional switches $S_{x2,i}$ and $S_{x4,i}$ connected to the DC-link neutral-point o, $\forall\, x \in \{a, b, c\}$. This structure determines the phase voltages $v_{i,xo}$ according to the operating states shown in Table 2.1 and assumes that the DC-link capacitors are balanced. To achieve the operating states, a phase disposition pulse width modulation (PD-PWM) scheme with sinusoidal modulation signals was considered, and since it's a well established modulation technique for multilevel converters [24], its details won't be covered in this work.

The operational states shown in Table 2.1 work for both current directions and

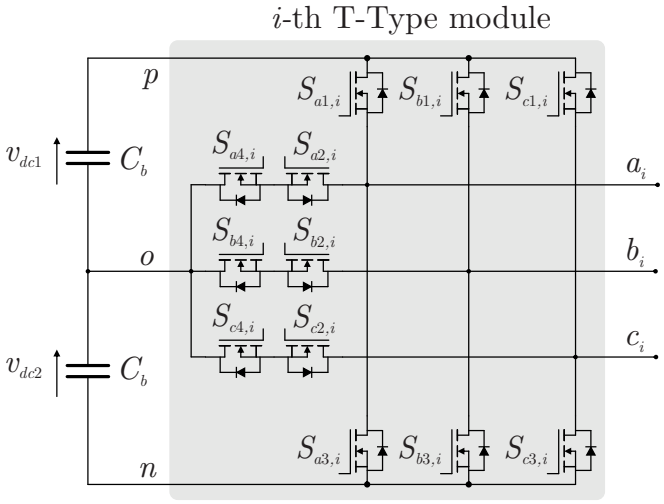


Figure 2.1 – Basic structure of the T-Type converter.

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	$v_{i,xo}$
P	on	off	off	on	$V_{dc}/2$
O	off	on	off	on	0
N	off	on	on	off	$-V_{dc}/2$

Table 2.1 – Operating states of the T-Type converter module.

provide a natural commutation between the states [25]. Figure 2.2 illustrates the current flow during each operational state. For instance, the commutation between the P state to the O state considering a positive current output would occur from the configuration shown in Figure 2.2a to Figure 2.2b. Initially, S_{x1} and S_{x4} are closed then S_{x1} is opened, making the current naturally change its path to S_{x4} and the body diode of S_{x2}. The commutation between the other states is analogous to the one previously described. The commutation process described is valid when the body diode is employed, however, the channel of the MOSFET can be used instead to reduce power losses.

2.2.2 Interleaving T-Type modules

When employing the interleaving technique to n converters, the carriers of each module are equally phase-shifted among adjacent converters of an angle φ, which is given by:

$$\varphi = \frac{2\pi}{n}. \tag{2.1}$$

This technique results in circulating currents among the respective phases of the modules, which can be mitigated with the use of interphase transformers (ITs). In case of n interleaved T-Type modules, the connection of the modules with the interphase transformers is illustrated in Figure 2.3, where each IT has n windings and will be referred to as T_x from now on, $\forall x \in \{a, b, c\}$.

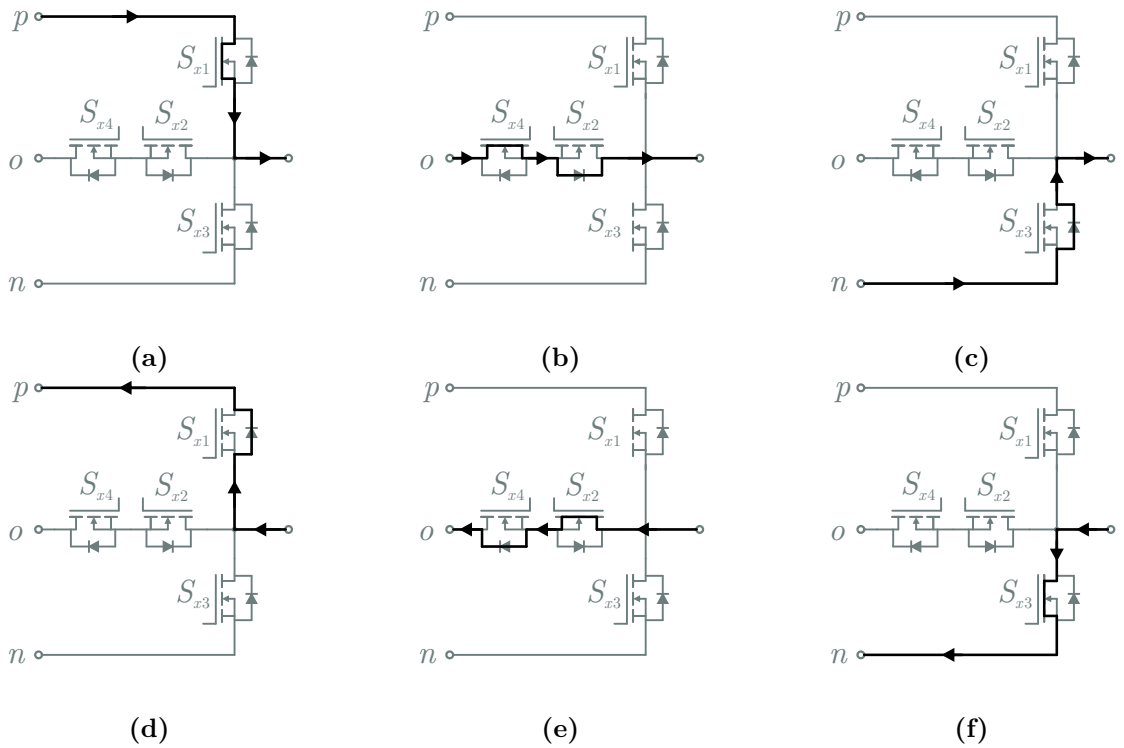


Figure 2.2 – Current path during operational states: P state with positive (a) and negative (d) current output; O state with positive (b) and negative (e) current output; and N state with positive (c) and negative (f) current output.

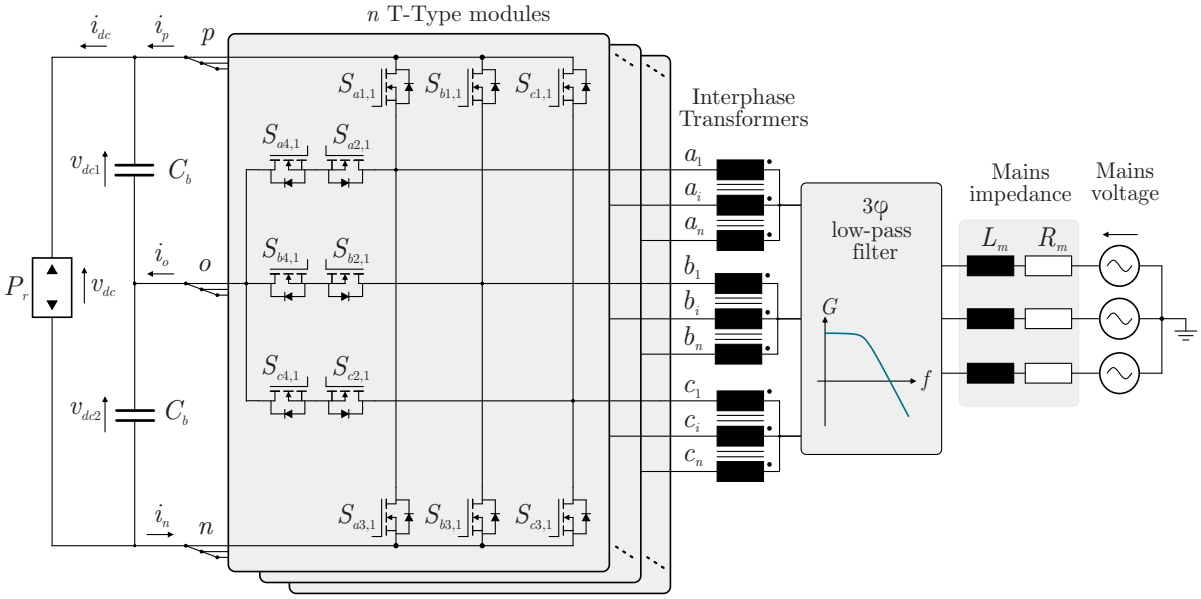


Figure 2.3 – Interleaving of n T-Type modules.

Parallel-connected converters are prone to generate circulating currents due to a range of underlying factors [26, 27, 28, 23]. These factors can be categorized into two main types: physical and logical. The physical factors encompass non-idealities, such as the presence of parasitic elements, deviations in filter parameters, asymmetries in the PCB layout, and variations in phase impedances. On the other hand, the logical factors are

linked to variations in duty cycles inherent in interleaved converters. These logical factors are particularly critical when compared to the physical factors, as they have the potential to lead to overall system failures. Additionally, circulating currents can cause increased current distortion and power losses, electromagnetic interference (EMI), and magnetic element saturation.

To address the challenges posed by circulating currents, diverse techniques can be employed. One approach involves utilizing coupled magnetic elements to increase the impedance in the frequency spectrum of the circulating currents. Moreover, active methodologies can be deployed, by using closed-loop control and the selection of appropriate modulation schemes to ensure equitable current distribution among the converters.

Even in scenarios where interphase transformers are employed, it is advisable to implement a closed-loop control for the circulating currents [29, 30]. This recommendation is due to the inevitability of physical deviations in the interphase transformer windings, including non-ideal coupling. Consequently, relying solely on passive strategies to address circulating currents is insufficient to ensure uniform power distribution among the converters. This highlights the necessity for a hybrid strategy that encompasses active control of these current components.

Even though the interleaving of multiple converters is an atractive option as it aggregates the advantages of the technique, it also brings constructive problems, as the design and assembly of an interphase transformer with multiple core-legs is highly complex. As an alternative, the whiffletree configuration works with multiple transformer stages to form an equivalent interphase transformer [22]. Figure 2.4 shows a comparison between the contructive methods of the interphase transformer. It is worth noting that the interphase transformer must provide a negative coupling factor between all its windings.

(a) **(b)**

Figure 2.4 – Different methods for implementing an interphase transformer: (a) Single core interphase transformer and (b) whiffletree configuration with multi-stage interphase transformer.

2.3 ANALYSIS OF THE T-TYPE INTERLEAVED CONVERTER

2.3.1 The Interphase Transformers

Considering $v_{i,x}$ the voltage across the i-th winding of the IT T_x, the voltage of each winding in T_x is then given by:

$$\underbrace{\begin{bmatrix} v_{1,x} \\ v_{2,x} \\ \vdots \\ v_{n,x} \end{bmatrix}}_{\mathbf{v}_{n,x}} = \underbrace{\begin{bmatrix} L_{11} & L_{12} & \dots & L_{1n} \\ L_{21} & L_{22} & \dots & L_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1} & L_{n2} & \dots & L_{nn} \end{bmatrix}}_{\mathbf{L}_w} D_t \underbrace{\begin{bmatrix} i_{1,x} \\ i_{2,x} \\ \vdots \\ i_{n,x} \end{bmatrix}}_{\mathbf{i}_{n,x}} + \underbrace{\begin{bmatrix} r_w & 0 & \dots & 0 \\ 0 & r_w & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & r_w \end{bmatrix}}_{\mathbf{R}_w} \begin{bmatrix} i_{1,x} \\ i_{2,x} \\ \vdots \\ i_{n,x} \end{bmatrix}, \tag{2.2}$$

where D_t is the differential operator with respect to time, i.e. $D_t f(x) = f'(x)$.

In Equation 2.2, the terms L_{ii}, $\forall\, i \in \{1, 2, ..., n\}$, represent the self-inductance of each winding. For simplicity, the winding self-inductance will be referred to as L_s. The terms L_{ij}, $\forall\, i, j \in \{1, 2, ..., n\}, i \neq j$, represent the mutual inductances between the i-th and the j-th windings. Since the windings are assumed to be perfectly coupled, the mutual inductances are given by:

$$L_{ij} = -\frac{L_s}{n-1}, \qquad i \neq j, \tag{2.3}$$

while the parameter r_w represents the resistance that accounts for power losses in each winding.

To improve readability, Lunze's Transformation is employed to decouple T_x's currents and voltages in Equation 2.2 into differential and common modes [31]. In this work, these modes will be referred to as subtractive and additive modes, respectively, to avoid confusion with the terms used in the context of electromagnetic compatibility (EMC). Lunze's Transformation, denoted by $\mathbf{T}_L$, is defined for an n-dimensional symmetrically coupled linear system as:

$$\mathbf{T}_L = \frac{1}{n} \begin{bmatrix} n-1 & -1 & \dots & -1 & -1 \\ -1 & n-1 & \dots & -1 & -1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -1 & -1 & \dots & n-1 & -1 \\ 1 & 1 & \dots & 1 & 1 \end{bmatrix}_{n \times n}. \tag{2.4}$$

Through $\mathbf{T}_L$, the original system variables, namely the voltage vector $\mathbf{v}_{n,x}$ and the current vector $\mathbf{i}_{n,x}$, are converted to $n-1$ subtractive mode variables and a single additive mode variable, as follows:

$$\mathbf{y}_{sm,am,x} = \mathbf{T}_L\ \mathbf{y}_{n,x}. \tag{2.5}$$

Hence, applying $\mathbf{T}_L$ to Equation 2.2 results in:

$$\mathbf{v}_{sm,am,x} = \mathbf{T}_L \mathbf{L}_w \mathbf{T}_L^{-1} \, D_t \, \mathbf{i}_{sm,am,x} + \mathbf{T}_L \mathbf{R}_w \mathbf{T}_L^{-1} \, \mathbf{i}_{sm,am,x}, \tag{2.6}$$

where the term $\mathbf{T}_L \mathbf{L}_w \mathbf{T}_L^{-1}$ is defined as $\mathbf{L}_{sm,am}$ and is given by:

$$\mathbf{L}_{sm,am} = \begin{bmatrix} L_s \left(\dfrac{n}{n-1} \right) \mathbf{I}_{(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & 0 \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{sm\,(n-1)\times(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & L_{am} \end{bmatrix}. \tag{2.7}$$

Since $\mathbf{R}_w = r_w \, \mathbf{I}_n$, where $\mathbf{I}_n$ is the n-th order identity matrix, the term $\mathbf{T}_L \mathbf{R}_w \mathbf{T}_L^{-1}$ is equal to $\mathbf{R}_w$. Therefore, this analysis reveal that the interphase transformers provide only an inductance for the subtractive modes, whereas the voltage in the additive mode is due to the equivalent resistance of the windings. Then, the resultant expression is:

$$\mathbf{v}_{sm,am,x} = \mathbf{L}_{sm,am} \, D_t \, \mathbf{i}_{sm,am,x} + \mathbf{R}_w \, \mathbf{i}_{sm,am,x}. \tag{2.8}$$

The analysis shows that each decoupled subtractive mode equivalent circuit exhibits an inductance equal to:

$$L_{sm} = L_s \, \frac{n}{n-1}, \tag{2.9}$$

which work as the impedance for limiting circulating currents in each winding. In contrast, the IT introduce only the resistance r_w as impedance for additive mode components.

Regarding the terminal voltage v_{xo} of the interphase transformer with respect to the neutral-point o, Kirchhoff's Voltage Law yields:

$$v_{xo} = v_{i,xo} + v_{i,x}, \tag{2.10}$$

where $v_{i,x}$ represents the voltage across the i-th winding in T_x and $v_{i,xo}$ denotes the x-phase voltage of the i-th T-Type module relative to the neutral-point o.

Considering the n equations of an IT based on Equation 2.10, and applying $\mathbf{T}_L$ results:

$$\begin{bmatrix} v_{xo} \\ v_{xo} \\ \vdots \\ v_{xo} \end{bmatrix} = \begin{bmatrix} v_{1,x} \\ v_{2,x} \\ \vdots \\ v_{n,x} \end{bmatrix} + \begin{bmatrix} v_{1,xo} \\ v_{2,xo} \\ \vdots \\ v_{n,xo} \end{bmatrix} \xrightarrow{\mathbf{T}_L} \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ v_{xo} \end{bmatrix} = \begin{bmatrix} v_{1,sm,x} \\ v_{2,sm,x} \\ \vdots \\ v_{n-1,sm,x} \\ v_{am,x} \end{bmatrix} + \begin{bmatrix} v_{1,sm,xo} \\ v_{2,sm,xo} \\ \vdots \\ v_{n-1,sm,xo} \\ v_{am,xo} \end{bmatrix}. \tag{2.11}$$

Finally, substituting Equation 2.8 in Equation 2.11, results:

$$v_{xo} = r_w \, i_{am,x} + v_{am,xo}. \tag{2.12}$$

The previous analysis showed that the terminal voltage of any IT v_{xo} depends solely on the additive mode current $i_{am,x}$ and the additive mode voltage $v_{am,xo}$ that encompasses the terminal voltage of every T-Type module. This expression leads to the conclusion that even though each module only achieves three voltage levels per phase, the interleaved converter is capable of achieving a higher number of levels. This feature of the proposed converter will be further explored in the following section.

2.3.2 Considerations on PFC rectifier operation

Consider Figure 2.5 as a depiction of the equivalent circuit of the T-Type interleaved converter based on Equation 2.12, where v_x represents the mains voltage and is assumed to be harmonic free, so can be given by:

$$v_x = V_p \sin(\theta_x), \tag{2.13}$$

where V_p is the peak-value of the mains voltage and θ_x represents the angle on the x-phase. On the other hand, v_{cm} represents the common mode voltage with respect to the phase voltage of the converter v_{xo}. For clarity sake, the filtering interface between the mains and the converter's terminals was considered to be of L type, represented by L_b and also referred to as boost inductor in the literature.

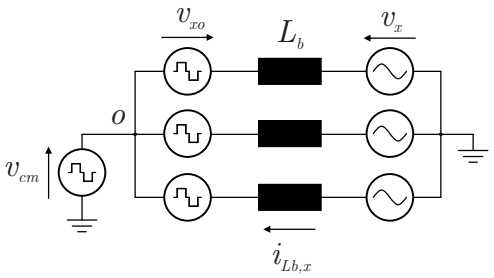


Figure 2.5 – Interleaved T-Type converter equivalent circuit considering an L filter.

To analyze v_{xo}, first consider a switch-level point of view on the i-th module, given by:

$$v_{i,xo} = v_{dc1}\, S_{x1,i}\, \sigma(m_{i,x}) - v_{dc2}\, S_{x3,i}\, \overline{\sigma}(m_{i,x}), \tag{2.14}$$

where $S_{x1,i}$ and $S_{x3,i}$ are the switching functions of the upper and lower semiconductor devices in a phase leg, respectively, $\sigma(x)$ is a function defined by:

$$\sigma(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ 0, & \text{if } x < 0 \end{cases}, \tag{2.15}$$

and $\overline{\sigma}(x)$ is its logical inverse, v_{dc1} and v_{dc2} are the DC-link capacitors' voltages, and $m_{i,x}$ is the x-phase modulation signal of the i-th T-Type module.

The high frequency components are not of interest for the present analysis, so a dynamic average operator is employed to Equation 2.14. In this work, the dynamic average value operator over a period T is defined as:

$$M_T f(t) = \langle f(t) \rangle_T = \frac{1}{T} \int_{t-T}^{t} f(\tau)\, d\tau. \tag{2.16}$$

Considering that the switching frequency is much higher than the mains frequency, the dynamic average value of the switching functions over the switching period T_s can be represented by:

$$\begin{aligned} M_{T_s}(S_{x1,i}\, \sigma(m_{i,x})) &= m_{i,x}\, \frac{\text{sign}\,(m_{i,x}) + 1}{2} \\ M_{T_s}(S_{x3,i}\, \overline{\sigma}(m_{i,x})) &= m_{i,x}\, \frac{\text{sign}\,(m_{i,x}) - 1}{2} \end{aligned}. \tag{2.17}$$

The DC-link voltage is defined as $v_{dc} = v_{dc1} + v_{dc2}$ and the unbalance between the DC-link capacitors voltage is given by $\Delta v_{dc} = v_{dc1} - v_{dc2}$. When relating to the rated value od the DC-link voltage, the uppercase notation V_{dc} will be used hereinafter. Substituting this new definitions and Equation 2.17 to the averaged expression of $v_{i,xo}$ over the switching period T_s yields:

$$M_{T_s}(v_{i,xo}) = \frac{v_{dc}}{2}\, m_{i,x} \left(1 + \frac{\Delta v_{dc}}{v_{dc}} \text{sign}\,(m_{i,x})\right). \tag{2.18}$$

The average voltage $\langle v_{i,xo} \rangle$ represents the fundamental component of the voltage synthesized by a T-Type module and can be represented by:

$$M_{T_s}(v_{i,xo}) = V_p \sin(\theta_x + \phi). \tag{2.19}$$

The parameter ϕ is a phase shift between the mains voltage and the converter output voltage and is related to the power processed in the converter, as will be explained later on this section.

The comparison between Equation 2.18 and Equation 2.19 leads to:

$$m_{i,x} = 2\, \frac{V_p}{V_{dc}} \sin(\theta_x + \phi) \rightarrow m_{i,x} = M \sin(\theta_x + \phi), \tag{2.20}$$

where the DC-link capacitors voltage imbalance was assumed negligible, leading to $v_{dc} = V_{dc}$ and $\Delta v_{dc} = 0$. Equation 2.20 also provides the definition of the modulation index M, which is a fundamental parameter in the context of rectifiers/inverters.

Regarding $i_{Lb,x}$, the analysis of Figure 2.5 reveals the expression:

$$\frac{V_{a,rms} \angle 0 - V_{dm,ao,rms} \angle \phi}{j\omega L_b} = I_{Lb,a,rms} \angle 0 \rightarrow \phi = \text{atan}\left(\frac{I_p \omega L_b}{V_p}\right) \tag{2.21}$$

for phase a. In the resulting expression, $V_{dm,xo,rms}$ is the rms value of the differential mode component of v_{xo}, given by $\mathbf{v}_{dm,abc,o} = \mathbf{T}_{dm} \mathbf{v}_{abc,o}$, where $\mathbf{T}_{dm}$ is the differential mode

transformation given by Equation 2.22. The parameter I_p is the peak-value of the phase current, and is dependent on the rated current processed by the converter.

$$\mathbf{T}_{dm} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{2.22}$$

With the voltage $v_{dm,xo}$ and ϕ defined, the voltage over the boost inductor v_{Lb} and, consequently, its current $i_{Lb,x}$ can be both defined as:

$$v_{Lb,x} = v_x - v_{dm,xo} \quad \therefore \quad i_{Lb,x}(t) = \frac{1}{L_b}\int [v_x(t) - v_{dm,xo}(t)]dt \tag{2.23}$$

The present method of determining v_{Lb} and i_{Lb} is used to numerically determine the waveforms illustrated in Figure 2.6, where f_s is the switching frequency and f_m is the mains frequency. The details of the numerical assessment of the switched waveforms is presented in Appendix A.

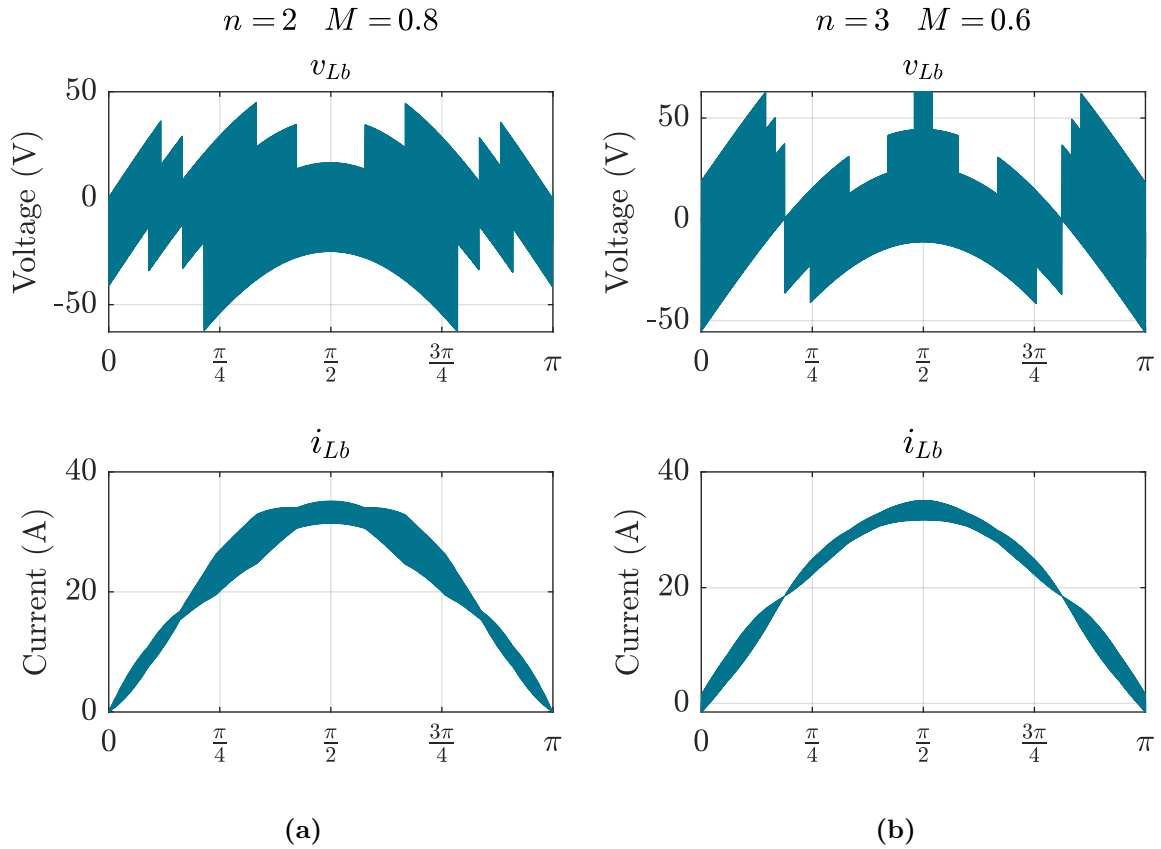


Figure 2.6 – Examples of voltage across the boost inductor v_{L1} and respective current i_{L1} considering a rated power of 5 kW, $L_b = 60\mu$H, $f_s/f_m = 500$, $V_p = 100$ V, $M = 0.8$, $n = 2$ (a) and $M = 0.6$, $n = 3$ (b).

In the presented examples, for the same rated power and boost inductor, the current oscillation changes dramatically by changing the number of interleaved converters n and

the modulation index M, leading to the conclusion that for a practical application of the proposed converter, these parameters must be carefully chosen in order to effectively explore the converter's features.

The presented model can be further explored for obtaining subtractive mode currents. Similarly to the additive mode currents, the expression

$$i_{Lsm,i,x}(t) = \frac{n-1}{nL_s} \int v_{i,sm,x}(t)dt \tag{2.24}$$

describes the mathematical definition of the subtractive mode currents. Figure 2.7 illustrates the method. It is worth noting that, even though the number of interleaved converters in Figure 2.7b is greater than in Figure 2.7a, the subtractive mode current in the former has a larger maximum value due to the smaller modulation index.

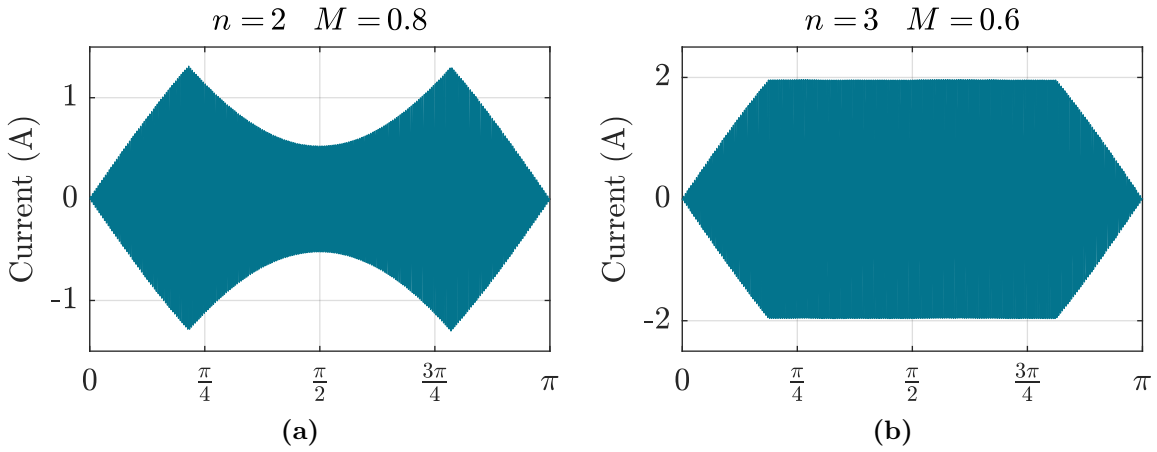


Figure 2.7 – Examples of subtractive mode currents $i_{i,sm,x}$ considering a rated power of 5 kW, $L_s = 200\mu H$, $f_s/f_m = 500$, $V_p = 100V$, $M = 0.8$, $n = 2$ (a) and $M = 0.6$, $n = 3$ (b).

2.3.3 Multilevel capability

As stated, the interleaving requires equal phase-shift of the carriers among the modules. Figure 2.8 presents the positive half-cycle carriers disposition for n interleaved T-Type converters, considering the angle reference in the switching frequency. Note that the n-th carrier coincides with the first of the next switching period, leaving only $n-2$ carriers between each period.

For the i-th carrier, the point of intersection with the first carrier descending segment occurs at θ_i with a value of y_i, which are given by:

$$\begin{cases} \theta_i = \pi\left(1 + \dfrac{i}{n}\right) \\ y_i = 1 - \dfrac{i}{n} \end{cases}. \tag{2.25}$$

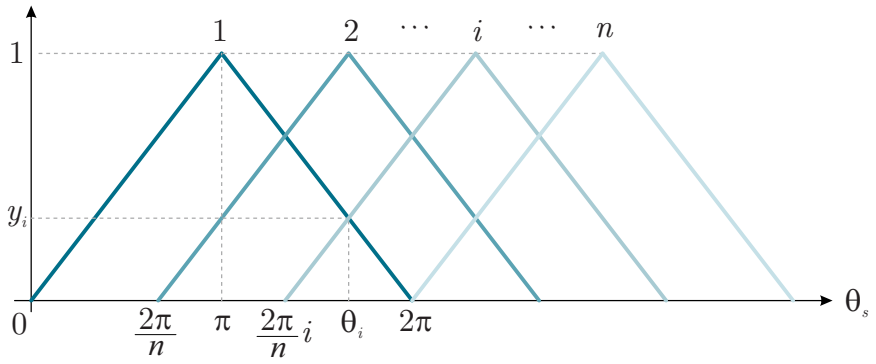


Figure 2.8 – Positive half-cycle carriers for n interleaved T-Type converters.

This results into $n-1$ threshold values that divide the amplitude axis into n regions. Each region causes the output voltage to increase its level count by one. This analysis results into the maximum number of levels the phase output can have, given by:

$$n_{lvl,max} = 2\,n + 1. \tag{2.26}$$

Even though the maximum number of levels in the phase voltage depends solely on the number of interleaved converters, the effective number of levels also depends on the modulation index M, which will define the operation region where the converter will operate for a given n. Therefore, the effective number of levels that the converter can achieve is given by:

$$n_{lvl,ef} = 2\{n - \text{floor}[n(1-M)]\} + 1. \tag{2.27}$$

To exemplify, Figure 2.9 illustrates how the switched phase voltage v_{xo} behaves for three different modulation indexes, considering $n = 3$ and a fixed DC-link voltage V_{dc}.

The angles at which the voltage level transition occurs is also dependent on n and M, and is given by:

$$\theta_i = \text{asin}\left(\frac{n-i}{Mn}\right), \quad i \in \{0, 1, \ldots, n-1-\text{floor}[n(1-M)]\}. \tag{2.28}$$

One should note that the sinusoidal signal is symmetrical on a quarter of its period, an so is the voltage level transitions, as depicted in Figure 2.9.

Finally, it should be noticed that the voltage on each level is a fraction of the total voltage available in the DC-link V_{dc}. So, the voltage on each level is given by:

$$v_{lvl} = \frac{V_{dc}}{2n}\,i, \qquad i \in \{1, \ldots, n\}. \tag{2.29}$$

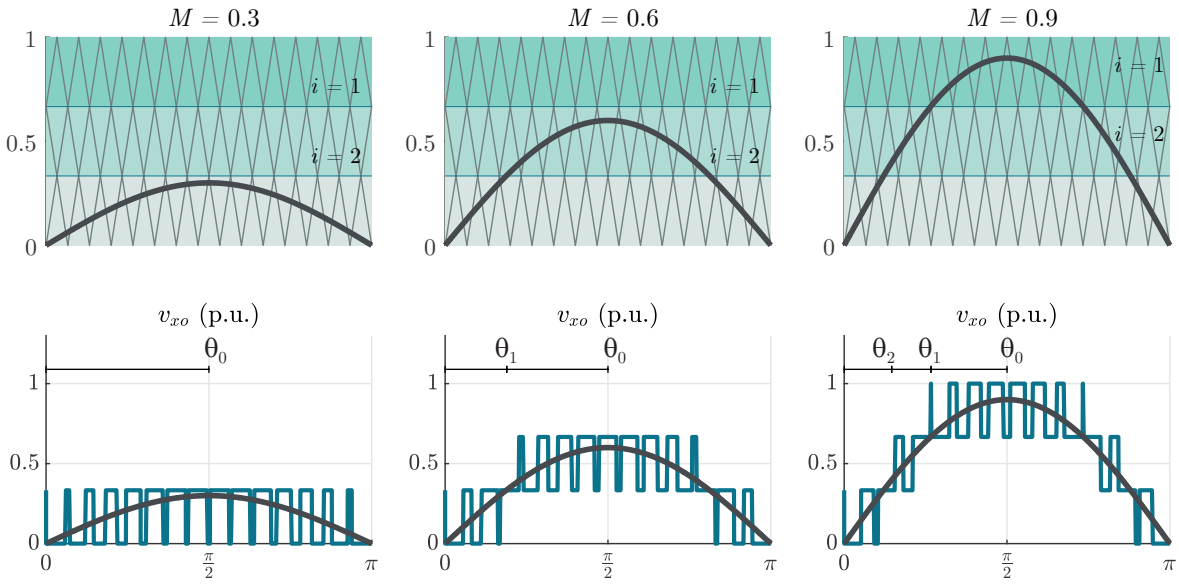


Figure 2.9 – Comparison between modulation signals and phase voltages v_{xo} for different modulation indexes. Number of interleaved converters: $n = 3$; Frequency ratio: $f_s/f_m = 10$; Voltage reference: 1.0 p.u. $= V_{dc}/2$.

2.3.4 Current in the DC-link capacitors

The current on the DC-link capacitors can be obtained by observing Figure 2.3, which provides:

$$\begin{aligned} i_{C1} &= -i_{dc} + i_p \\ i_{C2} &= -i_{dc} + i_n. \end{aligned} \tag{2.30}$$

The current in the upper and lower branches in DC-side of the converter, i_p and i_n respectively, are given by:

$$\begin{aligned} i_p &= \sum_{x=a,b,c} \sum_{i=1}^{n} S_{x1,i}\, \sigma(m_{i,x}) i_{i,x} \\ i_n &= -\sum_{x=a,b,c} \sum_{i=1}^{n} S_{x3,i}\, \overline{\sigma}(m_{i,x}) i_{i,x}. \end{aligned} \tag{2.31}$$

Substituting Equation 2.31 in Equation 2.30, results:

$$\begin{aligned} i_{C1} &= -i_{dc} + \sum_{x=a,b,c} \sum_{i=1}^{n} S_{x1,i}\, \sigma(m_{i,x}) i_{i,x} \\ i_{C2} &= -i_{dc} - \sum_{x=a,b,c} \sum_{i=1}^{n} S_{x3,i}\, \overline{\sigma}(m_{i,x}) i_{i,x}, \end{aligned} \tag{2.32}$$

which consists on a switch-level method to analyze the current in each of the DC-link capacitors.

Applying the proposed numerical approach, the switched current on the DC-link

capacitors can be obtained, as shown in the examples in Figure 2.10.

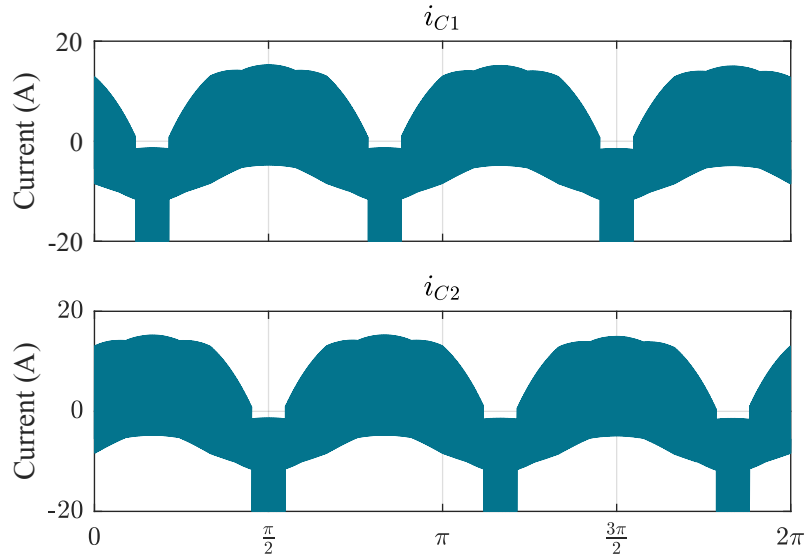


Figure 2.10 – Current in the DC-link capacitors considering a rated power of 5 kW, $L_1 = 60\,\mu H$, $f_s/f_m = 500$, $V_p = 100\,V$, $n = 2$ and $M = 0.8$.

With the switched current on the DC-link capacitors defined, it is possible to determine the rms current as shown generically in Algorithm 1.

Algorithm 1 Rms value numerical evaluation.

1: **Input**: Input vector vector $\mathbf{x}$, time vector $\mathbf{t}$, fundamental frequency f;
2: **Output**: RMS value of the input vector $\mathbf{x}$;
3: **for** $i = 2, \ldots, \text{length}(\mathbf{t}) - 1$ **do**
4: $\quad (x_{rms})^2 \leftarrow (x_{rms})^2 + f\ [\mathbf{t}(i) - \mathbf{t}(i-1)]\,[\mathbf{x}(i)^{\,2} + \mathbf{x}(i-1)^{\,2}]\,/2$;
5: **end for**
6: $x_{rms} \leftarrow \sqrt{(x_{rms})^2}$;

To validate the proposed method to evaluate the current stress on the DC-link capacitor, simulations were employed in PLECS® and the results were compared with the ones obtained through the proposed method. Since the small relative error observed between the simulations, the proposed method is considered validated. The larger errors observed can be assigned to the numerical error carried through the integration processes required to obtain i_{C1} and i_{C2}, which can only be minimized but not completely removed from the data.

2.3.5 Voltage oscillation in the DC-link capacitors

Due to the numerical errors accumulated to obtain i_{C1} and i_{C2}, the model used to compute the signals of interest in the T-Type converter cannot be used to assess the voltage oscillation in the DC-link capacitors, as the numerical error would only be carried

Simulation	M	**PLECS** (A)	**Proposed** (A)	**Error** (%)
I	0.8	8.5266	8.3301	0.3026
II	0.6	6.6485	6.6245	0.3610
III	0.4	7.4775	7.6877	2.8111
IV	0.2	7.9754	7.8073	2.1083

Table 2.2 – DC-link capacitors rms current validation. Parameters: 5 kW, $L_1 = 60\,\mu H$, $f_s/f_m = 500$, $V_p = 100\,V$ and $n = 2$.

through another integration process. Therefore, the analysis of the voltage dynamics in the DC-link will be carried out in Chapter 4.

However, from the converter's operation and from the analysis of Figure 2.10, it can be inferred that the capacitors receive current from each phase leg for only a half-cycle of the mains and due to the three-phase topology, the capacitors currents (and their voltages) carry a third harmonic. Another aspect to consider is that the currents in the capacitors are displaced of 180°.

In this work, the hold-up time (HUT) method was chosen to define the DC-link capacitances C_b, as given by [32]:

$$C_{b,min} = \frac{2P_r\Delta t}{V_{dc}^2 - V_{dc,min}^2}, \tag{2.33}$$

where P_r is the rated power of the system, V_{dc} is the rated DC-link voltage, $V_{dc,min}$ is the minimum DC-link voltage required in power outages and Δt is the time considered for the voltage to drop from V_{dc} to $V_{dc,min}$. Usually, Δt is assumed to be proportional to the mains period.

2.3.6 Modulation strategies

The analysis conducted thus far has solely focused on purely sinusoidal modulation signals (SPWM). However, literature [22] offers various modulation schemes for rectifiers, which incorporate a common-mode component to provide the converter with distinct characteristics.

The first alternative modulation strategy is the carrier-based Space Vector (SVM), which grants the converter the capability of increasing the modulation index up to $M = 2/\sqrt{3} \approx 1.155$. This feature provides more dynamic and static range for the converter and allows the DC-link voltage to be lower in comparison to the sinusoidal modulation. The common mode component of this strategy is given by

$$m_{cm,svm} = -\frac{1}{2}\left[\max(m_a, m_b, m_c) + \min(m_a, m_b, m_c)\right]. \tag{2.34}$$

Figure 2.11 illustrates the original sinusoidal modulation signal of a single phase in comparison to the SVM modulation signal and the corresponding common mode component.

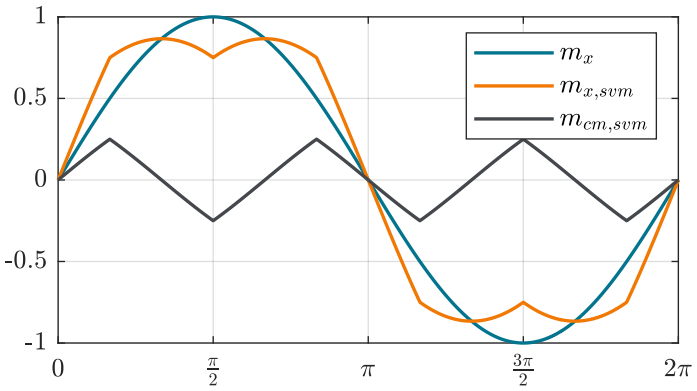


Figure 2.11 – Modulation signal and common mode component of the SVM scheme for $M = 1$.

Alternatively, the Sinusoidal Third Harmonic Injection (STHI) is a modulation scheme where the common-mode component is a purely sinusoidal signal with three times the fundamental frequency. The gain of the common-mode component depends on the desired characteristic: if the gain is 1/6, the converter behaves similarly to Space Vector Modulation (SVM) with a maximum modulation index of $M_{max} \approx 1.155$ [24]; and if the gain is 1/4, the maximum modulation index is $M_{max} \approx 1.122$. In the case of a converter with a split DC-link such as the one studied in this work, the 1/4 gain also minimizes the current at the central point o, consequently reducing voltage oscillation in the capacitors [22]. The 1/4 gain of the common-mode component is particularly relevant for this study and will be considered for the STHI modulation scheme. The common-mode component is expressed by:

$$m_{cm,sthi} = \frac{M}{4} \sin(3\theta), \tag{2.35}$$

and Figure 2.12 illustrates the modulation signal. Further analysis on this modulation strategy is shown in Chapter 5.

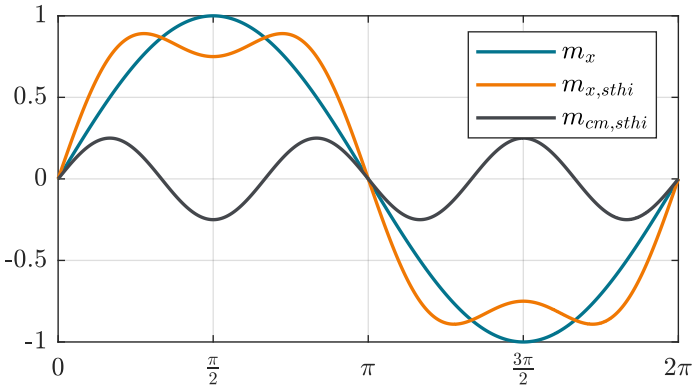


Figure 2.12 – Modulation signal and common mode component of the STHI modulation scheme for $M = 1$.

The last modulation scheme considered in the present work is the Discontinuous PWM (DPWM), which aims to reduce switching losses by clamping the output voltage in

$V_{dc}/2$, $-V_{dc}/2$ or 0, in case of three-level converters. A drawback of this strategy is that, by reducing the number of switching cycles per mains period, the current in the boost inductor increases. Numerous DPWM schemes can be found in the literature [33, 34], and in this study, the common-mode component will be defined following the approach proposed in [33]. In this context the common-mode component for the DPWM is defined as:

$$m_{cm,dpwm} = \frac{\text{sign}\left(m'_{max}\right)}{2} - m'_{max}, \tag{2.36}$$

where m'_{max} and the m'_x terms are determined by:

$$m'_{\max} = \begin{cases} m'_a \text{ if } |m'_a| = \max(|m'_a|, |m'_b|, |m'_c|) \\ m'_b \text{ if } |m'_b| = \max(|m'_a|, |m'_b|, |m'_c|) \\ m'_c \text{ if } |m'_c| = \max(|m'_a|, |m'_b|, |m'_c|) \end{cases} \text{where} \quad \begin{array}{l} m'_a = (m_a + 1) \bmod (1) - 0.5 \\ m'_b = (m_b + 1) \bmod (1) - 0.5 \\ m'_c = (m_c + 1) \bmod (1) - 0.5 \end{array} \tag{2.37}$$

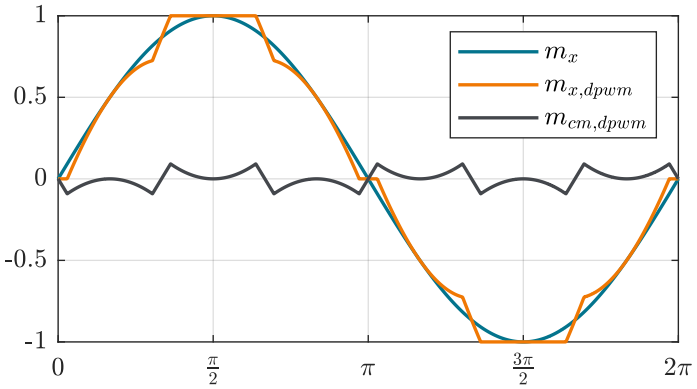


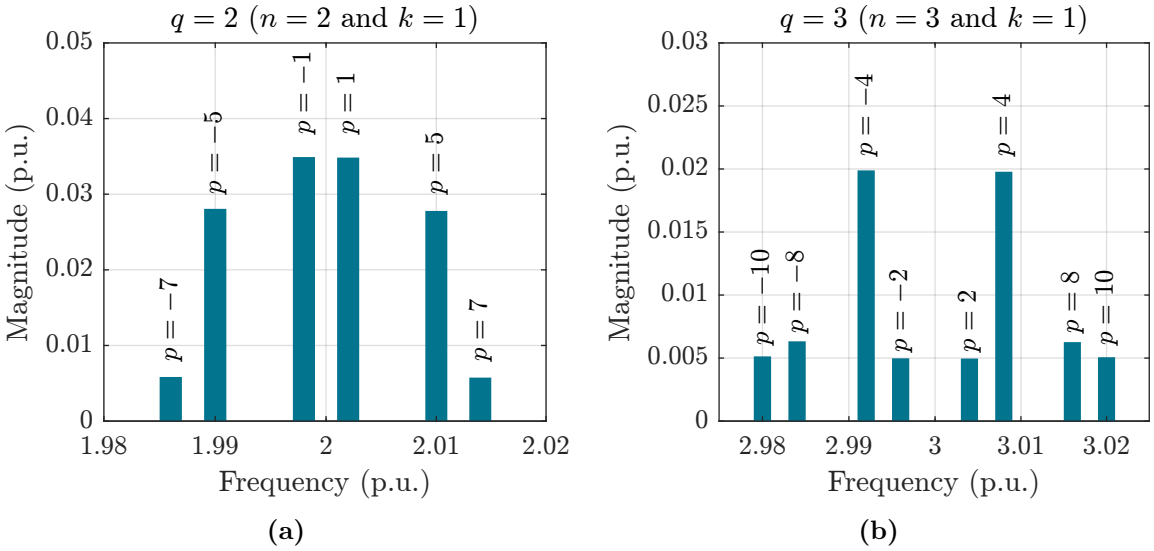
Figure 2.13 – Modulation signal and common mode component of the DPWM scheme for $M = 1$.

2.3.7 Harmonic profile

To analyze the harmonic profile of the IT output current, i.e. the current i_{L_b}, the frequency spectrum is given by [22]:

$$f = pf_m + qf_s \quad \text{where} \quad q = nk, \; k \in \mathbb{N}_0, \; p \in \mathbb{Z}. \tag{2.38}$$

Therefore, the first high frequency harmonic ($k = 1$) happen at $f = nf_s$. Figure 2.14 illustrates the harmonic profile through MATLAB® *fft* function at $k = 1$ for the cases when $n = 2$ and $n = 3$. In the figure, the magnitude is normalized to I_p and the frequency values are normalized to f_s. This feature of the interleaved T-Type converter allows compact filter designs to interface with the mains, which is advantageous for designs with volume and weight restrictions.



(a) **(b)**

Figure 2.14 – Normalized first high frequency harmonic ($k = 1$) for $n = 2$ (a) and $n = 3$ (b). Parameters: $P_r = 5$ kW, $L_1 = 60\,\mu H$, $f_s/f_m = 500$, $V_p = 100\,V$, and $M = 0.8$.

2.3.8 Current oscillation in the boost inductor

In a previous section, a method to determine the boost inductor current i_{Lb} was presented. The showcased examples revealed that the current oscillation depends not only of the inductance L_b but also on the parameters n, M and θ. Figure 2.15 shows the variation of the current oscillation envelope over half of the mains period for different modulation indexes, which were obtained by varying the DC-link voltage. It can be inferred that the analytical determination of Δi_{Lb} requires great mathematical effort and it would return a table for each mains interval that represent the current oscillation behavior, and therefore, it would not be of practical use. Hence, in the present work, the assessment of the current oscillation was achieved through the proposed computational approach.

The computational method extends its utility to various modulation strategies, as exemplified in Figure 2.16, where the current ripple is compared between additive and subtractive modes across previously defined modulation schemes, while also considering variations in the number of interleaved modules.

2.3.9 Coupled boost inductor variation

Instead of utilizing a single boost inductor connected to the terminal of the IT in each phase, an alternative approach involves employing a coupled boost inductor with n windings connected in series with the IT for each phase as shown in Figure 2.17a. The dot notation was supressed to avoid conflict between both magnetics elements, and instead, each is identified by the coupling factor α_c.

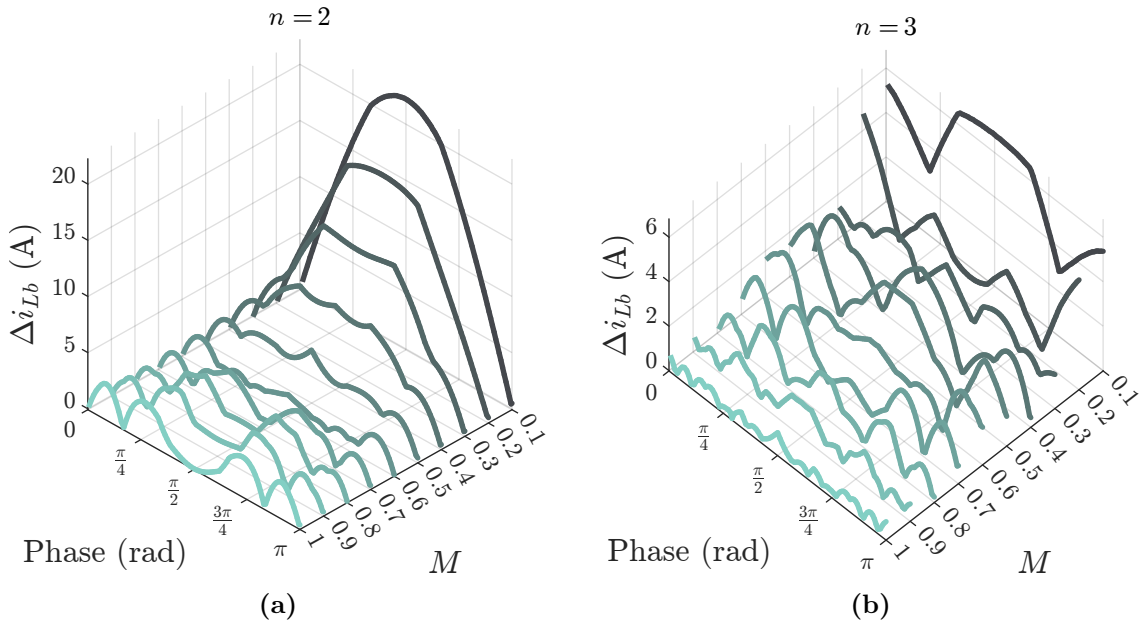


Figure 2.15 – Normalized current oscilation envelope ΔI_{Lb} for several modulation indexes (variating V_{dc}) considering a rated power of 5 kW, SPWM, $L_b = 60\,\mu H$, $f_s/f_m = 250$, $V_p = 100\,V$, $n = 2$ (a) and $n = 3$ (b).

Under this method, the phase voltage v_{xo} is determined by:

$$\begin{bmatrix} v_{xo} \\ \vdots \\ v_{xo} \end{bmatrix} = \underbrace{\begin{bmatrix} L_{11,b} + L_{11,s} & \dots & L_{1n,b} + L_{1n,s} \\ \vdots & \ddots & \vdots \\ L_{n1,b} + L_{n1,s} & \dots & L_{nn,b} + L_{nn,s} \end{bmatrix}}_{\mathbf{L}_{w,bs}} D_t \begin{bmatrix} i_{1,x} \\ \vdots \\ i_{n,x} \end{bmatrix} + \underbrace{\begin{bmatrix} r_{w,bs} & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & r_{w,bs} \end{bmatrix}}_{\mathbf{R}_{w,bs}} \begin{bmatrix} i_{1,x} \\ \vdots \\ i_{n,x}. \end{bmatrix} \tag{2.39}$$

Here, $L_{ii,s}$, $i \in 1, 2, ..., n$, denotes the self-inductance of each winding in the IT, while $L_{ii,b}$, also with $i \in 1, 2, ..., n$, represents the self-inductance of each winding in the coupled boost inductor. As the previous setup, the self-inductance of the IT windings is denoted as L_s, while the self inductance of the coupled boost inductor is denoted as L_b. Additionally, $L_{ij,b}$, $i, j \in 1, 2, ..., n$ and $i \neq j$, signifies the mutual inductances between the i-th and the j-th windings in the coupled boost inductor. Assuming perfect coupling of windings, the mutual inductances are described by:

$$L_{ij,b} = \frac{L_b}{n-1}, \qquad i \neq j. \tag{2.40}$$

Lastly, the parameter $r_{w,bs}$ accounts for an equivalent resistance, representing power losses in both series windings.

Applying $\mathbf{T}_L$ to Equation 2.39 results:

$$v_{xo}\boldsymbol{\lambda} = \mathbf{T}_L \mathbf{L}_{w,bs} \mathbf{T}_L^{-1} D_t \, \mathbf{i}_{sm,am,x} + \mathbf{T}_L \mathbf{R}_{w,bs} \mathbf{T}_L^{-1} \, \mathbf{i}_{sm,am,x}, \tag{2.41}$$

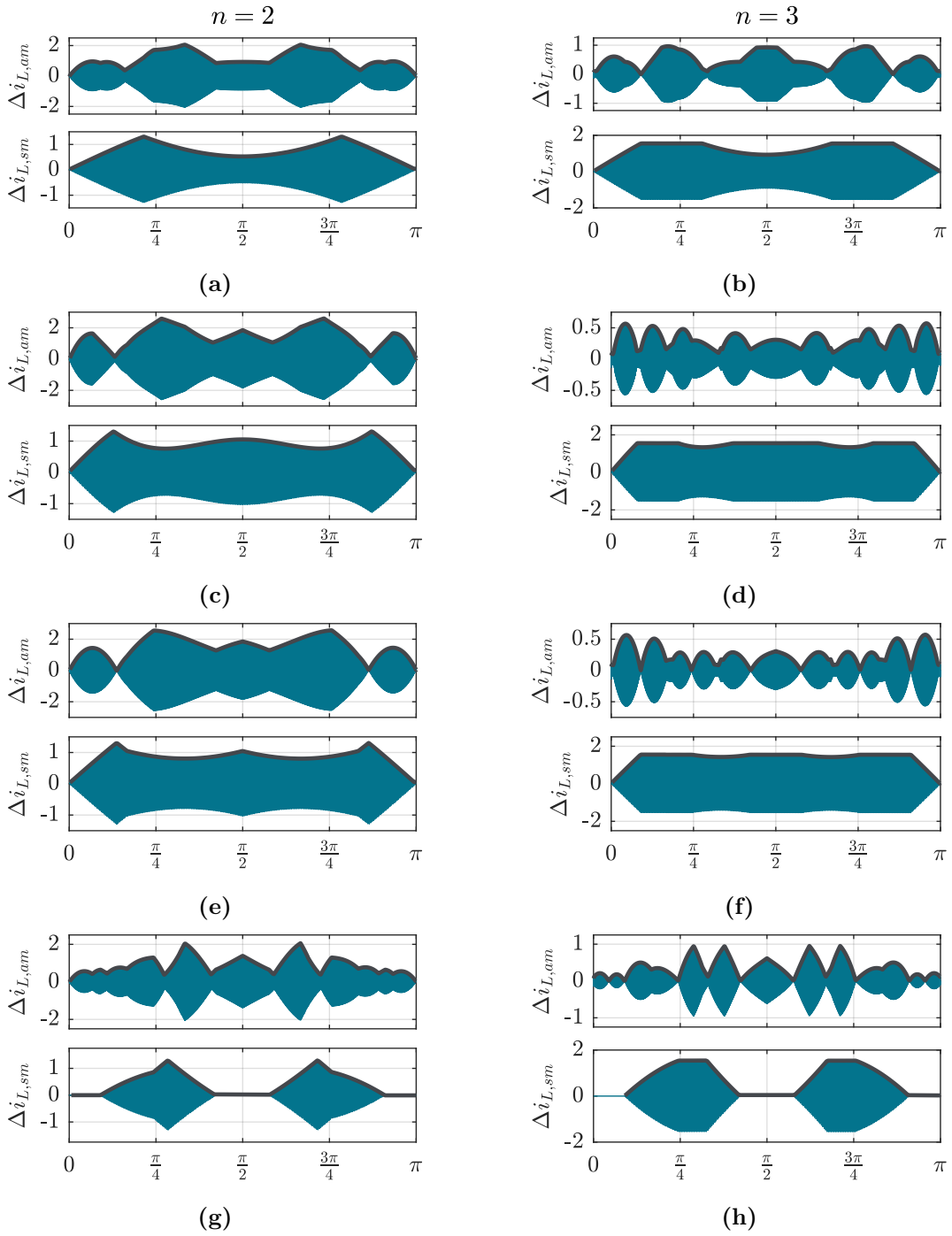


Figure 2.16 – Current oscillation and corresponding envelope for additive and subtractive modes considering $P_r = 5$ kW, $L_b = 60\,\mu$H, $L_s = 200\,\mu$H, $f_s/f_m = 500$, $V_p = 100$ V, SPWM (a, b), STHI (c, d), SVM (e, f) and DPWM (g, h).

where $\boldsymbol{\lambda} = [0 \ldots 1]^T_{1\times n}$. The term $\mathbf{T}_L \mathbf{R}_{w,bs} \mathbf{T}_L^{-1}$ results $r_{w,bs}\,\mathbf{I}_n$ and $\mathbf{T}_L \mathbf{L}_{w,bs} \mathbf{T}_L^{-1}$, denoted by $\mathbf{L}_{sm,am,bs}$, with $n \neq 1$, is equal to:

$$\mathbf{L}_{sm,am,bs} = \begin{bmatrix} \dfrac{(n-2)\,L_b + n\,L_s}{n-1}\,\mathbf{I}_{(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & 2\,L_b \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{sm\,(n-1)\times(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & L_{am} \end{bmatrix} \tag{2.42}$$

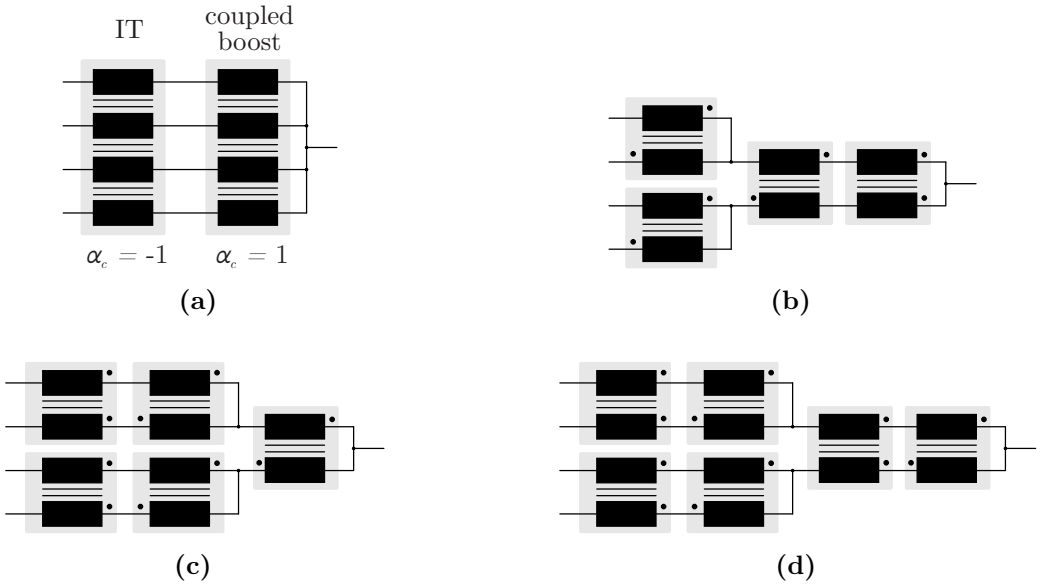


Figure 2.17 – Series connection between IT and coupled boost inductor with n windings (a); Whiffletree configuration with a single couple boost inductor per phase (b), a coupled boost inductor per pair of interleaved legs (c) and the same amount of coupled inductors as ITs per phase (d).

The approach of coupling the boost inductance in each phase as described can increase the subtractive mode inductance when n is greater than 2. When $n = 2$, the subtractive mode inductance depends only on the self inductance of the interphase transformer. However, one can point that the additive mode inductance is always $2L_b$ independently of n, which may be a drawback when a larger boost inductance is required since the magnetic design turns into a complex challenge.

Regarding the whiffletree configuration, Figures 2.17b, 2.17c and 2.17d show different ways to implement the coupling of the boost inductor, where the dot notation is adopted to identify each magnetic element. In Figure 2.17b, the equivalent additive and subtractive modes are the same as the Figure 2.17a case analyzed before, with the merit of employing magnetic elements with easier design and physical implementation. In Figure 2.17c, the equivalent boost inductance is also $2L_b$, however, the subtractive mode in the outer layer is added with a $2L_b$ term. Lastly, in Figure 2.17d the equivalent boost inductance is $4L_b$ and the presence of the coupled boost inductor in both layers increment even further the equivalent subtractive modes inductance, with the cost of being the alternative that employs the higher count of magnetic elements. Therefore, considering the design complexity, number of magnetic elements and subtractive and additive mode equivalent inductances, the option depicted in Figure 2.17b is the most relevant among the ones presented. An efficiency-wise comparison of the Figure 2.17b method is carried out in Chapter 3.

2.4 CONCLUSION

This chapter introduces the three-phase T-Type interleaved converter and outlines its major characteristics. A numerical model was developed to analyze the converter's switched waveforms of currents and voltages. This model is versatile, enabling simulation of the converter under various parameters without increasing in complexity. Despite its simplicity, the model demonstrated good fidelity with PLECS® simulations. A drawback of the numerical method is the absence of analytical equations to describe the converter's features. However, given the converter's complex operation states, the focus was on developing a more intuitive analysis tool.

All things considered, the model is an important asset for quantitative analysis of the converter, and thus it was used for the design of the passive components addressed in Chapter 3.

Chapter

3 Optimization-aided magnetic element design

3.1 INTRODUCTION

The design of the low-pass passive filter that interfaces a three-phase rectifier with the mains has been approached in various ways in the literature. The most cited systematic design procedure is presented in [35]. This procedure focuses on reducing the current ripple generated by the switching process to a desired level, and it was used as base for several systematic design methods [36, 37, 38]. These methods favors designs with higher harmonic content attenuation and lower current oscillation, resulting in normally bulky filters, which may be a drawback considering the physical implementation constraints, such as weight and volume.

As an alternative, optimization-based approaches have gained attention in the literature [39, 40, 41, 42]. Optimization methods typically involve iterative algorithms that adjust parameters while evaluating a model of the analyzed system, in order to maximize or minimize specifics figures of merit. In the context of filter design, power quality factors such as harmonic attenuation, along with performance indicators like efficiency and temperature rise, serve as common criteria for evaluating the feasibility of the design.

In this context, the present chapter will be dedicated to present a filter design focused on optimal efficiency. Hence, to assess the efficiency of the T-Type converter, the power losses model in the semiconductor devices and magnetic elements will be presented in the following sections. Also, a thermal model was developed in order to predict the magnetics operating temperature, which was used as a design constraint.

The main objective of this chapter is to present a systematic design methodology for the boost inductor and interphase transformers employed in the T-Type interleaved converter. In accordance with the discussion, Table 3.1 provide the parameters of the system that will be considered for the filter discussion and design.

Parameter	Description	Value
P_r	Rated power	10 kW
V_{rms}	Mains rms phase voltage	127 V
f_m	Mains frequency	60 Hz
V_{dc}	DC-link voltage	400 V
n	Number of interleaved modules	2
f_s	Switching frequency	35 kHz

Table 3.1 – Parameters for optimally designed filter.

3.2 BOOST INDUCTOR AND INTERPHASE TRANSFORMER DESIGN

To effectively optimize the design of a magnetic element, it is crucial to comprehend the mathematical principles governing its operation. This understanding enables the identification and elimination of impractical or suboptimal designs throughout the iterative optimization process, ensuring the development of viable and desirable solutions.

In this context, the material and shape of the cores are the basic information required to analyze a magnetic element. As for the boost inductor, toroidal iron powder cores were considered. Toroidal cores have advantages such as reduced magnetic coupling with surrounding elements, smaller proximity power losses and small volume due to lower thermal resistance, however, this type of core presents disadvantages such as difficulty to wind and to include a gap and high costs. As for the iron powder material, it has a low permeability, which exempts the necessity of air gaps and allows high flux density. In the present work, the 0088439A7 toroidal AmoFlux core (Magnetics) was used to design the boost inductors.

For the interphase transformers, E ferrite cores were considered. This type of core is normally employed for high frequency range, given its high electrical resistivity and low eddy currents. Ferrite materials offer a high permeability, allowing the design of high inductance magnetics with fewer turns. In the present work, the E 42/21/20 N97 ferrite core (TDK) was used to design the interphase transformers.

With the core's shape and material defined, the constructive aspects and electrical characteristics of the boost inductor and interphase transformers can be determined. The following sections disccuss each magnetic element particular features that lead to the design employed in the optimization process.

3.2.1 Boost inductor

After selecting the core, determining the number of turns necessary for achieving the desired boost inductance is achieved through the following expression:

$$N_{t,L_b} = \sqrt{\frac{L_b}{A_L}}, \tag{3.1}$$

where A_L represents the inverse of the core's reluctance. For iron powder toroidal cores, A_L is typically a predetermined parameter provided by the core manufacturer in the product's datasheet. In the case of coupled boost inductors, L_b represent the self-inductance and N_{t,L_b} the number of turns of each winding.

In practice, the inductance of a ferromagnetic core inductor is not constant due to the non-linear correlation between the magnetic field and the magnetic flux density. As current in the windings rises, the core's permeability decreases, subsequently decreasing the inductance. Manufacturers typically provide the relationship between the core's permeability and the magnetic flux in the form of a curve. For the 0088439A7 core, Figure 3.1 illustrates this relationship.

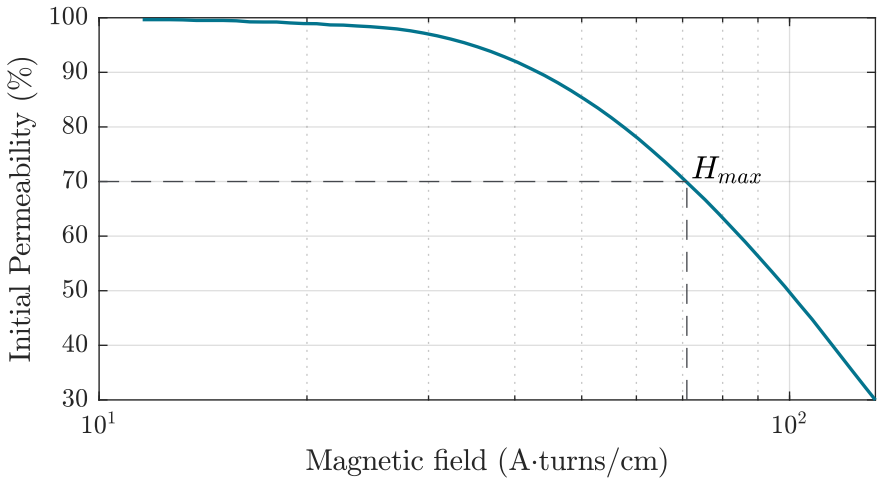


Figure 3.1 – Voltage and current of the boost inductor considering the parameters on Table 3.1.

To account for the core's saturation, the optimization process considers a maximum magnetic flux allowed fo the inductor, which corresponds to an arbitrarily chosen 30% drop on the inductance, as illustrated in Figure 3.1 .In this context, for a given design, the maximum magnetic field contribution by each winding for the total magnetic field in the core is given by:

$$H_{max,L_b} = \frac{N_{t,L_b} I_{max,L_b}}{l_c}, \tag{3.2}$$

where I_{max,L_b} is the maximum current observed in the winding and l_c is the mean magnetic path length of the core. Therefore, designs that make the cumulative sum of H_{max,L_b} greater than H_{max} are considered unfeasible and are discarded from the optimization.

As stated previously, the boost inductors can be employed as single windings magnetics or coupled inductors. This choice ensures that the impedance in additive mode remains consistent at $2L_b$ when utilizing the same toroidal core. Consequently, the number of turns in the core remains constant regardless of the selected alternative. However, with coupled boost inductors, the current in each winding is halved compared to the single-winding option, enabling the use of thinner wire and resulting in less bulky designs.

Despite accommodating subtractive mode currents, the coupled alternative is anticipated to yield a more compact overall design.

For the winding, the first constraint is associated to the current carrying capacity, which is named current density and is given by:

$$J_w = \frac{I_{rms}}{n_p A_w}, \tag{3.3}$$

where A_w is the cross section area of the wire. The maximum current density of a winding is dependent on the material and its maximum value was assumed to be 2000 A/cm^2 for the copper [23].

For the constructive aspects of the winding, for a specific number of required turns N_{L_b}, it is necessary to determine the number of layers required for a given winding made with n_p paralleled wires of r_{awg} radius. This information is essential for winding losses calculation, and in the present work it was determined employing Algorithm 2.

Algorithm 2 Number of layers of a toroidal core winding.

Input: core internal radius r_c, number of parallel wires n_p, wire radius r_{awg}, required number of turns N_{t,L_b};
Output: number of layers n_l;
$r_b \leftarrow n_p r_{awg}$;
$r_{eq} \leftarrow r_c$;
$n_l \leftarrow 1$;
$n_{turns} \leftarrow N_{t,L_b}$;
while $2n_{turns}r_b > 2\pi(r_{eq} - r_b)$ **do**;
    $n_{turns} \leftarrow n_{turns} - \text{floor}(2\pi(r_{eq} - r_b)/(2r_b))$;
    $r_{eq} \leftarrow r_{eq} - 2r_b$;
    if $n_{turns} \leq 0$ or $r_{eq} \leq 0$ **then**
        break;
    end if
    $n_l \leftarrow n_l + 1$;
end while

Finally, for a given winding configuration, the window utilization factor k_w is a numeric assessment of the disposable space on the core. To determine k_w, it follows:

$$k_w = \frac{2\, N_{t,L_b}\, n_p\, A_w}{W_c}, \tag{3.4}$$

where W_c is the window area of the core.

3.2.2 Interphase transformer

After the core selection, the structure of the interphase transformers must be defined, as its an essential aspect on the losses calculation. In this context, the structure

considered for the ITs is employing EE ferrite cores, where the wingdings are wound in a plastic coil former placed on the central leg.

The winding layout can be executed in several ways in order to minimize certain aspects such as parasitic elements and ac resistance, as discussed in [23]. In the present work, it was defined that the windings would be vertical, since it reduces the number or layers when compared to a horizontal approach. Also, it was chosen a interleaved winding strategy, where the layers alternate between primary and secondary windings.

With the IT structure defined, it is necessary to establish the number of turns N_{L_s} for a required self inductance. In this case, it is necessary to say that a gap was used in the IT design, in order to increase the core's material resistance to saturation by increasing the reluctance, which is approximately given by:

$$\mathfrak{R} = \frac{2g}{\mu_0 A_e}, \tag{3.5}$$

which was adapted from [43]. In the optimization routines, the gap was evaluated from 0.1 mm to 2 mm. That said, the addition of a gap to the IT changes reduces the permeability of the core assembly. The effective permeability of the gapped core is given by:

$$\mu_{eff} = \frac{1}{\dfrac{1}{\mu_r} + \dfrac{1}{l_c/2g}}. \tag{3.6}$$

Therefore, the required number of turns N_{L_s} for a given L_s is given by:

$$N_{t,L_s} = \sqrt{L_s \mathfrak{R} \left(1 + \frac{\mu_{eff}}{\mu_r}\right)}. \tag{3.7}$$

Regarding the core's saturation, manufacture's of ferrite cores provide the maximum magnetic flux density the material can handle before saturation, denoted by B_{sat}. In the optimization process, the maximum magnetic flux density in the ITs is assessed through the expression:

$$B_{max,L_s} = \frac{N_{t,L_s} I_{max,L_s} A_e}{\mathfrak{R}}, \tag{3.8}$$

which is then compared to B_{sat} to exclude unfeasible designs from the process.

Regarding the windings contraints, the current density and the window utilization factor are both determined using the same process for the boost inductor. On the other hand, the number of layers per winding is given by:

$$n_l = \text{ceil}\left(\frac{2 N_{t,L_s} r_{awg}}{w_h}\right), \tag{3.9}$$

where w_h is the window height.

3.3 POWER LOSS MODEL

3.3.1 Losses on switching devices

Switching devices power losses depend on the technology considered, so in this work only SiCFET (silicon carbide FETs) power losses are going to be assessed. In this context, the power losses on SiCFETs, as for any semiconductor device, can be divided into two categories: conduction and switching. The conduction losses, which occur during an operating state of the switching device, can be numerically assessed by:

$$P_c = R_{ds,on}\, I_{s,rms}^2, \tag{3.10}$$

where $R_{ds,on}$ is the resistance between drain and source during conduction stage for a specific temperature and $I_{s,rms}$ is the rms current in the switching device with respect to a mains period, which is numerically assessed as described in Algorithm 1.

Given the distinctive current distribution among the semiconductor devices within a single phase leg of the T-Type interleaved converter, it is necessary to determine the current of each device separately in order to assess conduction power losses accurately.

Regarding the switching losses, the energy spent during the turn-on and turn-off switching processes must be determined for the device's operational current and voltage range. This information can be obtained through double-pulse tests but can also be provided by suppliers. Figure 3.2 exemplifies the turn-on and turn-off energies for the operational range of the E3M0075120K SiCFET (Wolfspeed), which was chosen for the S_{x1} and S_{x3} semiconductor devices. As for the S_{x2} and S_{x4}, the UF3C065080K4S SiCFET (UnitedSiC) was chosen.

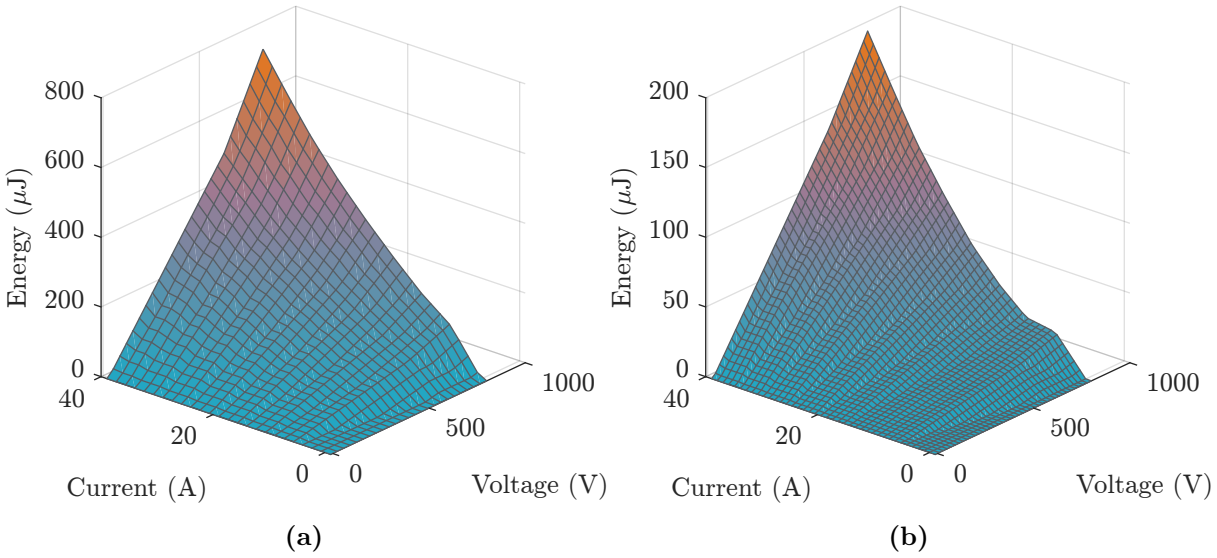


Figure 3.2 – Switching energy: turn-on (a) and turn-off (b) energy for the E3M0075120K (Wolfspeed) SiCFET given by the manufacturer.

To encompass for the operational points that are not provided by the suppliers,

a fitting through linear interpolation is performed to obtain a surface as depicted in Figure 3.2. With this information, it is necessary to identify the instantaneous current on the devices for every switching event over a mains period, as illustrated in Figure 3.3.

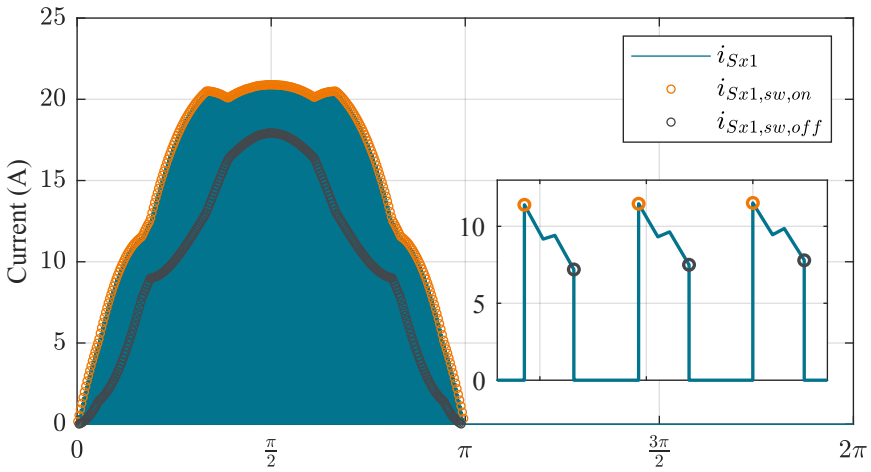


Figure 3.3 – Current i_{Sx1} highlighting the instantaneous current during off-to-on state transition and vice -versa. The zoomed image show in detail i_{Sx1} during three switching periods.

By analyzing the switching energy and the instantaneous current flowing through each device in the converter during switching, we can determine the total energy lost $(E_{sw,on} + E_{sw,off})$ for each switching period. Consequently, the average switching power loss for every switching period in a mains cycle can be calculated using the expression:

$$P_{sw} = f_s(E_{on,total} + E_{off,total}). \tag{3.11}$$

The switching power losses for each switching period in S_{x1} are illustrated in Figure 3.4, showcasing the contributions of both the off-to-on state transition power loss $(P_{sw,on})$ and vice versa $(P_{sw,off})$. It's important to note that, for a mains cycle, the switching power loss of interest is the average value of P_{sw}, denoted by $P_{sw,avg}$.

3.3.2 Power losses in magnetic elements

The power losses in magnetic elements are divided into the losses originated from the magnetic material that constitutes the core and from the winding. To assess the core losses in a magnetic element, the most common method is the Generalized Steinmetz Equation (GSE) [44], which is given by:

$$P_{GSE} = k_c f^{\alpha} B_p^{\beta}, \tag{3.12}$$

where P_{GSE} is the volumetric power losses, which depends on the frequency f and B_p, the peak value of the magnetic flux density. The parameters k_c, α and β are dependent on the material of the core and the temperature and are generally found empirically.

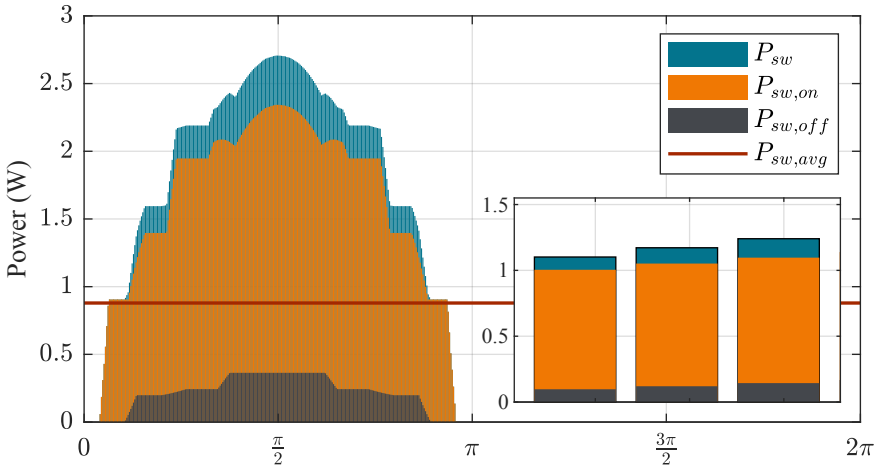


Figure 3.4 – Contributions of off-to-on and on-to-off state transitions power losses to the total power loss during each switching period for $S_{x,1}$ considering the E3M0075120K SiCFET (Wolfspeed) energy curves. The zoomed image shows the evolution of the power loss contributions through the mains period.

The GSE provides a good assessment to the core losses when the magnetic flux density is approximately sinusoidal. When the currents are not purely sinusoidal, i.e. when there are a considerable amount of harmonic content, the GSE cannot be relied. To get around this limitation, the improved GSE (iGSE) was developed, and is given by:

$$P_{iGSE} = \frac{1}{T}\int_0^T k_i \left|D_t B\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt, \tag{3.13}$$

where ΔB is the peak to peak flux variation and k_c, α and β are the same parameters used in the GSE, and k_i is calculated through the expression:

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int\limits_0^{2\pi} 2^{\beta-\alpha}|\cos(\theta)|^{\alpha} d\theta}. \tag{3.14}$$

The cores suppliers often provide volumetric power curves with respect to frequency or flux density, which can be used to determine the parameters k_c, α and β. As examples, Figure 3.5a shows the volumetric power losses for the N97 material for different operational temperatures [45] and Figure 3.5b shows the core power losses for the AmoFlux material under different frequencies [46].

To obtain the desired parameters from the material in Figure 3.5, the quadratic minimization method can be employed. The process was detailed in [47] and will not be covered in the present work. Hence, the application of the quadratic minimization for the N97 material considering $T = 100°C$ leads to $k_c = 0.036$, $\alpha = 1.735$ and $\beta = 2.448$, while for the AmoFlux material leads to $k_c = 18.382$, $\alpha = 1.355$ and $\beta = 2.214$.

For PFC rectifier applications, the magnetic material in the boost inductor is excited by a voltage composed by a sinusoidal low frequency component (typically 50 or 60

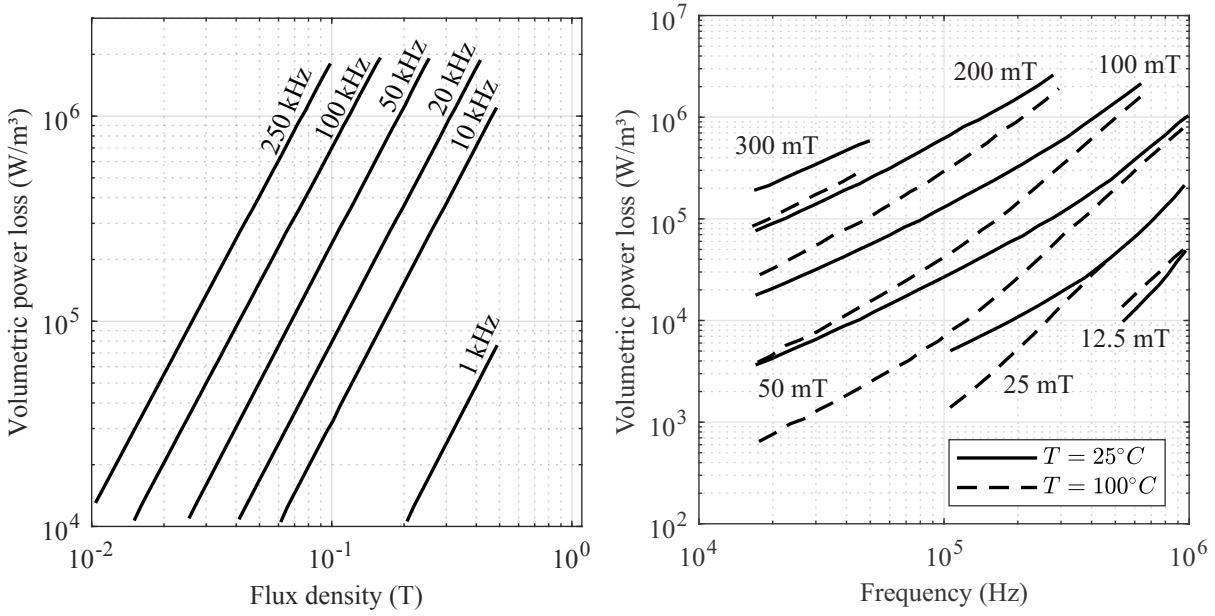


Figure 3.5 – Volumetric power loss: AmoFlux (a) and N97 (b).

Source: [45, 46].

Hz) and high frequency square-wave components originated from the switched operation of the converter. The low-frequency fundamental component generates a B-H curve that is called the major loop, while the high frequency components generates minor loops. Therefore, [39] proposed that the power loss in the major loop can be calculated through Equation 3.12, while for the high frequency component, it is proposed that its waveform is divided into piecewise linear segments and the loss associated to each segment is calculated as part of the energy associated to a minor loop. Note that this method does not consider how the minor loops close. To calculate the power losses associated to each segment in the high frequency component, [39] proposes the improved iGSE (i²GSE), which considers the effect of the relaxation of the magnetic material in the power losses.

Since the i²GSE is a method that requires further experimental testing of the core materials to obtain a loss map, this method will not be used in the present work. Alternatively, the piecewise evaluation of the high frequency power losses will be applied to the iGSE method, resulting in the following expression:

$$P_{pw,iGSE} = f_m \sum_{k=1}^{n_s} k_i \left|\Delta B_k\right|^{\beta} (\Delta t_k)^{1-\alpha}, \tag{3.15}$$

where ΔB_k is the peak-to-peak flux density variation during the time interval Δt_k, and n_s is the number of piecewise linear segments in the mains period.

Regarding the winding losses, it can be categorized into two sources of losses: skin effect and proximity effect. The skin effect is caused by the self-induced magnetic field

associated to an alternating current passing through a conductor. The electric field that is induced inside the conductor results in a current that counteracts the excitation current in the center of the conductor, causing the majority of the current to flow through an outer layer of the conductor. The skin-effect losses encompass the losses caused by the flowing current in a conductor and the self-induced eddy currents, and thus, it includes the DC losses. The skin effect losses are numerically assessed by:

$$P_{skin} = F_r(f) R_{DC} \left(I_p\right)^2, \tag{3.16}$$

where R_{DC} is the DC resistance, I_p is the peak current and $F_r(f)$ is a factor that represents the ratio between the AC and DC resistance of the conductor for the frequency f and it depends on the type of conductor.

For the present work, only round conductors were considered. To encompass for the litz wires, the effective wire diameter is given by:

$$\xi = \left(\frac{\pi}{4}\right)^{0.75} \frac{d}{\delta_w} \sqrt{\frac{d}{p_w n_w}}, \tag{3.17}$$

where d is the wire diameter, p_w is the pitch between paralleled strands, n_w is the number of parallel strands and δ_w is the skin depth, given by:

$$\delta_w = \sqrt{\frac{\rho_w}{\pi f \mu_r \mu_0}}. \tag{3.18}$$

In Equation 3.18, ρ_w is the conductor material resistivity, μ_0 is the vacuum permeability ($\mu_0 = 4\pi.10^{-7} N.A^{-2}$) and μ_r is the relative permeability, which can be assumed as one for conductor materials [48, 39].

Finally, the skin effect contribution in winding losses for litz wires can be calculated by:

$$P_{nw,skin} = n_w F_r(f) R_{DC} \left(\frac{I_p}{n_w}\right)^2, \tag{3.19}$$

where $F_r(f)$ is given by:

$$F_r = \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right). \tag{3.20}$$

The terms ber_k and bei_k are Kelvin functions of k-th order.

Regarding the proximity effect losses, the Dowell's approximation was considered. Hence, the proximity effect losses can be approximated by:

$$P_{nw,prox} = n_w G_r(f) R_{DC} \left(\frac{I_p}{n_w}\right)^2. \tag{3.21}$$

The term $G_r(f)$ is calculated through the expression:

$$G_r = \xi \frac{2({n_l}^2 n_w - 1)}{3} \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) - \cos(\xi)}, \tag{3.22}$$

where n_l is the number of layers in the same winding.

Literature [39, 49] provides more precise methods for proximity effect power loss calculation, however, those methods require the magnetic field calculation for each wire, which was considered out of the scope of this work. Moreover, even though the power loss value calculated through Dowell's approximation is much larger than the ones provided by the more precise methods, its tendency over frequency is the same, which allows its use for the purpose of optimization only.

3.4 THERMAL MODEL

To calculate the temperature rise given the winding losses P_w and core losses P_{co}, [44] proposed a simplified thermal model based on resistance network as illustrated in Figure 3.6. So, to obtain the temperature on the winding T_w and the temperature on the core T_c to a given room temperature T_∞, the resitances that compose the network must be described. In the present work, T_∞ was assumed to be 40°C.

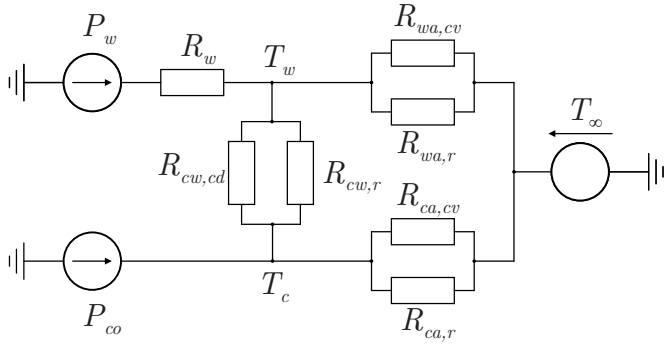


Figure 3.6 – Simplified thermal model based on resistance network

First, R_w models the conduction heat transfer between the copper windings to the copper coil surface, whose temperature is assume to be uniform for the sake of simplicity. This resistance represents the parasitic air gaps in the coil, and is expressed as:

$$R_w = \frac{g_w}{k_{tc}(A_{wc} + A_{wa})}, \tag{3.23}$$

where g_w is the equivalent air gap representing the in windings and between the winding and the coil-former, and k_{tc} is the air thermal conductivity, which is $k_{tc} = 0.031\,\mathrm{W/m} \cdot^\circ \mathrm{C}$ at 100°C and $k_{tc} = 0.026\,\mathrm{W/m} \cdot^\circ \mathrm{C}$ at 30°C. The terms A_{wc} and A_{wa} represent the area of contact between the winding and the core and the area of the winding directly exposed to the ambient air respectively.

The resistances $R_{cw,cd}$ and $R_{cw,r}$ represent the conduction and radiation heat transfer between the winding and the core respectively. The resistance $R_{cw,cd}$ is calculated through the expression:

$$R_{cw,cd} = \frac{g_{cw}}{k_{tc} A_{cw}}, \tag{3.24}$$

where g_{cw} is the equivalent air gap between the winding and the core.

Regarding $R_{cw,r}$, consider the following expression:

$$R_{cw,r} = \frac{T_w - T_c}{\epsilon_w \sigma (T_w^{\,4} - T_c^{\,4}) A_{cw}} \tag{3.25}$$

where ϵ_w is the emissivity of the winding surface and is assumed to be equal to 0.8 [44], and σ is the Stefan-Boltzman constant ($\sigma = 5.67.10^{-8}\,\mathrm{W/m^2 \cdot K^4}$).

The resistances $R_{wa,cv}$ and $R_{wa,r}$ represent the convection and the radiation heat transfer between the winding and the ambient air respectively. The resistance $R_{wa,cv}$ is calculated through:

$$R_{wa,cv} = \frac{1}{1.42 \left(\dfrac{T_w - T_\infty}{H_m} \right)^{0.25} A_{wa}}, \tag{3.26}$$

where H_m is the height of the magnetic component. The resistance $R_{wa,r}$ is given by:

$$R_{wa,r} = \frac{T_w - T_\infty}{\epsilon_w \sigma (T_w^{\,4} - T_\infty^{\,4}) A_{wa}}. \tag{3.27}$$

Similarly, The resistances $R_{ca,cv}$ and $R_{ca,r}$ represent the convection and the radiation heat transfer between the core and the ambient air and are expressed by:

$$R_{ca,cv} = \frac{1}{1.42 \left(\dfrac{T_c - T_\infty}{H_m} \right)^{0.25} A_{ca}} \tag{3.28}$$

and

$$R_{ca,r} = \frac{T_c - T_\infty}{\epsilon_w \sigma (T_c^{\,4} - T_\infty^{\,4}) A_{ca}}, \tag{3.29}$$

respectively.

Finally, to obtain the temperature rise, the resistance network depicted in Figure 3.6 with the known circuit laws for the unknown temperatures T_w and T_c.

3.5 OPTIMIZATION PROCESS

The optimization algorithm chosen for the present work was the Particle Swarm Optimization (PSO), which is supported in MATLAB®. The PSO algorithm is an evolutionary technique and thus is a population-based search algorithm, which is initialized with a population of random solution called particles. Each particle has an associated velocity, which is dynamically adjusted every iteration based on the particle behavior with

respect to the objective function, in order to make the swarm move towards the better search area in the process [50]. Literature present a variety of meta-heuristic optimization methods that could be used in place of the PSO, such as, Genetic Algorithm (GA), Ant Colony Optimizatiopn (ACO) and Cuckoo Search (CS) [51], however, its simplicity, low computational cost and convergence time were considered a fair trade-off for near-optima solutions.

In this study, a multi-objective optimization approach was utilized to optimize several parameters, namely the boost inductor self-inductance L_b, the self-inductance of the ITs L_s, and the IT gap g. First, the power losses in the switching devices are calculated. The magnetics evaluation conducted in each iteration is illustrated in Figure 3.7, where the feasibility constraints are employed to filter the search space for the desired results.

Note that the evaluation process can be employed for a database of different cores and switching devices in order to select the best combination of elements, but because of available materials, the present work focused on a single core for each magnetic element evaluation and preset semiconductor devices. Finally, the objective function of the optimization was formulated as the sum of all power losses modeled in the converter, which was minimized by the PSO algorithm.

Regarding the modulation considered for the optimization process, [22] conducts a comparative analysis of the SPWM, SVM, STHI and DPWM strategies.The analysis considers common mode voltage, boost inductor current oscillation, subtractive mode currents in interphase transformers, and current at the central point of the DC-link o as key metrics. Although the modulation schemes exhibit similar performance overall, each excels in specific aspects. Accordingly, STHI is selected for its ability to minimize current at the central point of the DC-link, resulting in reduced voltage oscillation across the DC-link capacitors.

The optimization results are depicted in Figure 3.8a for the boost inductor and Figure 3.8b for the interphase transformer (IT), using their respective chosen cores. The figures compare power losses and window utilization factor, which serves as a representative of the overall design volume since the core remains constant. In Figure 3.8a, all 283 designs feature $L_b = 40.12, \mu\text{H}$ but vary in winding design. Similarly, Figure 3.8b shows 203 resulting designs for $L_s = 224.52, \mu\text{H}$. In both figures, the Pareto front delineates the boundary of the design space and mark the global optima, where no point is better then another without a trade-off.

From Figure 3.8, it's evident that the chosen design from each optimization chart didn't prioritize minimizing power loss. Despite the potential for smaller losses, the optimal designs in both cases prioritize a larger k_w, necessitating parallel wire windings and increased copper usage in more intricate windings. However, less complex designs were selected with negligible impact on overall converter efficiency. Therefore, Figure 3.9a illustrates the boost inductor wound with 17 turns per winding using an 0088439A7 iron

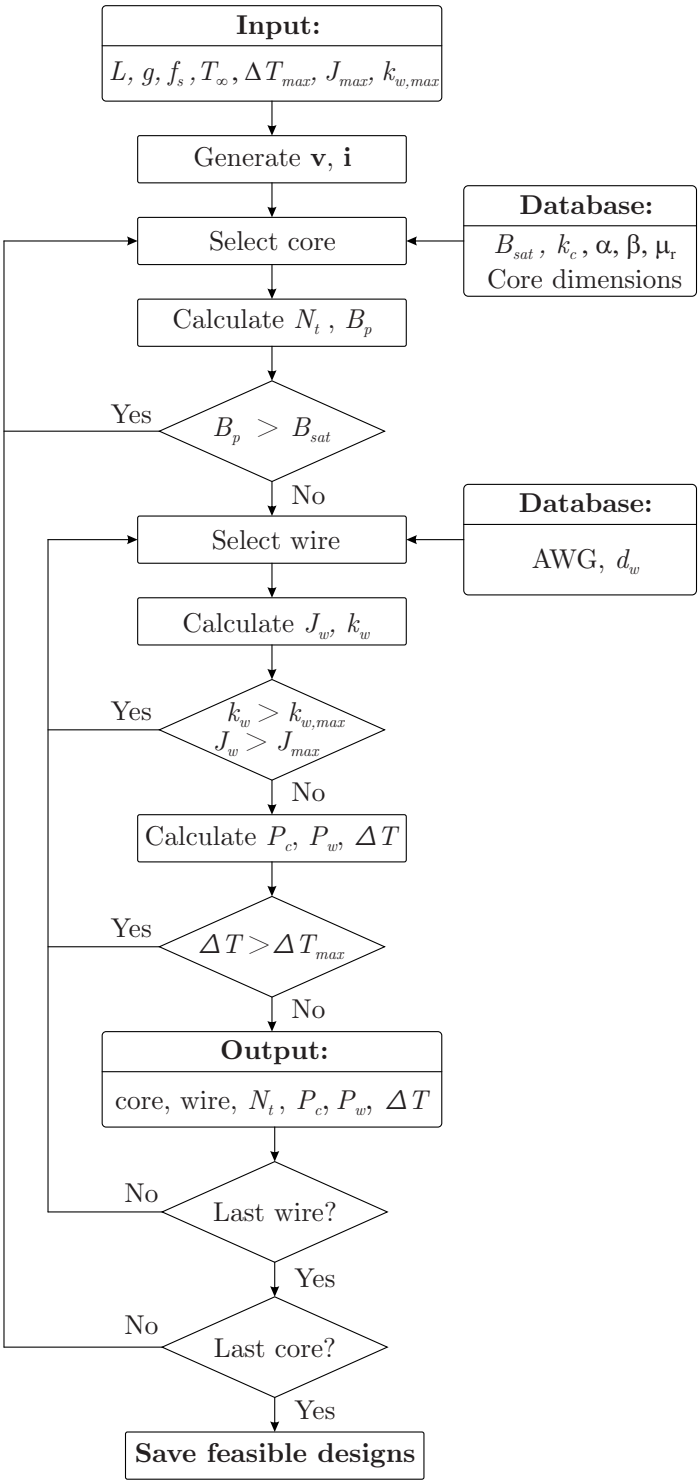


Figure 3.7 – Magnetic elements evaluation flowchart.

Source: Adapted from [23].

powder toroidal core. On the other hand, Figure 3.9b showcases the interphase transformer wound with 13.5 turns per winding for an EE 42/21/20 N97 ferrite core with a 0.1 mm gap. Both designs utilized AWG 15 wire and interleaved winding.

For comparison, the power loss model was adjusted to assess the boost inductor design with a single winding and an inductance of $2L_b$. Results are presented in Figure 3.10.

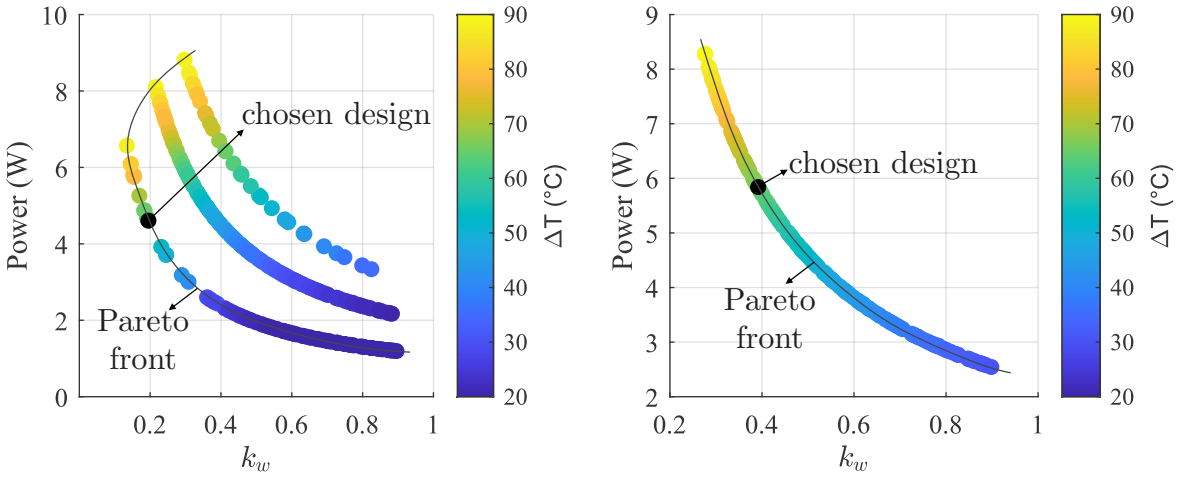


Figure 3.8 – Optimized designs for L_b (a) and L_s (b).

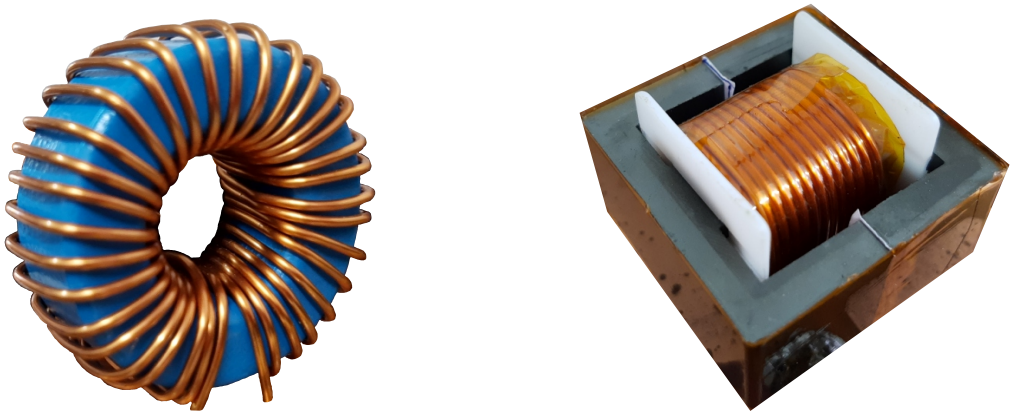


Figure 3.9 – Implemented boost inductor (a) and interphase transformer (b).

Notably, achieving the same power losses as the chosen coupled boost inductor design yields an expected k_w of approximately 0.75, significantly higher than the obtained value of around 0.2 for the coupled variation. This indicates a bulkier design with a single winding, potentially limiting for applications with weight and volume constraints. Additionally, the more compact designs in the optimal space exhibit higher temperature rises, which may pose additional application constraints.

In regards to the different modulation strategies, Figure 3.11 compares power losses in the selected optimal design across the different studied schemes, and displays power loss contributions and expected efficiencies for each modulation. While overall performance across strategies remains relatively consistent, it's notable that the DPWM scheme exhibited slightly better efficiency, attributed to lower power losses in the switching devices compared to other strategies.

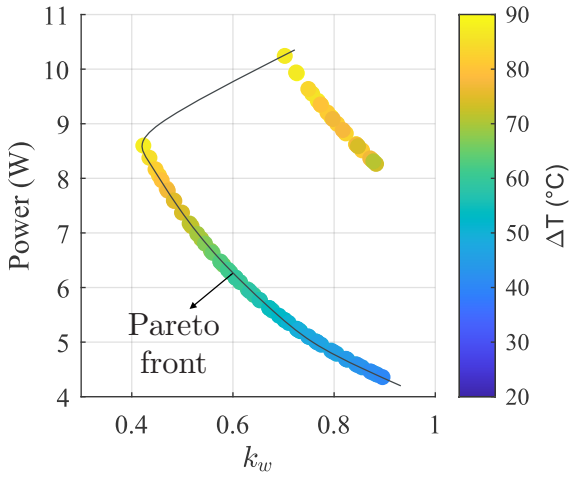


Figure 3.10 – Optimized designs for a single winding boost inductor.

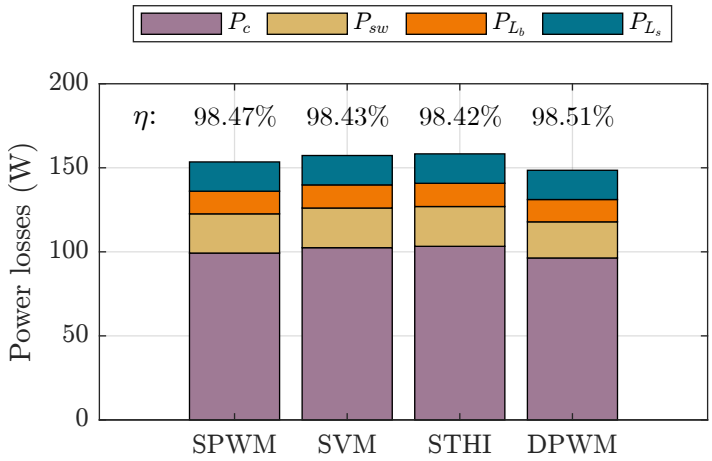


Figure 3.11 – Power losses comparison between different modulation strategies considering conduction (P_c) and switching losses (P_{sw}) in the semiconductors, losses in the boost inductors (P_{Lb}) and in the interphase transformers (P_{Ls}).

3.6 FILTER DESIGN

Once the boost inductor is defined, the next step is to address the differential mode low-pass filter, which will interface the converter with the mains. Typically, the filter's attenuation capability is directly proportional to its complexity. The literature presents three primary low-pass passive filter topologies: L, LC, and LCL configurations.

The L filter, a first-order filter, offers -20 dB/decade of attenuation across the entire frequency spectrum. It's ideal for applications employing high switching frequencies, where the required filter inductance is small, resulting in a more compact design. The LC filter, a second-order filter, provides -40 dB/decade of attenuation beyond its resonance frequency. On the other hand, the LCL filter, a third-order filter, offers -60 dB/decade of attenuation past its resonance frequency.

While LC and LCL filters offer higher attenuation, their resonance in the frequency response can cause operational instabilities in the converter, which can be avoided though

damping strategies. Literature suggests two damping methods: passive damping involves adding a resistive element to dissipate undesired high-frequency components, while active damping emulates a virtual impedance through additional control inputs. Ideally, both strategies complement each other for optimal resonance damping. However, due to the complexity involved, passive damping strategies are commonly preferred and implemented alone in such designs.

For practical applications, the implementation of a common-mode filter is mandatory to comply with regulatory standards. This filter is connected in series with the differential-mode filter and, due to leakage inductances, it can support the attenuation of the differential-mode filter. Additionally, the mains impedance should not be neglected when design a filter as it can be modeled as a resistor in series with an inductor. Considering these factors, it becomes apparent that the presence of inductances between the boost inductor and the actual mains voltage renders the filter equivalent to an LCL topology when employing an LC filter. Therefore, for the present work, the LC filter topology is chosen. Regarding the common-mode filter, as EMI compliance is not the focus of this work, the design of the LC common-mode filter utilized will not be addressed.

3.6.1 Filter capacitor

Given that capacitors are restricted to specific values by manufacturers, determining the filter capacitance is based on setting performance constraints and choosing a compliant particular solution. First, the capacitor should minimize voltage ripple at the converter's input to mitigate voltage stress on the semiconductor devices. [52]. Hence, the minimum filter capacitance can be assessed by:

$$C_{min} = \frac{\Delta I_{am,max}}{8 f_s \Delta V_{in,max}}, \tag{3.30}$$

where $\Delta I_{am,max}$ is the maximum current ripple in the filter, f_s is the switching frequency and $\Delta V_{in,max}$ is the maximum voltage ripple in the converter output [52]. The designed boost inductors provides $\Delta I_{am,max} = 10.83$ A, and assuming that $\Delta V_{in,max}$ is 10% of the peak rated phase voltage, yields $C_{min} = 2.15\,\mu$F.

To prevent the significant decrement of the converter's power factor in light load situations, a maximum reactive power can be defined as a fraction of the rated active power. Therefore, the maximum filter capacitance is given by:

$$C_{max} = \frac{k_S P_r}{6\pi f_m V_{rms}^2}, \tag{3.31}$$

where k_S denotes the active power fraction that represents the maximum reactive power, which was considered to be 0.05 [53]. The parameters assumed for this filter design yield $C_{max} = 27.41\,\mu$F.

Regarding the filter's resonance frequency, in order to prevent the fundamental frequency attenuation, and at the same time, provide sufficient attenuation for the high frequency components, [35] suggests to impose the constraint given by:

$$10f_m \leq f_{res} \leq f_{1h}/2, \tag{3.32}$$

where f_{1h} is the frequency of the first harmonic originated from the switching process. In the case of the design parameters, $f_{1h} = 2f_s = 70$ kHz.

Based on the defined constraints, the filter capacitance was set to 2.2 μF. This specific capacitance value results in $f_{1h}/f_{res} = 5.79$.

3.6.2 Damping branch

To passively dampen the LC filter resonance, literature primarily suggests three methods [54, 55]. The first involves adding a damping resistor in parallel with the filter capacitor, which subjects it directly to mains voltage, resulting in excessive losses. The second method incorporates another capacitor in series with the damping resistor. When appropriately designed, this capacitor serves as high impedance to low-frequency grid components and low impedance to high-frequency components requiring damping. The third method employs an inductor in series with the boost inductor and a damping resistor in parallel. However, this strategy introduces additional lossy components, as line current passes through the damping inductor. In this work, it was adopted the parallel RC branch strategy, illustrated in Figure 3.12. In this figure, L_1 represents the additive mode equivalent boost inductance, C_1 denotes the filter capacitor, R_d is the damping resistor, C_2 represents the damping branch capacitor, L_2 stands for common mode inductor leakage inductance (assumed to be 1 μH), while R_m and L_m characterize the mains impedance.

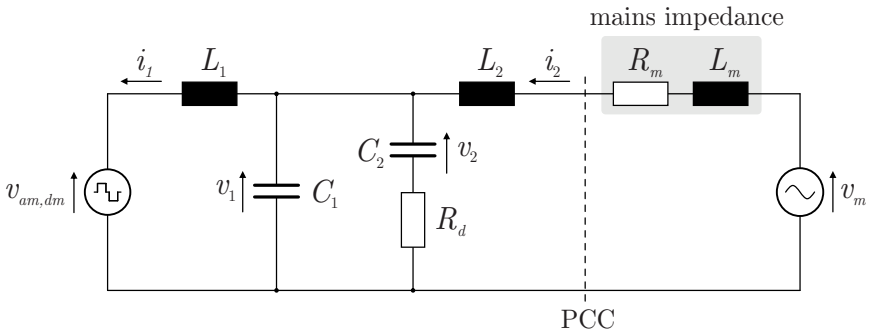


Figure 3.12 – Phase equivalent of the chosen filter topology.

The resonance gain and frequency of the equivalent filter are influenced by several parameters, including the damping branch capacitance, resistance, and mains impedance. Therefore, to analyze the effect of these parameters on the filter resonance, they must be defined. Initially, the damping branch filter capacitor C_2 is defined as proportional to the filter capacitance C_1 by a factor of α_c, such that $C_2 = \alpha_c C_1$.

The mains impedance can be evaluated using the short circuit ratio (SCR) at the point of common coupling (PCC), defined by:

$$SCR = \frac{S_{sc}}{S_r} = \frac{V_m^2}{|Z_m|\, S_r} \quad \therefore \quad SCR = \frac{1}{|Z_{m,pu}|}. \tag{3.33}$$

Here, S_{sc} represents the short-circuit apparent power at the PCC, S_r denotes the apparent rated power of the converter, and $Z_{m,pu}$ denotes the line impedance in per unit (p.u.) [56, 57].

Referring to Equation 3.33, establishing the line voltage at the generator as the base voltage and the rated active power at the PCC as the base power leads to the derivation of:

$$Z_b = \frac{V_b^2}{S_b} = \frac{3V_{rms}^2}{P_r} \quad \therefore \quad SCR = \frac{|Z_m|}{Z_b} = \frac{\sqrt{R_m^2 + (\omega_m L_m)^2}}{Z_b}. \tag{3.34}$$

For estimating mains impedance, it is reasonable to assume a proportional relationship between the resistive and reactive components of the impedance, expressed as $k_m R_m = \omega_m L_m$, where k_m denotes this proportion. Given that the mains grid typically exhibits significant inductive behavior, it is chosen $k_m = 4$ in this study.

To design an effective damping branch, it's essential to analyze the system's frequency response to assess the resonance magnitude and frequency. Therefore, considering the phase equivalent in Figure 3.12, the state-space model of the system is described by:

$$\begin{cases} D_t\, \mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B} v_{am,dm} + \mathbf{E} v_m \\ \mathbf{y} = \mathbf{C}\mathbf{x} \end{cases} \tag{3.35}$$

where

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & -\frac{R_m}{L_2 + L_m} & -\frac{1}{L_2 + L_m} & 0 \\ -\frac{1}{C_1} & \frac{1}{C_1} & -\frac{1}{R_d C_1} & \frac{1}{R_d C_1} \\ 0 & 0 & \frac{1}{R_d C_2} & -\frac{1}{R_d C_2} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} -\frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \mathbf{E} = \begin{bmatrix} 0 \\ \frac{1}{L_2 + L_m} \\ 0 \\ 0 \end{bmatrix} \quad \mathbf{C} = \mathbf{I}_4$$

In this model, the additive differential mode voltage $v_{am,dm}$ serves as the internal input, the mains voltage v_m acts as the external input, and $\mathbf{x}$ represents the state vector, defined as $\mathbf{x} = [i_1, i_2, v_1, v_2]^T$.

From Equation 3.35, the frequency response can be analyzed through the system transfer functions with:

$$G(s) = \mathbf{C}(s\, \mathbf{I}_4 - \mathbf{A})^{-1}\mathbf{B}. \tag{3.36}$$

To inspect the resonance peak of the filter, the transfer function from the mains side

current i_2 with respect to the system input $v_{am,dm}$ is going to be considered.

By varying the parameters of interest and observing the magnitude of the resonance in the system, yields Figure 3.13. From Figure 3.13a, where it was arbitrarily chosen $\alpha_c = 1$, it can be seen that the resonance point has a strong dependency on the grid impedance, whereas in Figure 3.13b, where $SCR = 10$ it can be seen that the proportionality factor α_c present a weaker influence on the resonance magnitude of the system for $\alpha_c \geq 1$. In this situation, it was decided to keep $\alpha_c = 1$ as commonly done in literature.

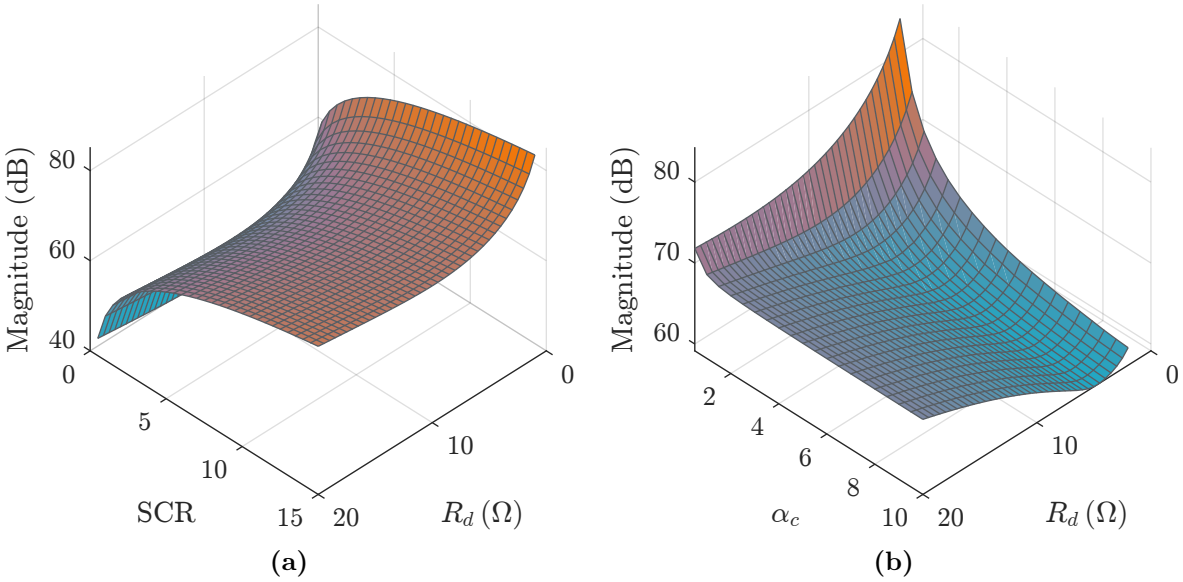


Figure 3.13 – Magnitude of the system resonance for $\alpha_c = 1$ (a) and for $SCR = 10$ (b).

In this scenario, to chose the damping resistance it is still necessary to truncate the degrees of freedom in the filter design and to chose an SCR value. Therefore, considering grid-connected application in urban centers, it is expected a strong grid behavior in the PCC. According to [57], an arbitrary point in an AC system is considered weak if its SCR is between 2 and 3. Systems with SCR bellow this interval are classified as very weak, whereas systems with SCR greater then 3 are classified as strong. Therefore, for this work it will be considered an SCR of 6.

With the damping branch capacitance and mains impedance defined, the next step is to calculate the damping resistance. Figure 3.14 illustrates the effect of R_d in the filter resonance magnitude. It can be seen that for a null value of R_d, the equivalent filter resonance is the parallel equivalent between C_1 and C_2, while for an infinite damping resistance, the damping branch is removed from the filter. Both situations result on undamped systems, indicating that an optimal value of R_d can be found which will result in the minimum resonance magnitude for the parameters considered.

To obtain the optimal value of R_d, the method employed in this work is described in Algorithm 3. One should note that the algorithm is simply an iterative loop that evaluates the magnitude of the frequency response at resonance for multiple values of R_d within an predefined interval and it returns the value of R_d that corresponds to the minimum

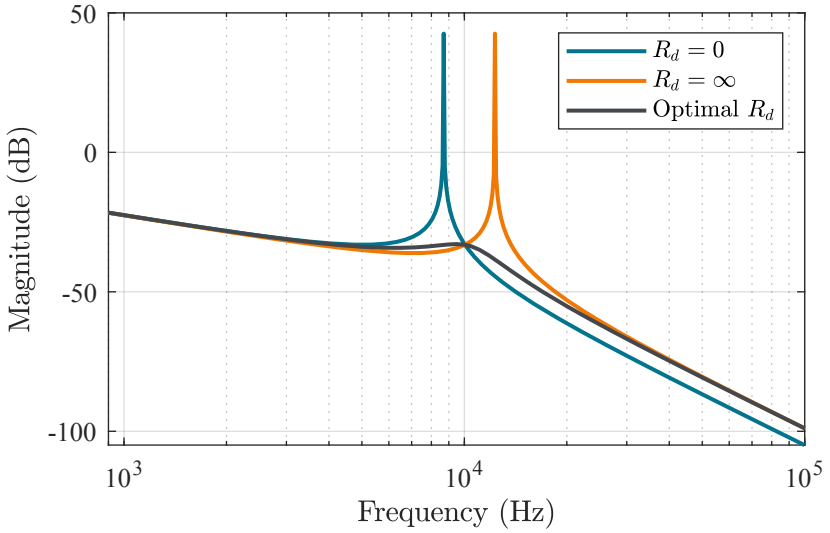


Figure 3.14 – Frequency response of the filter for $SCR = 6$, α_c =1 and different values of R_d.

magnitude at resonance. The boundaries of the vector with the values of R_d used for the analysis were empirically defined.

Algorithm 3 Optimal damping resistor R_d.

Input: State space matrices of the system **A**, **B** and **C**;
Output: Optimal value of R_d;
$R_{d,vec} \leftarrow 0.1 : 0.01 : 20$;
for $k \leftarrow 1$ **to** length$(R_{d,vec})$ **do**
    $R_d \leftarrow R_{d,vec}(k)$;
    $G(s) \leftarrow \mathbf{C}(s\,\mathbf{I}_4 - \mathbf{A})^{-1}\mathbf{B}$;
    $[mag, \omega] \leftarrow$ bode$(sG(s))$;
    $ResMag(k) \leftarrow \max(mag)$;
end for
$[-, index] \leftarrow \min(ResMag)$;
$R_{d,opt} \leftarrow R_{d,vec}(index)$;

Hence, the optimal value of R_d for the damping branch is determined as $R_d = 10.17, \Omega$. The inclusion of the damping branch shifts the resonance frequency to 9.959 kHz. Nevertheless, as this value complies to the constraint specified in Equation 3.32, the damping branch design is deemed acceptable. One may observe that the design of R_d did not take into account the power losses in these components, despite the proposed filter aiming for improved efficiency. This oversight stems from the significantly low power losses in this component when compared to the converter's rated power.

3.6.3 Final filter topology

With all the passive elements that compose the filter properly designed, the final filter topology is depicted in Figure 3.15, where L_{sm} represents the interphase transformers,

L_{am} represents the coupled boost inductors, C_1 is the filter capacitance, C_2 and R_d are the damping branch capacitor and resistor respectively, L_2 is a three-phase common mode choke and C_3 and $R_{d,cm}$ are the common mode damping branch capacitor and resistor respectively. As previously stated, the common mode filter was not designed as EMC is out of the scope of this work, and therefore, the components were chosen based on literature [23]. In this scenario, the common mode choke used is a commercial model 6123-X140 (Vacuumschmelze). As for the common mode damping branch, it was chosen $C_3 = 2.5\,\text{nF}$ and $R_{d,cm} = 1.1\,\Omega$.

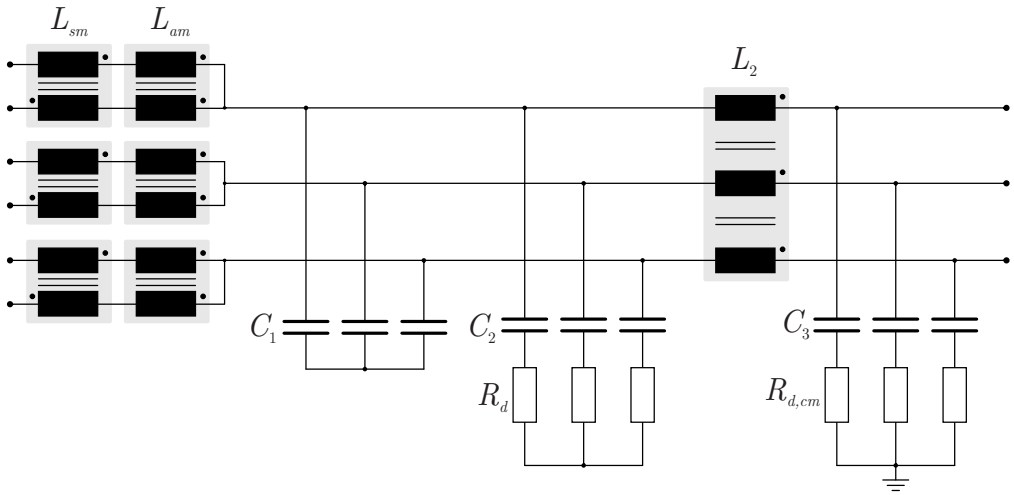


Figure 3.15 – Complete filter topology.

3.7 CONCLUSION

This chapter outlines the method for designing the passive components of the low-pass filter connecting the interleaved T-Type converter and the mains. The optimization routine used for designing the boost inductor and interphase transformer integrates established power loss models from the literature into a simple algorithm. This approach yields optimally efficient designs, making it valuable for industrial applications where efficiency, size, and weight are critical constraints.

The proposed method's expected drawback lies in its thermal model, which may introduce significant errors in estimating the practical temperature of magnetic elements. This model simplifies the heat transfer process for the magnetic element's geometric structure, potentially leading to inaccuracies. Developing a high-fidelity thermal model would be complex and demand substantial computational resources for optimization, which wasn't the focus of this work. Consequently, the employed thermal model serves as a useful tool for initial temperature estimation of magnetic elements and is deemed sufficient for optimization purposes.

Concerning the filter frequency performance, it was demonstrated that it depends on various parameters, with mains impedance being perhaps the most critical since it cannot

be directly controlled but only estimated. In this context, changes in the SCR at the PCC lead to variations in the resonance attenuation of the filter, potentially destabilizing the converter. To mitigate this problem, the control design involves narrowing the bandwidth of the current control to enhance converter robustness at the expense of rapid performance. This aspect will be further elaborated in the following chapter.

Chapter

4 Modeling and control design

4.1 INTRODUCTION

In previous analysis in Chapter 2, it was demonstrated that the T-Type interleaved converter can be studied by decoupling its current components into additive and subtractive modes. The additive mode corresponds to processed power in the converter, while the subtractive mode is associated to circulating currents among the respective phases of the interleaved modules.

Concerning the additive mode, control can be executed through a cascaded control scheme, typically with the DC-link control loop as the outer loop, a method extensively documented in the literature. However, in addressing the subtractive mode, conventional practice involves employing passive mitigation structures solely with the Interleaved Transformers (ITs), neglecting potential asymmetries within the ITs that could lead to imbalanced power distribution among phases. Thus, alongside the ITs, integrating a control loop becomes necessary to ensure equal power distribution within the converter.

Furthermore, controlling the DC-link voltage is not sufficient in guaranteeing voltage balance among the DC-link capacitors. Consequently, a dedicated control loop is necessary to generate a common-mode component (gamma/0-axis) to offset any imbalances in the DC-link capacitors' voltages, thereby resulting in a hybrid approach.

It is evident that operating the T-Type interleaved converter effectively demands the simultaneous operation of several control loops. Consequently, this chapter aims on the control-oriented modeling of the T-Type converter and propose a control scheme that meets the desired performance criteria. The coupled boost variation of the converter will be considered.

4.2 INTERLEAVED T-TYPE CONVERTER MODEL

4.2.1 Equivalent circuits for additive and subtractive modes

Previous analysis over the IT + coupled boost and operation as a PFC rectifier served to obtain the converter's equivalent circuits for the additive mode and subtractive mode. Recalling Equation 2.41, repeated here for clarity

$$v_{xo}\boldsymbol{\lambda} = \mathbf{L}_{sm,am,bs}\, D_t\, \mathbf{i}_{sm,am,x} + \mathbf{R}_{w,bs}\ \mathbf{i}_{sm,am,x}, \tag{4.1}$$

where $\boldsymbol{\lambda} = [0 \dots 1]^T_{1\times n}$,

$$\mathbf{L}_{sm,am,bs} = \begin{bmatrix} \dfrac{(n-2)\,L_b + n\,L_s}{n-1}\,\mathbf{I}_{(n-1)\times(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & 2\,L_b \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{sm\,(n-1)\times(n-1)} & \mathbf{0}_{(n-1)\times 1} \\ \mathbf{0}_{1\times(n-1)} & L_{am} \end{bmatrix}, \tag{4.2}$$

and

$$\mathbf{R}_{w,bs} = \begin{bmatrix} r_{w,bs} & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & r_{w,bs} \end{bmatrix}. \tag{4.3}$$

Applying the dynamic average operator M_{T_s} over Equation 4.1 and substituting the dynamic average of $v_{i,xo}$, given by

$$M_{T_s}(v_{i,xo}) = \frac{v_{dc}}{2}\, m_{i,x} \left(1 + \frac{\Delta v_{dc}}{v_{dc}} \text{sign}\,(m_{i,x})\right), \tag{4.4}$$

yields

$$M_{T_s}\begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ v_{xo} \end{bmatrix} = M_{T_s}\begin{bmatrix} v_{1,x,sm} \\ v_{2,x,sm} \\ \vdots \\ v_{n-1,x,sm} \\ v_{x,am} \end{bmatrix} + \frac{v_{dc}}{2}\begin{bmatrix} d_{1,x,sm} \\ d_{2,x,sm} \\ \vdots \\ d_{n-1,x,sm} \\ d_{x,am} \end{bmatrix}, \tag{4.5}$$

where the following variable exchange was adopted

$$d_{i,x} = m_{i,x} \left(1 + \frac{\Delta v_{dc}}{v_{dc}} \text{sign}\,(m_{i,x})\right). \tag{4.6}$$

From Equation 4.5 it can be concluded that the average value of the voltage across T_x for each subtractive mode equivalent is given by:

$$M_{T_s}(v_{i,x,sm}) = -\frac{v_{dc}}{2}\, d_{i,x,sm}, \tag{4.7}$$

while for the additive mode results the relation expressed by:

$$M_{T_s}(v_{xo}) = \langle v_{x,am} \rangle + \frac{v_{dc}}{2}\, d_{x,am} \tag{4.8}$$

By comparing the last results with Equation 4.1, it can be concluded that $n-1$ subtractive mode equivalent circuits and one additive mode equivalent circuit can be derived per phase, as given by Equation 4.9 and Equation 4.10 respectively, with $n \neq 1$.

$$-\frac{v_{dc}}{2}\, d_{i,x,sm} = \frac{(n-2)\, L_b + n\, L_s}{n-1}\; D_t\left(M_{T_s}(i_{i,x,sm})\right) + r_{w,bs}\, M_{T_s}(i_{i,x,sm}) \tag{4.9}$$

$$M_{T_s}(v_{xo}) = 2L_b\, D_t\left(M_{T_s}(i_{x,am})\right) + r_{w,bs}\, M_{T_s}(i_{x,am}) + \frac{v_{dc}}{2}\, d_{x,am} \tag{4.10}$$

Therefore, Figures 4.1 and 4.2 illustrate the decoupled three-phase additive and subtractive mode equivalent circuit models respectively. Is should be noted that the subtractive mode circuit represents the i-th equivalent circuit of each phase out of the $n-1$ subtractive mode circuits, as shown in Fig.Figure 4.2. Note that in the additive mode equivalent circuit, the components power losses were considered and added to the model as series resistances. Also, one should notice that the additive mode equivalent boost inductance was denoted by $L_1 = 2L_b$ and the common mode inductor leakage inductance was denoted as L_2, as adopted in Chapter 3.

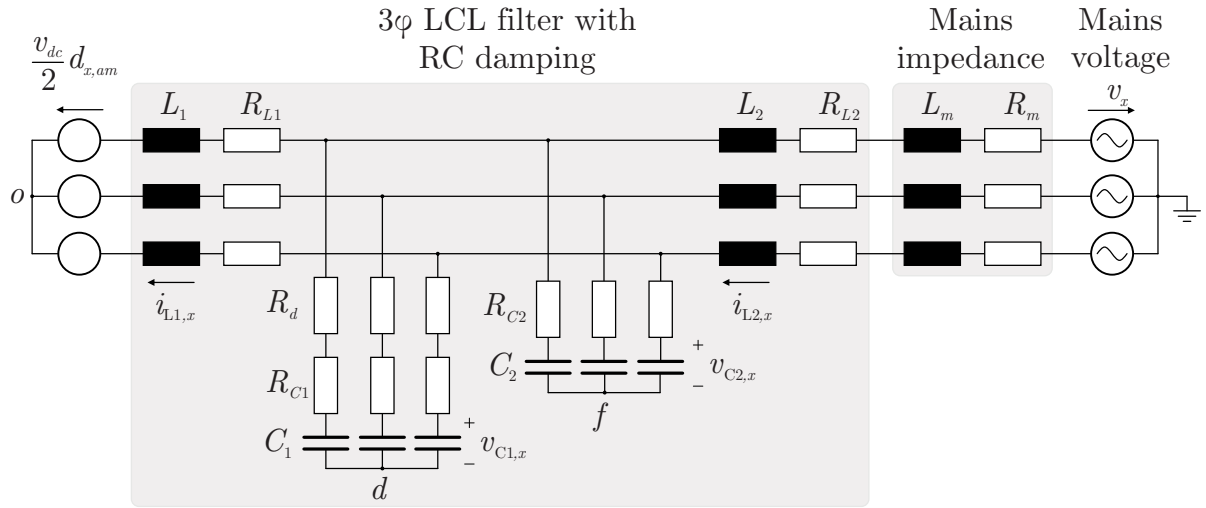


Figure 4.1 – Additive mode three-phase equivalent circuit.

4.2.2 DC-link analysis

Regarding the DC-link capacitors, applying Kirchoff's Current Law yields

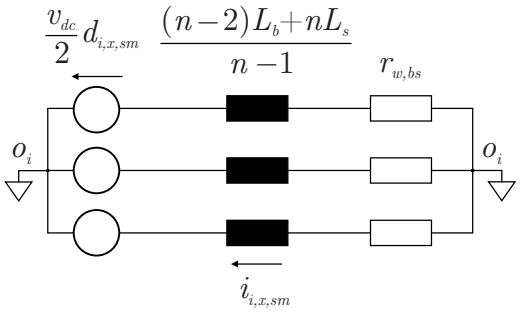


Figure 4.2 – Subtractive mode three-phase equivalent circuit.

$$\begin{aligned} C_b\, D_t v_{dc1} &= i_p - i_{dc} \\ C_b\, D_t v_{dc2} &= i_n - i_{dc}\,. \end{aligned} \tag{4.11}$$

Recalling the definitions $v_{dc} = v_{dc1} + v_{dc2}$ and $\Delta v_{dc} = v_{dc1} - v_{dc2}$ and substituting them into Equation 4.11 results

$$\begin{aligned} C_b\, D_t v_{dc} &= i_p + i_n - 2i_{dc} \\ C_b\, D_t \Delta v_{dc} &= i_p - i_n\,. \end{aligned} \tag{4.12}$$

Moreover, the switch-level current in the upper and lower branches in DC-side of the converter, i_p and i_n respectively, are given by

$$\begin{aligned} i_p &= \sum_{x=a,b,c} \sum_{i=1}^{n} S_{x1,i}\, \sigma(m_{i,x}) i_{i,x} \\ i_n &= -\sum_{x=a,b,c} \sum_{i=1}^{n} S_{x3,i}\, \overline{\sigma}(m_{i,x}) i_{i,x}\,. \end{aligned} \tag{4.13}$$

Substituting Equation 4.13 into Equation 4.12 results in the following equations

$$\begin{aligned} C_b D_t v_{dc} &= -2i_{dc} + \sum_{x=a,b,c} \sum_{i=1}^{n} \left[S_{x1,i}\sigma(m_{i,x}) - S_{3x,i}\overline{\sigma}(m_{i,x}) \right] i_{i,x} \\ C_b\, D_t \Delta v_{dc} &= \sum_{x=a,b,c} \sum_{i=1}^{n} \left[S_{1x,i}\sigma(m_{i,x}) + S_{3x,i}\overline{\sigma}(m_{i,x}) \right] i_{i,x}\,. \end{aligned} \tag{4.14}$$

Applying the dynamic average value operator M_{T_s} to Equation 4.14 results in Equation 4.15. In this equation, the dynamic average operator has been omitted for notation clarity. This omission will be maintained throughout the chapter, as all variables are assumed to represent their dynamic average values, unless stated otherwise. Additionally, the current supplied to the load connected to the DC-link, denoted as i_{dc}, has been replaced to model a constant power source with a rated power of P_r. The utilization of a constant power source in modeling the load aims to provide a more precise representation of the behavior of a DC-DC converter, which is typically linked to the DC-link in a two-stage rectifier/inverter configuration.

$$\begin{aligned} C_b\, D_t v_{dc} =& -2\,\frac{P_r}{v_{dc}} + \sum_{x=a,b,c}\sum_{i=1}^{n} d_{i,x}\left[1 - \frac{\Delta v_{dc}}{v_{dc}}\text{sign}\,(m_{i,x})\right] i_{i,x} \\ C_b\, D_t \Delta v_{dc} =& \sum_{x=a,b,c}\sum_{i=1}^{n} d_{i,x}\left[\text{sign}\,(m_{i,x}) - \frac{\Delta v_{dc}}{v_{dc}}\right] i_{i,x} \end{aligned} \tag{4.15}$$

The equations can be rewritten using matrix notation to encompass all three phases as follows

$$\begin{aligned} C_b\, D_t v_{dc} &= -2\,\frac{P_r}{v_{dc}} + \mathbf{d}_{3n,abc}^{\,T}\left[\mathbf{I}_{3n} - \frac{\Delta v_{dc}}{v_{dc}}\,\mathbf{M}\right]\mathbf{i}_{3n,abc} \\ C_b\, D_t \Delta v_{dc} &= \mathbf{d}_{3n,abc}^{\,T}\left[\mathbf{M} - \frac{\Delta v_{dc}}{v_{dc}}\,\mathbf{I}_{3n}\right]\mathbf{i}_{3n,abc}\,, \end{aligned} \tag{4.16}$$

where $\mathbf{M} = \text{diag}\,(\text{sign}\,(\mathbf{m}_{3n,abc}))$.

Changing the state variables to additive and subtractive mode through Lunze's Transformation yields

$$\begin{aligned} C_b\, D_t v_{dc} =& -2\frac{P_r}{v_{dc}} + \mathbf{d}_{3n,sm,am}^{\,T}\left(\mathbf{I}_3 \otimes \mathbf{\Gamma} - \frac{\Delta v_{dc}}{v_{dc}}\mathbf{\Lambda}\right)\mathbf{i}_{3n,sm,am} \\ C_b\, D_t \Delta v_{dc} =& \mathbf{d}_{3n,sm,am}^{\,T}\left(\mathbf{\Lambda} - \frac{\Delta v_{dc}}{v_{dc}}\mathbf{I}_3 \otimes \mathbf{\Gamma}\right)\mathbf{i}_{3n,sm,am}\,. \end{aligned} \tag{4.17}$$

where

$$\mathbf{\Gamma} = \begin{bmatrix} \mathbf{1}_{n-1} + \mathbf{I}_{n-1} & \mathbf{0}_{n-1\times 1} \\ \mathbf{0}_{1\times n-1} & n \end{bmatrix} \tag{4.18}$$

and

$$\begin{aligned} \mathbf{\Lambda} &= (\mathbf{I}_{3n} \otimes \mathbf{T}_L^{-1})^T \mathbf{M}\,(\mathbf{I}_{3n} \otimes \mathbf{T}_L^{-1}) \\ \therefore \mathbf{\Lambda} &= \begin{bmatrix} \text{sign}\,(m_a) & 0 & 0 \\ 0 & \text{sign}\,(m_b) & 0 \\ 0 & 0 & \text{sign}\,(m_c) \end{bmatrix} \otimes \mathbf{\Gamma} \end{aligned} \tag{4.19}$$

In the definition of $\mathbf{\Lambda}$, the differences between the modulation signals of the same phase were assumed negligible, leading to a single modulation signal for each phase.

The application of $\mathbf{T}_L$ decouple each phase into additive and subtractive modes, which was rearranged in three-phase groups for application of Park's Transformation. The rearrangement follows the logic given by

$$\begin{aligned} \mathbf{d}_{3n,sm,am}^{T} &= [d_{1,sm,a}\ \ d_{2,sm,a} \ldots d_{am,a}\ \ d_{1,sm,b}\ \ d_{2,sm,b} \ldots d_{am,b}\ \ d_{1,sm,c}\ \ d_{2,sm,c} \ldots d_{am,c}]^T \\ &\downarrow \\ \mathbf{d}_{3n,sm,am}^{T} &= [d_{1,sm,a}\ \ d_{1,sm,b}\ \ d_{1,sm,c}\ \ d_{2,sm,a}\ \ d_{2,sm,b}\ \ d_{2,sm,c} \ldots d_{am,a}\ \ d_{am,b}\ \ d_{am,c}]^T \end{aligned} \tag{4.20}$$

Evidently, the matrices $\mathbf{I}_3 \otimes \mathbf{\Gamma}$ and $\mathbf{\Lambda}$ must also be reorganized to maintain the previous multiplication values unaltered. The reorganized matrices will be denoted as $(\mathbf{I}_3 \otimes \mathbf{\Gamma})_R$

and $\mathbf{\Lambda}_R$.

4.2.3 Control-oriented model

With the DC-side mathematically described, the AC-side can be analyzed directly through Kirchoff's Laws. Afterwards, Lunze's Transformation can be applied to obtain the decoupled system's equations. It must be noted the expression given by:

$$i_{L1,x} = n\, i_{x,am}, \tag{4.21}$$

which relates the current on the boost inductor equivalent L_1 and the additive mode currents on the IT windings $i_{x,am}$, which are going to be adopted as part of the control strategy.

Aiming the control feasibility of the converter, Park's Transformation (Equation 4.22) is applied to the model, resulting the set of differenctial equations expressed in Appendix B.

$$\mathbf{T}_P = \underbrace{\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{\text{Clarke's Transformation}} \underbrace{\begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{\text{Rotation of } \theta} \tag{4.22}$$

The conversion to $dq0$ frame causes a coupling between the axis that need to be addressed in order to obtain the desired transfer functions to design the controllers. The matrix $\mathbf{\Theta}$ represents the coupling between the d and q axis and is given by

$$\mathbf{\Theta} = \mathbf{T}_P\, D_t\, \mathbf{T}_P^{-1} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{4.23}$$

where ω is the angular frequency of the mains.

First, the continuous-time model of the T-Type interleaved converter can be described as

$$\begin{cases} D_t\, \mathbf{x} = f(\mathbf{x}, \mathbf{u}, \mathbf{w}) \\ \mathbf{y} = g(\mathbf{x}, \mathbf{u}, \mathbf{w}), \end{cases} \tag{4.24}$$

where $\mathbf{x} \in \mathbb{R}^{nx}$ is the state vector, $\mathbf{u} \in \mathbb{R}^{nu}$ is the input vector, $\mathbf{w} \in \mathbb{R}^{nw}$ is the disturbance vector. The variables n_x, n_u and n_w are the number of states, input variables and disturbances respectively. Finally, $\mathbf{y}$ is the output vector.

From Equation 4.24, the state-space continuous-time linear model of the T-Type interleaved converter is given by

$$\begin{cases} D_t\,\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{E}\mathbf{w} \\ \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} + \mathbf{F}\mathbf{w}, \end{cases} \tag{4.25}$$

where

$$\begin{aligned} \mathbf{A} &= \mathbf{J}_{\mathbf{x}}(f(\mathbf{x},\mathbf{u},\mathbf{w})) \\ \mathbf{B} &= \mathbf{J}_{\mathbf{u}}(f(\mathbf{x},\mathbf{u},\mathbf{w})) \\ \mathbf{E} &= \mathbf{J}_{\mathbf{w}}(f(\mathbf{x},\mathbf{u},\mathbf{w})), \end{aligned} \tag{4.26}$$

and $\mathbf{J}_{\mathbf{k}}$ is the Jacobian matrix with respect to the vector $\mathbf{k}$. For simplification, $\mathbf{C} = \mathbf{I}_{n_x}$ will be assumed, and $\mathbf{D} = 0$ and $\mathbf{F} = 0$ are observed for the considered system.

4.2.3.1 Decoupling strategy

In this scenario, the matrix A can be rewritten as $\mathbf{A} = \mathbf{A}_{dec} + \mathbf{A}_c$, the coupling between the axis is given by $\mathbf{A}_c$. In order to decouple the axis, a decoupling matrix $\mathbf{u}_{dec}$ is assumed in the input vector $\mathbf{u}$, as showed as follows:

$$\begin{cases} D_t\mathbf{x} = \mathbf{A}_{dec}\mathbf{x} + \mathbf{B}(\mathbf{u}\text{-}\mathbf{u}_{dec}) \\ \mathbf{y} = \mathbf{C}\mathbf{x}. \end{cases} \tag{4.27}$$

The comparison to the coupled model leads to the required matrix to decouple the d and q axis completely, which is given by

$$\mathbf{u}_{dec} = \mathbf{B}^{-1}\mathbf{A}_c\mathbf{x}. \tag{4.28}$$

However, it is clear that the complete decoupling of the axes require the observation of all state variables, which could be achieved through direct measuring or estimation. At any case, this method of decoupling becomes impractical considering a real application.

In this context, to address the coupling in this paper, only the controlled variables are going to be decoupled, i.e. the additive mode ($\mathbf{i}_{dq0,am}$) and subtractive mode ($\mathbf{i}_{i,dq0,sm}$) currents are the only state-variables that are going to be decoupled. The decoupling of the other variables is treated as perturbation that will be rejected by the control system. Therefore, the decoupling of additive and subtractive mode currents is achieved through $\mathbf{u}_{dec,am}$ and $\mathbf{u}_{i,dec,sm}$ respectively.

$$\mathbf{u}_{dec,am} = n \begin{bmatrix} -4\omega L_b \dfrac{i_{q,am}}{v_{dc}} \\ 4\omega L_b \dfrac{i_{d,am}}{v_{dc}} \\ 0 \end{bmatrix} \qquad \mathbf{u}_{i,dec,sm} = \begin{bmatrix} 4\omega L_s \dfrac{i_{i,q,sm}}{v_{dc}} \\ -4\omega L_s \dfrac{i_{i,d,sm}}{v_{dc}} \\ 0 \end{bmatrix} \tag{4.29}$$

4.2.4 Synchronization with the mains

One should note that Park's Transformation does not remove the time variance of the DC-link voltage differential equations in Appendix B as initially intended. To address the time variance of these equations, literature provides two distinctive methods. First, the dynamic average-operator can be applied over the mains period to the time-variant terms, as shown in [58, 59]. Alternatively, the time-variance can be addressed through the addition of the PLL to the model, which results in θ becoming a state variable [60]. The later was employed in this work, considering a Moving Average Filter Synchronous Reference Frame PLL (MAFSRF-PLL) based on [61]. The diagram of the PLL considered in this paper is depicted in Figure 4.3, where ω_0 is the nominal frequency of the grid.

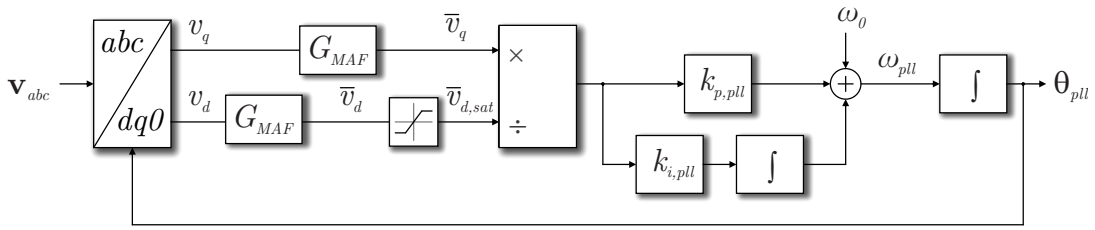


Figure 4.3 – Diagram of the MAFSRF-PLL.

The moving average filter transfer function (G_{MAF}) is defined as,

$$G_{MAF}(s) = \frac{1 - e^{-sT_w}}{sT_w} \approx \frac{1}{1 + \dfrac{1}{2}sT_w}, \tag{4.30}$$

where T_w is the filtering window period. In order to simplify the analysis, a first order Padé approximant was adopted. The comparison between MAF's frequency response and the 1st order Padé approximant is depicted in Figure 4.4. Also, in this work T_w was chosen as equal to the mains period, in order to provide attenuation to every harmonic component eventually present in the mains voltage.

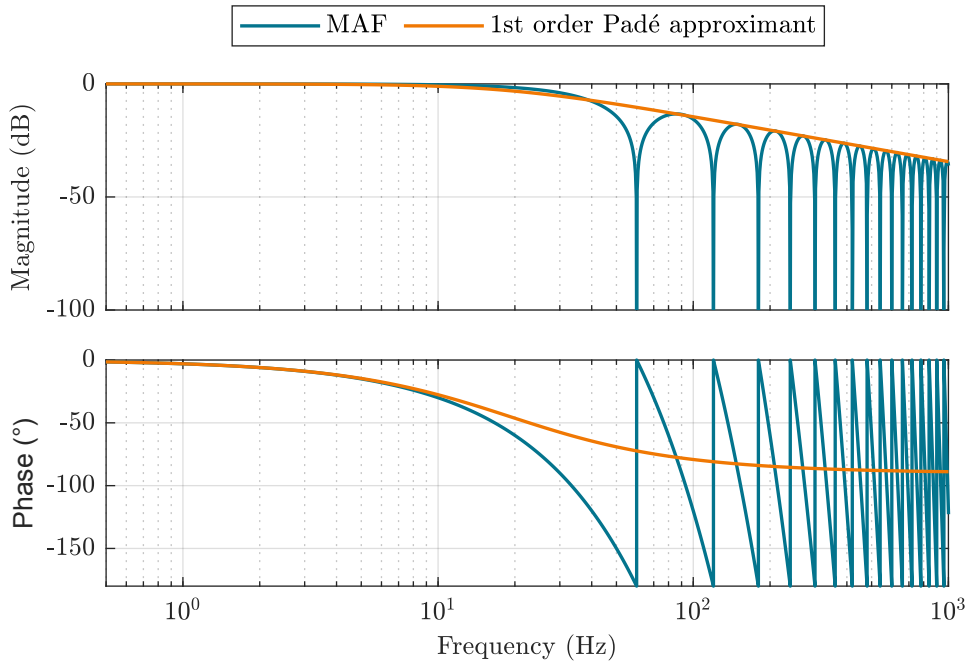


Figure 4.4 – between MAF's frequency response and the 1st order Padé approximant.

The state space model of the MAFSRF-PLL in Figure 4.3 is given by

$$\begin{cases} D_t \overline{v}_d = \dfrac{2}{T_w}(v_d - \overline{v}_d) \\ D_t \overline{v}_q = \dfrac{2}{T_w}(v_q - \overline{v}_q) \\ D_t\, \theta_{pll} = \omega_0 + k_{p,pll}\dfrac{\overline{v}_q}{\overline{v}_{d,sat}} + k_{i,pll}\varepsilon_{pll} \\ D_t\, \varepsilon_{pll} = \dfrac{\overline{v}_q}{\overline{v}_{d,sat}} \end{cases} \tag{4.31}$$

The Proportional-Integral (PI) controller employed in the PLL was designed for 5 Hz of gain crossover frequency and 60° of phase margin.

The model of the PLL is validated in Figure 4.5 for unbalanced and with high harmonic distortion mains voltage. It can be seem the accuracy of the proposed model given highly distorted mains voltage. The PLL output θ_{pll} was wrapped between 0 and 2π as to represent the actual implementation. In the complete model, the input of the PLL was configured as the voltage across the filter capacitors.

4.2.5 Controllers design

As the system is fully modeled, the to obtain the plants of the converter, consider the Laplace Transform of the state-space model, which yields

$$G(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A}_{dec})^{-1}\mathbf{B}. \tag{4.32}$$

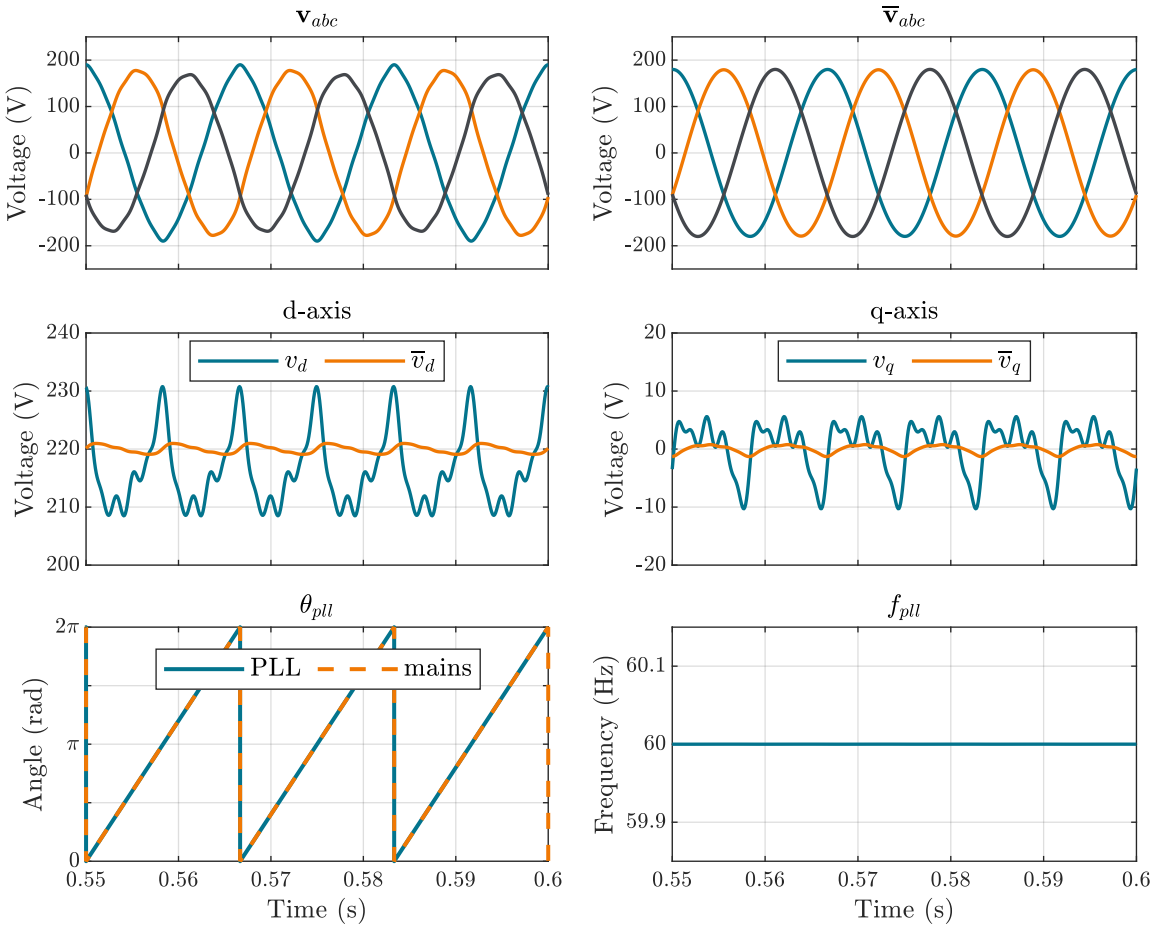


Figure 4.5 – Validation of the model of the MAFSRF-PLL.

With the small-signal model, the open loop transfer functions can be assessed and the controllers can be designed.

Moreover, to assess the controllers performance, a closed-loop approach was employed. In this scenario, if the controller dynamic equations are described by

$$\begin{cases} D_t\,\boldsymbol{\varepsilon} = \mathbf{A}_\varepsilon\,\mathbf{x} + \mathbf{B}_\varepsilon\,\boldsymbol{\varepsilon} + \mathbf{E}_\varepsilon\,\mathbf{r} \\ \mathbf{y}_\varepsilon = \mathbf{C}_\varepsilon\,\mathbf{x} + \mathbf{D}_\varepsilon\,\boldsymbol{\varepsilon} + \mathbf{F}_\varepsilon\,\mathbf{r} \end{cases} \tag{4.33}$$

where $\boldsymbol{\varepsilon} \in \mathbb{R}^{n_\varepsilon}$ is the controller's states vector, $\mathbf{r} \in \mathbb{R}^{nr}$ is the references vector. The variable n_ε represents the number of state variables in the controller and depends on the type of controllers employed, whereas n_r represents the number of references and is equal to the number of controlled states in $\mathbf{x}$.

In this scenario, the closed-loop model of the T-Type interleaved converter consid-

ering Equation 4.25 and Equation 4.33 is expressed as

$$\begin{cases} D_t \begin{bmatrix} \mathbf{x} \\ \boldsymbol{\varepsilon} \end{bmatrix} = \begin{bmatrix} \mathbf{A}_{dec} + \mathbf{B}\mathbf{C}_{\varepsilon} & \mathbf{B}\mathbf{D}_{\varepsilon} \\ \mathbf{A}_{\varepsilon} & \mathbf{B}_{\varepsilon} \end{bmatrix} \begin{bmatrix} \mathbf{x} \\ \boldsymbol{\varepsilon} \end{bmatrix} + \begin{bmatrix} \mathbf{B}\mathbf{F}_{\varepsilon} \\ \mathbf{E}_{\varepsilon} \end{bmatrix} \mathbf{r} + \begin{bmatrix} \mathbf{E} \\ 0 \end{bmatrix} \boldsymbol{\omega} \\ \mathbf{y} = \mathbf{C}\mathbf{x}. \end{cases} \tag{4.34}$$

With the closed-loop model defined, the control loops can be designed separately and integrated to the system.

4.2.6 Current controllers

The control strategy considered for the current in both additive and subtractive modes is depicted in Figure 4.6. The references for the current control are all zero but $i_{d,am,ref}$, which is directly related to the power processed by the converter. Moreover, m_0 is a gamma/0-axis component added to the modulation signals in order to balance the DC-link capacitors voltages, which can be assumed to be zero at this point of the control design, as the DC-link is assumed to be constant and equal to its rated voltage.

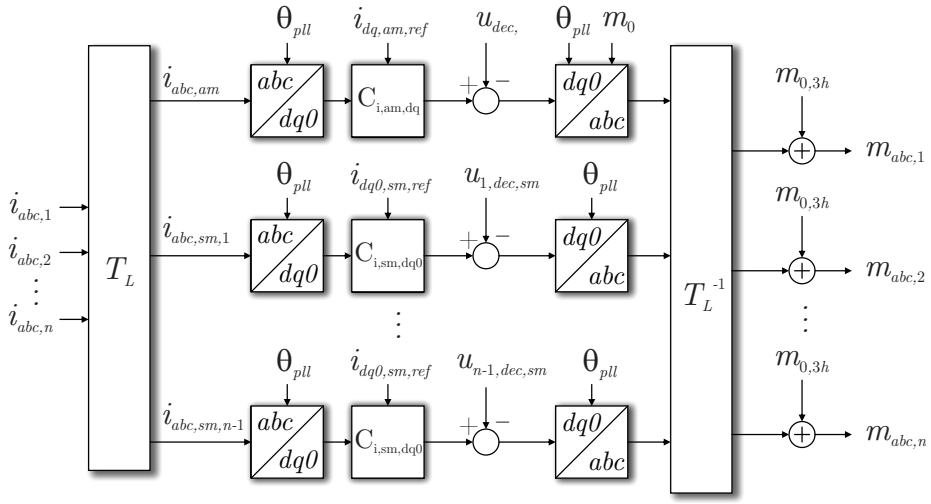
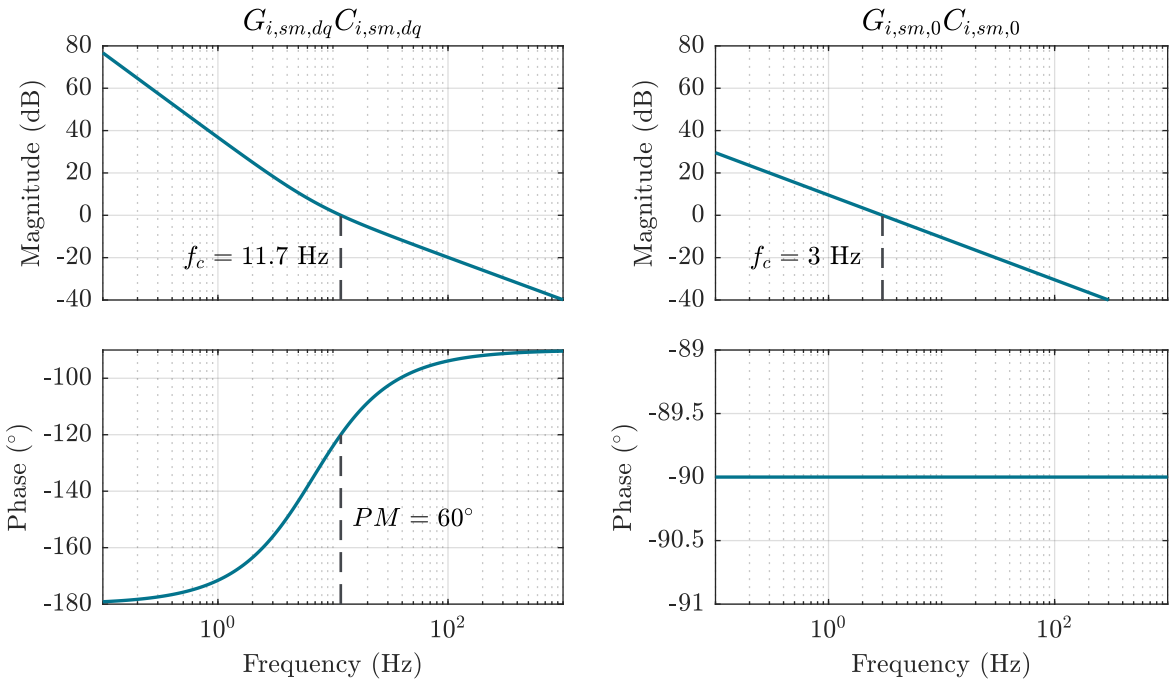


Figure 4.6 – Diagram of current control strategy.

Considering the dq0 frame, PI controllers can be employed at a first approach. The state-space representation of a PI controller is defined as

$$\mathbf{A}_{pi} = 0, \quad \mathbf{B}_{pi} = 1, \quad \mathbf{C}_{pi} = K_i, \quad \mathbf{D}_{pi} = K_p. \tag{4.35}$$

Considering the design parameters in Table 3.1 and the coupled inductors designed in Chapter 3, the subtractive mode current controllers were designed for gain crossover frequency of 11.7 Hz and phase margin of 60°. This lead to $K_{p,i,dq,sm} = -0.00014258$ and $K_{i,i,dq,sm} = -0.0060505$ used for the dq axes. For the gamma/0-axis, only a proportional controller was employed considering a bandwidth of 3 Hz, leading to $K_{p,i,0,am} = -4.2223.10^{-5}$. The open-loop controlled bode diagrams are depicted in Figure 4.7.



(a) **(b)**

Figure 4.7 – Open-loop controlled subtractive mode currents bode diagram: (a) dq-axes and (b) 0-axis.

Regarding the additive mode, the controller aimed a bandwidth of 100 Hz and phase margin of 60°, leading to $K_{p,i,dq,am} = -0.016896$ and $K_{i,i,dq,am} = -3.5654$. The open-loop controlled bode diagram is depicted in Figure 4.8. However, for the additive mode it is observed that a PI controller is not sufficient to mitigate the low order harmonics eventually present in the mains voltage. Therefore, literature [53, 62, 63] suggest the implementation of resonant controllers in parallel to the PI controller in order to provide attenuation to the harmonics.

The state-space model of a multi-resonant controller can be defined as

$$\begin{aligned}
\mathbf{A}_r &= \begin{bmatrix} 0 & \omega_1 & \dots & 0 & 0 \\ -\omega_1 & -2\zeta_1\omega_1 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 0 & \omega_{n_r} \\ 0 & 0 & \dots & -\omega_{n_r} & -2\zeta_{n_r}\omega_{n_r} \end{bmatrix} \\
\mathbf{B}_r &= \begin{bmatrix} 0 & 2\zeta_1\omega_1 & \dots & 0 & 2\zeta_{n_r}\omega_{n_r} \end{bmatrix}^T \\
\mathbf{C}_r &= \begin{bmatrix} 0 & K_{r,1} & \dots & 0 & K_{r,n_r} \end{bmatrix} \\
\mathbf{D}_r &= 0,
\end{aligned} \tag{4.36}$$

where ω_k, ζ_k and $K_{r,k}$, $k \in \{1, 2, \dots, n_r\}$, are the resonance frequency, damping factor and

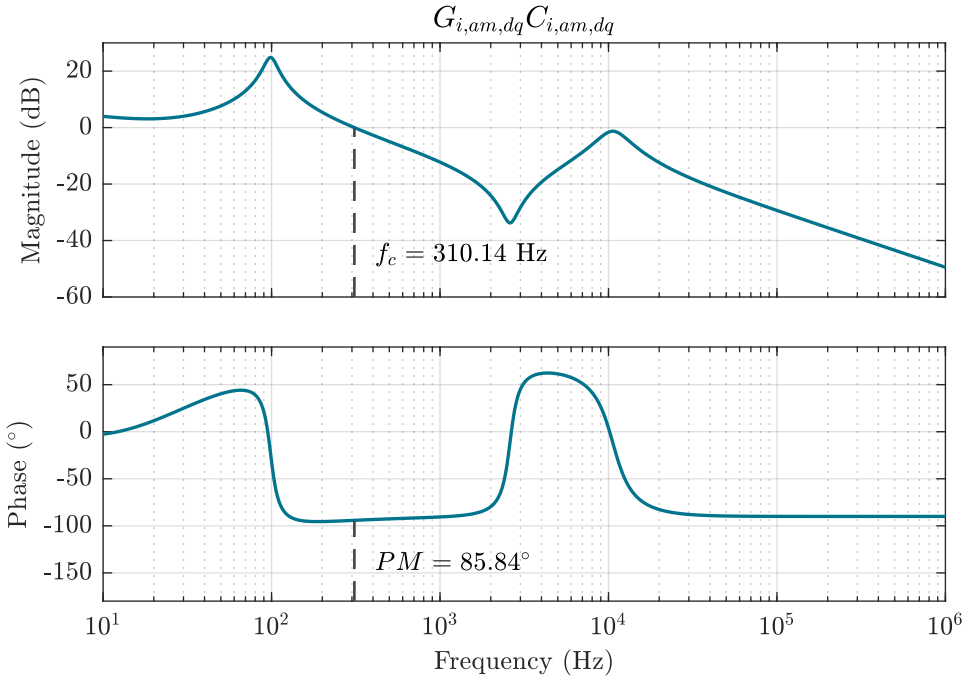


Figure 4.8 – Bode diagram of open-loop controlled current plant.

resonance gain of the k-th resonant controller.

One important aspect of the resonant controllers in dq-frame is that each controller has a double harmonic compensation, as a k-th order resonant controller is able to compensate both negative sequence (1-k)-th and positive sequence (1+k)-th order harmonics [63]. In this scenario, a 6th and 12th order resonant controllers were considered for the additive mode current controller design for both dq-axes. The controllers were designed empirically through the analysis of the impedance in the PCC. The process lead to a damping factor $\zeta = 0.002$ and resonant gains of $K_{r,1} = -0.23$ and $K_{r,1} = -0.18$ for the 6-th and the 11-th order resonant controllers respectively. The impedance frequency response at the PCC for the proposed controllers is illustrated in Figure 4.9.

4.2.7 Voltage controllers

The control strategy considered for the DC-link voltage is depicted in Figure 4.10. A DC-link voltage controller and a voltage balance controller are required to ensure rated voltage during operation of the converter under various circumstances maintaining balanced voltages across the DC-link capacitors. In this work, the DC-link voltage controller employed was a PI controller, which was designed for a bandwidth of 4.03 Hz and phase margin of 22.9°, leading to $K_{p,v} = 0.033469$ and $K_{i,v} = 1.5042$. Regarding the voltage balance controller, a PI controller was employed and it was designed for a bandwidth of 75.7 Hz and phase margin of 11.3°, leading to $K_{p,\Delta v} = 0.0034284$ and $K_{i,\Delta v} = 0.02853$.

For applications in weak grids, the consideration of $i_{q,am,ref}$ being null to guarantee high power factor operations cannot be applied. In this scenario, the voltage drop on the

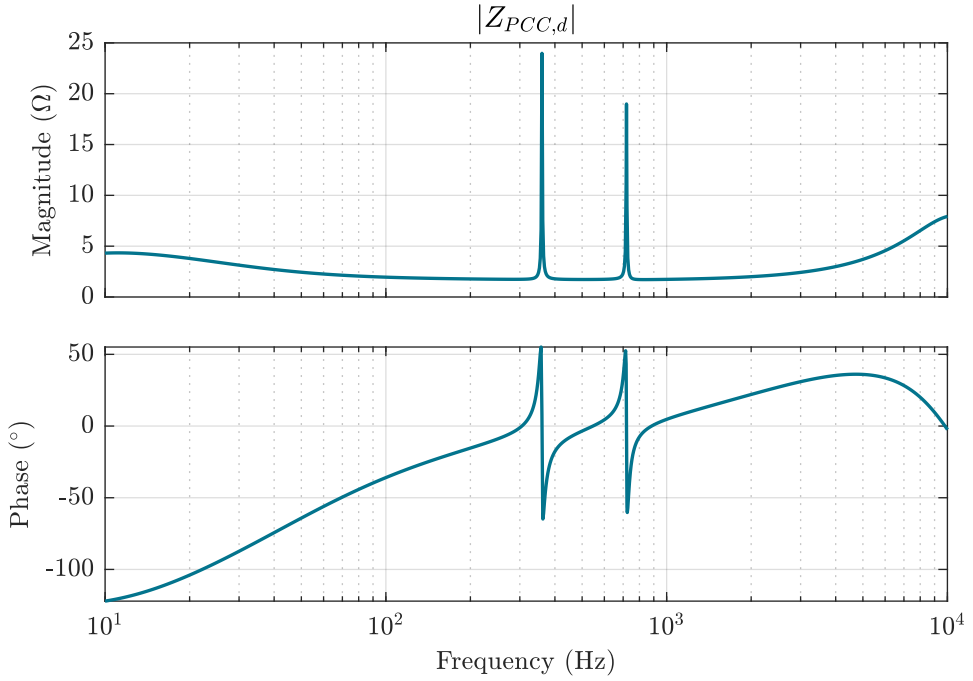


Figure 4.9 – Frequency responce of the impedance in the PCC in the d-axis.

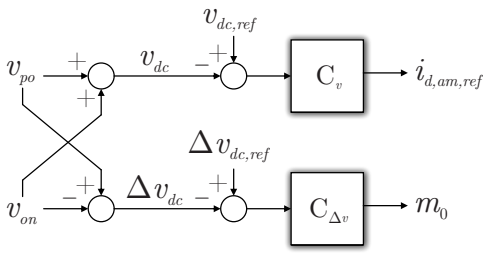


Figure 4.10 – Diagram of voltage control strategy.

mains impedance cause a raise in the AC side current in order to keep the output power constant. Therefore, to compensate the voltage drop in the mains impedance, a voltage controller is employed as depicted in Figure 4.12. The control acts on the q-axis additive mode current reference, which is directly associated to the reactive power processed by the converter. Hence, a PI controller is employed with $K_{p,vm} = 0.167345$ and $K_{i,vm} = 0.55605$.

4.2.8 Considerations on stability

In order to analyze the proposed system stability, the eigenvalues method was chosen. However, the addition of the PLL dynamics and the consideration of mains voltage harmonics make the proposed-closed loop model time-variant. In this context, the model must be truncated for the purpose of stability analysis. Therefore, the PLL is adjusted in order to portray only the delay relative to the mains reference in the control frame, as follows [64]:

$$\mathbf{v}_{c,dq} = \mathbf{R}(\Delta\theta)\mathbf{v}_{m,dq} \tag{4.37}$$

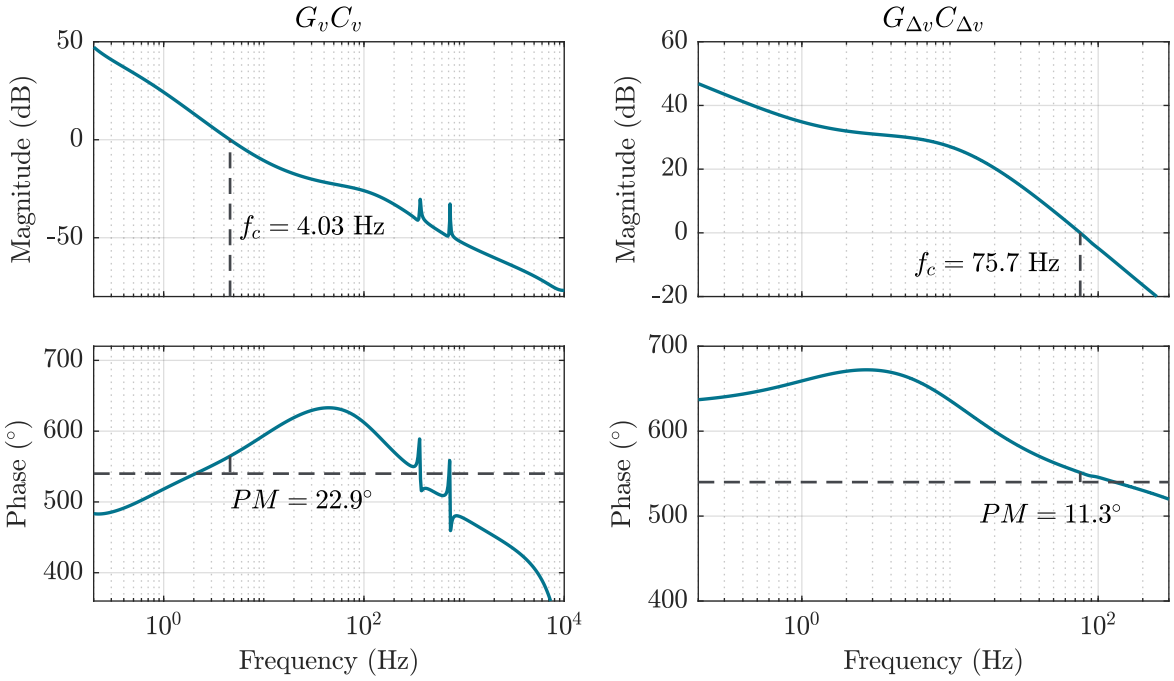


Figure 4.11 – Open-loop controlled DC-link voltage bode diagram.

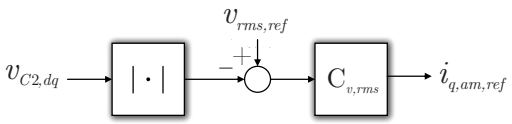


Figure 4.12 – Diagram of mains voltage compensation strategy.

where, $\mathbf{v}_{c,dq}$ represents the voltage input of the PLL in the control dq-frame whereas $\mathbf{v}_{m,dq}$ represents the same voltage in the mains dq-frame, considered as the reference. One should notice that the 0-axis was neglected in the definition as it is assumed to be constantly null in normal operation of the mains. Matrix $\mathbf{R}(\Delta\theta)$ denotes a rotation of $\Delta\theta$ amongst the frames and this angle variation is the new state of the PLL. Moreover, the matrices $(\mathbf{I}_3 \otimes \mathbf{\Gamma})_R$ and $\mathbf{\Lambda}_R$ were substituted by their average value considering the mains period in order to remove time variance.

However, the eigenvalue criterion for stability analysis of the simplified model shows poor guidance on the stability boundaries assessment of the converter for the proposed control strategy. Simulations varying the SCR for the rated active power showed a minimum value of $SCR = 0.98$ where the converter was still stable. However, when this value was confronted in the complete model, it showed that the converter is in fact not stable at this operation point.

4.2.9 Conclusion

The developed model in this chapter has demonstrated accuracy by effectively simulating dynamics in the T-Type interleaved converter, enabling appropriate controller

design. Similarly, the proposed closed-loop model successfully captured controller dynamics and served as a valuable tool for control tuning, eliminating the need for switched-level simulation software.

However, the proposed model has limitations due to its time variance, preventing direct use for stability assessment of the converter. To address this challenge, simplifications must be made, potentially truncating system dynamics and resulting in imprecise stability boundaries. Alternatively, employing a different modeling technique capable of removing time variance without compromising dynamic properties could be explored, like the Floquet-theory-based method [65]. This area warrants further investigation beyond the scope of this study and could be considered for future research.

Chapter

5

Experimental and computational validation results

5.1 INTRODUCTION

The previous chapters focused on magnetic elements and filter design. To validate the proposed design, a prototype was conceptualized and constructed according to the desired parameters. This chapter outlines the prototype design and the main components utilized.

Following this, it is presented experimental validation results of the converter for various modulation schemes discussed in this work. Efficiency curves for each modulation strategy are analyzed. Additionally, a temperature assessment of the magnetic elements is conducted to validate the thermal model used in the optimization routine.

Lastly, the chapter validates the control strategy through experiments conducted in the simulation software PLECS. These experiments aim to demonstrate the dynamic performance of the converter under different conditions, including operation under weak grids, operation as a rectifier with asymmetric loads connected to the DC-link, and the impact of the STHI modulation technique on the DC-link voltage.

5.2 OPEN-LOOP EXPERIMENTAL VALIDATION

5.2.1 Prototype design

The prototype was conceived based on the parameters specified in Table 3.1, repeated on Table 5.1 for clarity. Considering this set of parameters, the filter components were designed with an optimization strategy as described in Chapter 3. The optimally designed coupled inductors for additive and subtractive modes lead to the design of the other elements of the filter in Chapter 3, which are listed in Table 5.2.

With the filter elements designed, a printed circuit board (PCB) was made to accommodate all filter elements as depicted in Figure 5.1. The filter PCB dimensions are $246\,\text{mm} \times 203\,\text{mm} \times 100\,\text{mm}$.

Regarding the T-Type interleaved converter, a PCB was designed considering the use

Parameter	Description	Value
P_r	Rated power	10 kW
V_{rms}	Mains rms phase voltage	127 V
f_m	Mains frequency	60 Hz
V_{dc}	DC-link voltage	400 V
n	Number of interleaved modules	2
f_s	Switching frequency	35 kHz

Table 5.1 – Parameters for the interleaved T-Type converter prototype.

Parameter	Description	Value
L_b	Self-inductance of additive mode inductor	40.12 μH
L_s	Self-inductance of subtractive mode inductor	224.52 μH
C_1	Filter capacitor	2.2 μF
C_2	Damping branch capacitor	2.2 μF
R_d	Damping resistor	10 Ω
L_2	Common-mode choke	6123-X140
C_3	Common mode damping branch capacitor	2.5 nF
$R_{d,cm}$	Common mode damping branch resistor	1.1 Ω

Table 5.2 – Filter elements for the interleaved T-Type converter prototype.

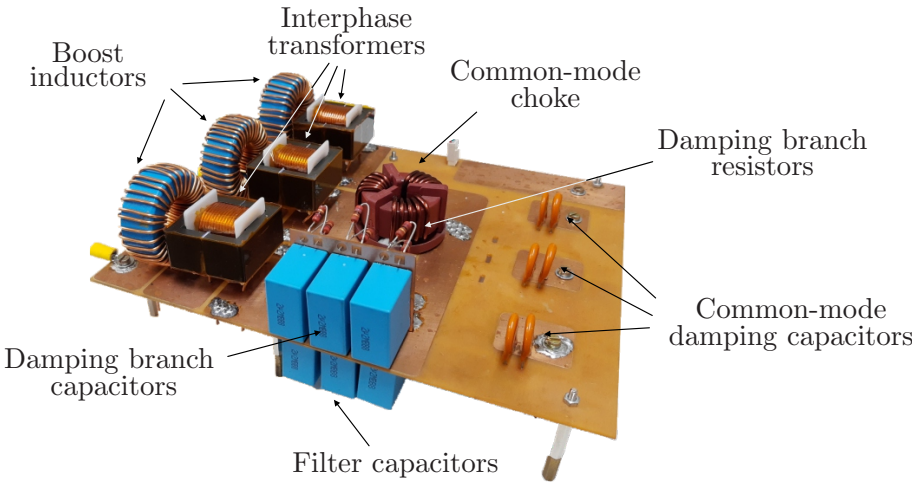


Figure 5.1 – Filter PCB.

of E3M0075120K (Wolfspeed) SiCFETs for the bridge semiconductors and UF3C065080K4S (UnitedSiC) SiCFETs for the connection of the phase leg to the central point of the DC-link. For the DC-link capacitors, the minimum capacitance required was stipulated with Equation 2.33, considering $\Delta_t = 0.5/f_m$ and $V_{dc,min} = 0.7V_{dc}$, leading to $C_{b,min} = 2$ mF. To obtain the minimum DC-link capacitance, two 1 mF electrolytic capacitors were employed for each half of the DC-link. Film and ceramic capacitors were employed in parallel to the DC-link and switching semiconductor pairs to support the switching process with low

equivalent series resistance (ESR) and inductance (ESL). Acquisition circuits were designed to measure the currents at each phase, the DC-link capacitors voltages and the voltages on the filter capacitors. The schematics for the acquisition circuits are shown in Appendix D. The main components in the converter PCB are listed in Table 5.3 and the built PCB is shown in Figure 5.2. The converter PCB dimensions are 262 mm × 320 mm × 106 mm.

Component	Description
E3M0075120K	Bridge semiconductors
UF3C065080K4S	Central point semiconductors
TMDSCNCD28377D	Digital Signal Processor (DSP)
CASR 25-P	Current transducers
UCC5350MCQDWVRQ1	Gate drivers
MGJ2D121505SC	2 W isolated power supply
LAM-4-150	Heatsinks

Table 5.3 – PCB components for the interleaved T-Type converter prototype

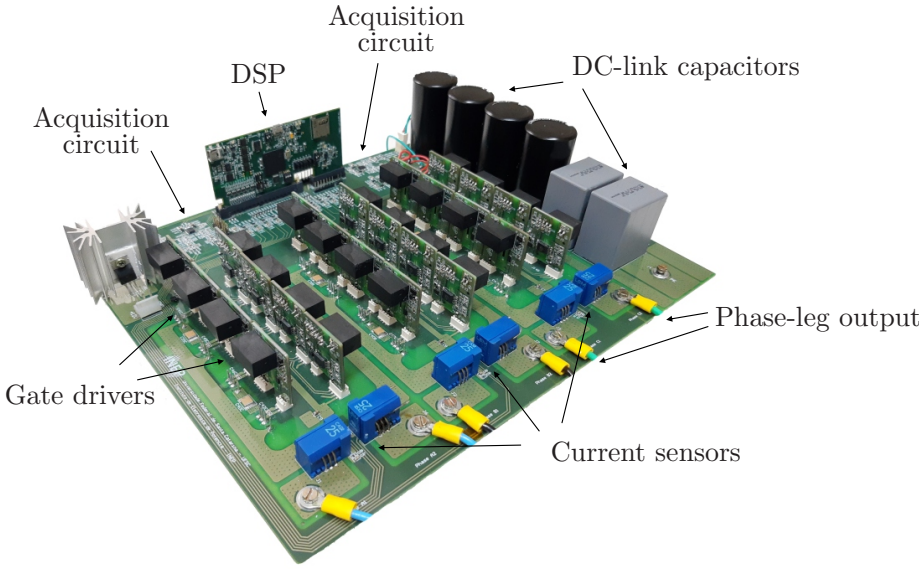


Figure 5.2 – Interleaved T-Type converter PCB.

Although two different SiCFET models were utilized in the prototype, both being third-generation SiCFETs, a single gate driver was designed for all semiconductor devices. The gate-to-source voltages during the on and off stages were +15 V and -4 V, respectively [66]. Gate resistors of 4.7 Ω and 10 Ω were employed for turn-on and turn-off stages, respectively. For the gate driver, the UCC5350MCQDWVRQ1 from Texas Instruments was selected to meet the Miller clamp-protection requirements specified by semiconductor device manufacturers and to reduce turn-off energy [67]. Additionally, a cutout was incorporated into the dedicated gate driver PCBs to enhance creepage between primary and secondary components.

The schematics of the PCBs utilized in this testing configuration, including the power PCB, filter, and gate driver, are presented in Appendix D.

5.2.2 Experimental results

5.2.2.1 Modulation strategies

The modulation strategies underwent experimental evaluation in an open-loop inverter mode setup of the converter, using a 10 kW rated load and a modulation index $M = 0.898$ across all tests. Results for each modulation are depicted in Figure 5.3. Measurements were conducted using a Tektronix 5034 oscilloscope and a Yokogawa WT1800 power analyzer. Each test analyzed the terminal voltage $v_{1,ao}$ and its dynamic average value $M_{Ts}(v_{1,ao})$ to observe the direct impact of the modulation strategy on the converter terminal voltage. Additionally, currents $i_{1,a}$, $i_{2,a}$, and $i_{1,sm,a}$ were monitored to ensure equal power distribution among corresponding phase legs. Line voltages and phase currents at the PCC were assessed to compute AC power using the two wattmeters method. These variables are also recorded in the results obtained from the Yokogawa WT1800 power analyzer.

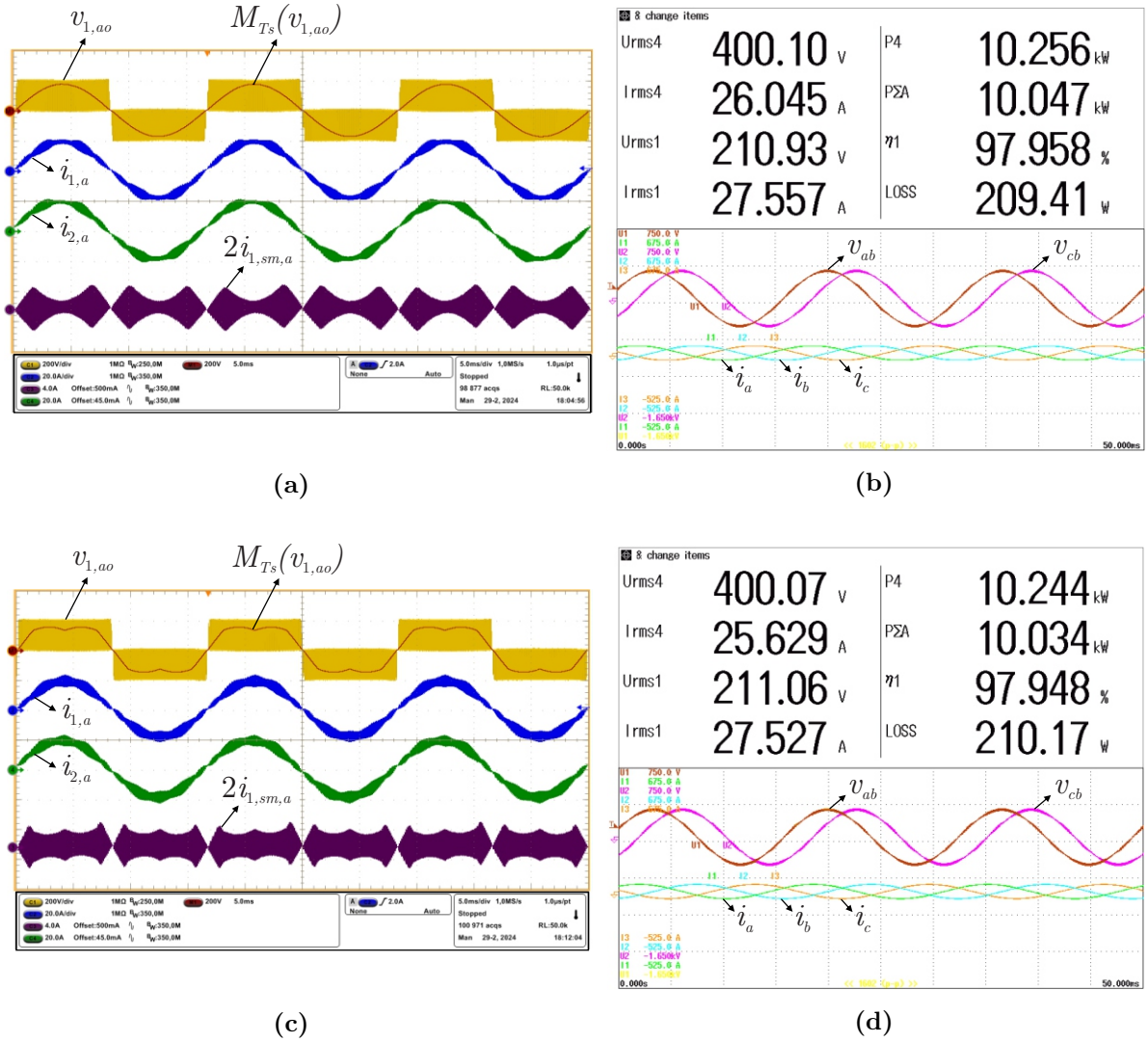


Figure 5.3 – Experimental results for SPWM (a,b), SVM (c,d), STHI (e,f) and DPWM (g,h) modulation schemes (Part 1).

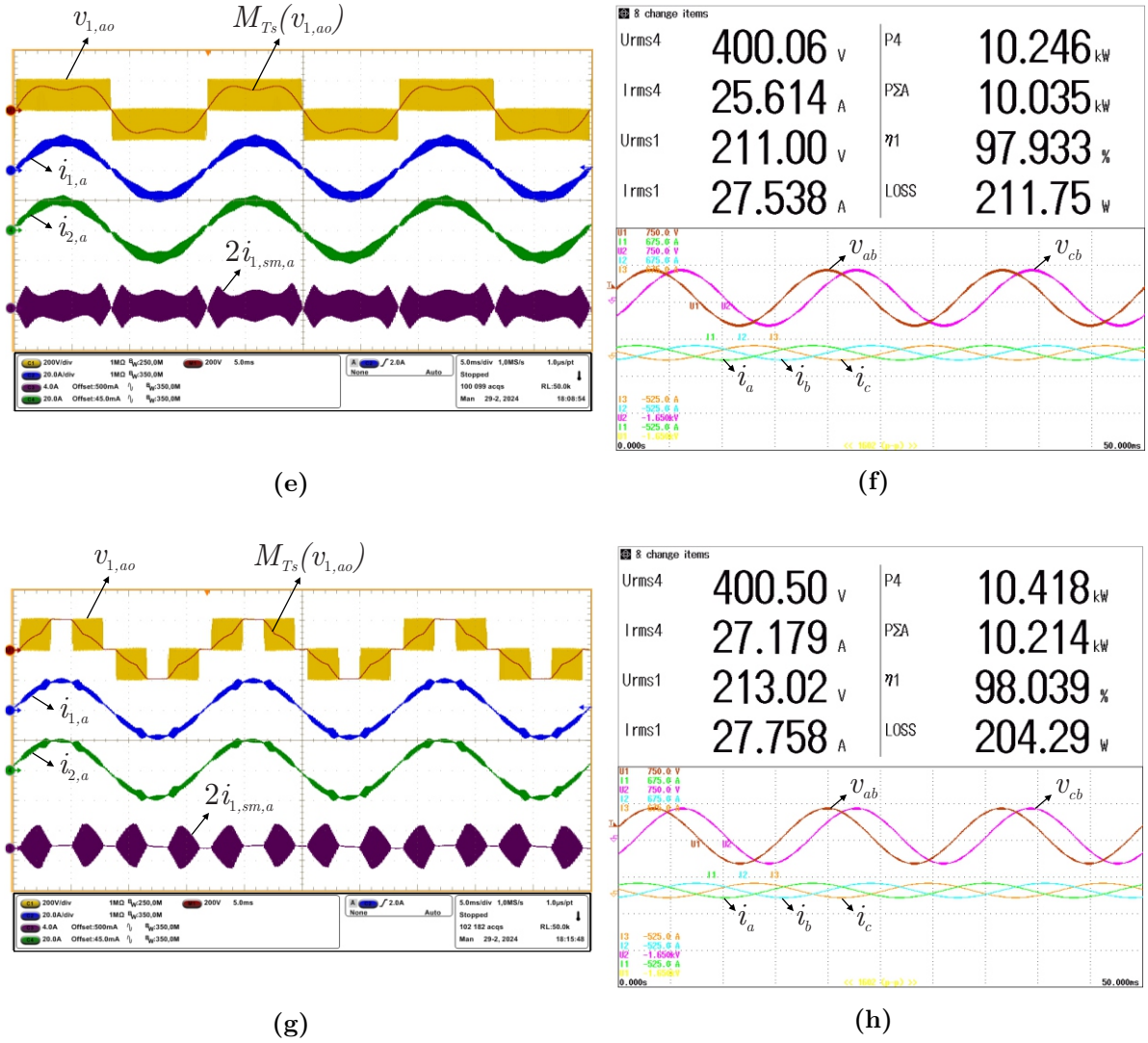
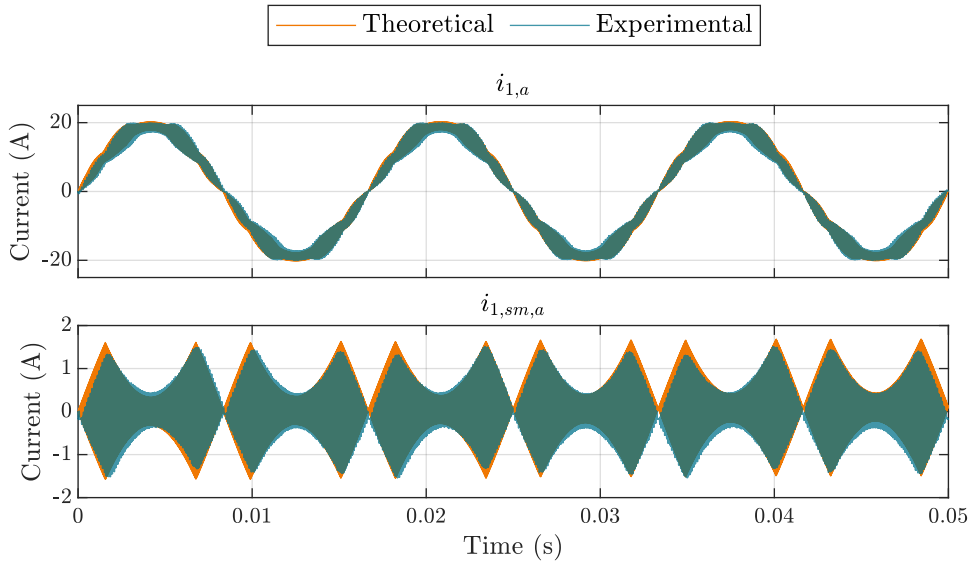


Figure 5.3 – Experimental results for SPWM (a,b), SVM (c,d), STHI (e,f) and DPWM (g,h) modulation schemes (Part 2).

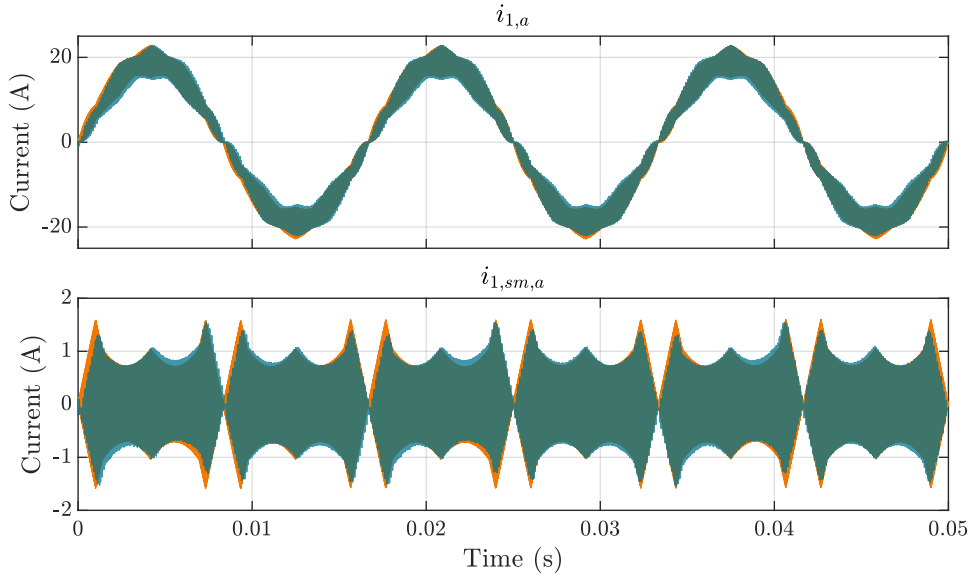
The efficiency of the converter measured by the power analyzer does not account the losses in the auxiliary sources, which were provided by external sources. Therefore, based on Figure 5.3, it is evident that DPWM outperforms other modulation strategies in terms of efficiency. The remaining strategies exhibit similar efficiency levels, consistent with the proposed power losses model in Chapter 3. Thus, employing DPWM instead of STHI in the optimization method could potentially lead to further reduction in the resulting filter size.

To validate the experimental results, Figure 5.4 and Figure 5.5 compares these results to their theoretical counterparts for currents $i_{1,a}$ and $i_{1,sm,a}$ for each modulation strategy. The close agreement between the shown results validates both the proposed numerical model for assessing converter currents and the experimental measurements. Further analysis of the compliance between theoretical and experimental results is presented in Table 5.4, which compares the rms values of $i_{1,a}$ and $i_{1,sm,a}$ for each modulation scheme.

Noticeably, the DPWM scheme exhibits the largest error for both figures of merit, while for $i_{1,sm,a}$ the errors are more significant due to the low amplitude of this parameter. These mismatches may be attributed to parasitic elements and asymmetries in both boost inductors and interphase transformers, which were not considered in the model. Additionally, inconsistencies in the test setup, such as oscillations in the DC power supply, can negatively influence result compliance. Finally, the error in the subtractive mode currents can also be associated to the measuring method, which consisted into passing the cables from both phases through the same current probe with different directions.



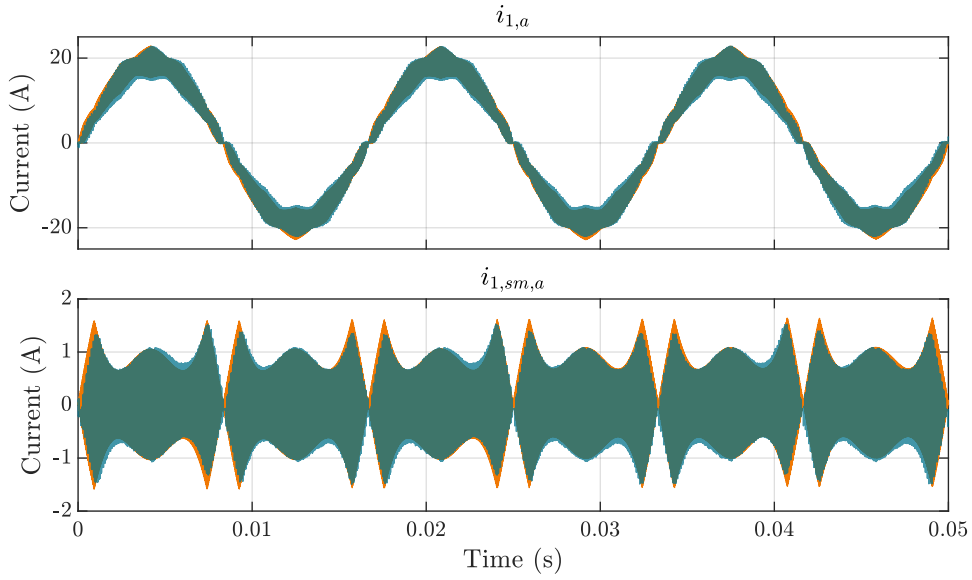
(a)



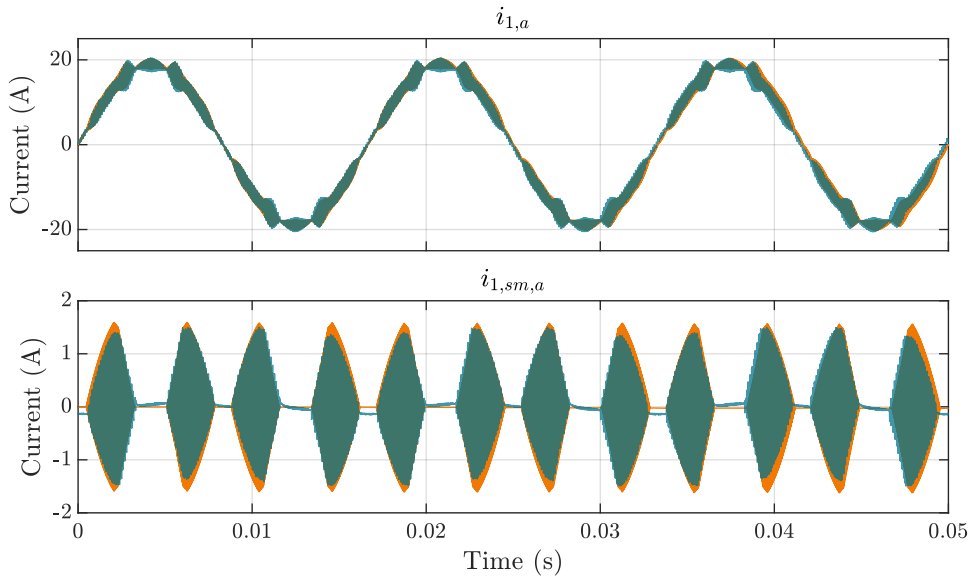
(b)

Figure 5.4 – Comparison between theoretical and experimental results for SPWM (a) and SVM (b) modulation schemes.

Finally, the theoretical and experimental efficiency curves for each modulation



(a)



(b)

Figure 5.5 – Comparison between theoretical and experimental results for STHI (a) and DPWM (b) modulation schemes.

strategy was assessed and the results as shown in Figure 5.6. One may notice that the proposed power losses model can assess the converter's efficiency with reasonable accuracy, having the smaller error in the DPWM modulation. The errors observed are assigned to the power losses that were not considered in the model, as the losses in the common-mode choke, the damping resistors from both differential and common-mode filter and other parasitic losses that occur in contact and cables.

Modulation	$i_{1,a}$			$i_{1,sm,a}$		
	Theo.	**Exp.**	**Error** (%)	**Theo.**	**Exp.**	**Error** (%)
SPWM	13.4895	13.2590	1.7087	0.6416	0.7159	11.5804
SVM	13.4906	13.2647	1.6745	0.6842	0.7572	10.6694
STHI	13.4907	13.2604	1.7071	0.6919	0.7634	10.3339
DPWM	13.6846	13.3288	2.6000	0.5728	0.6534	14.0712

Table 5.4 – Theoretical and experimental rms values of the phase and subtractive currents and relative percentual error.

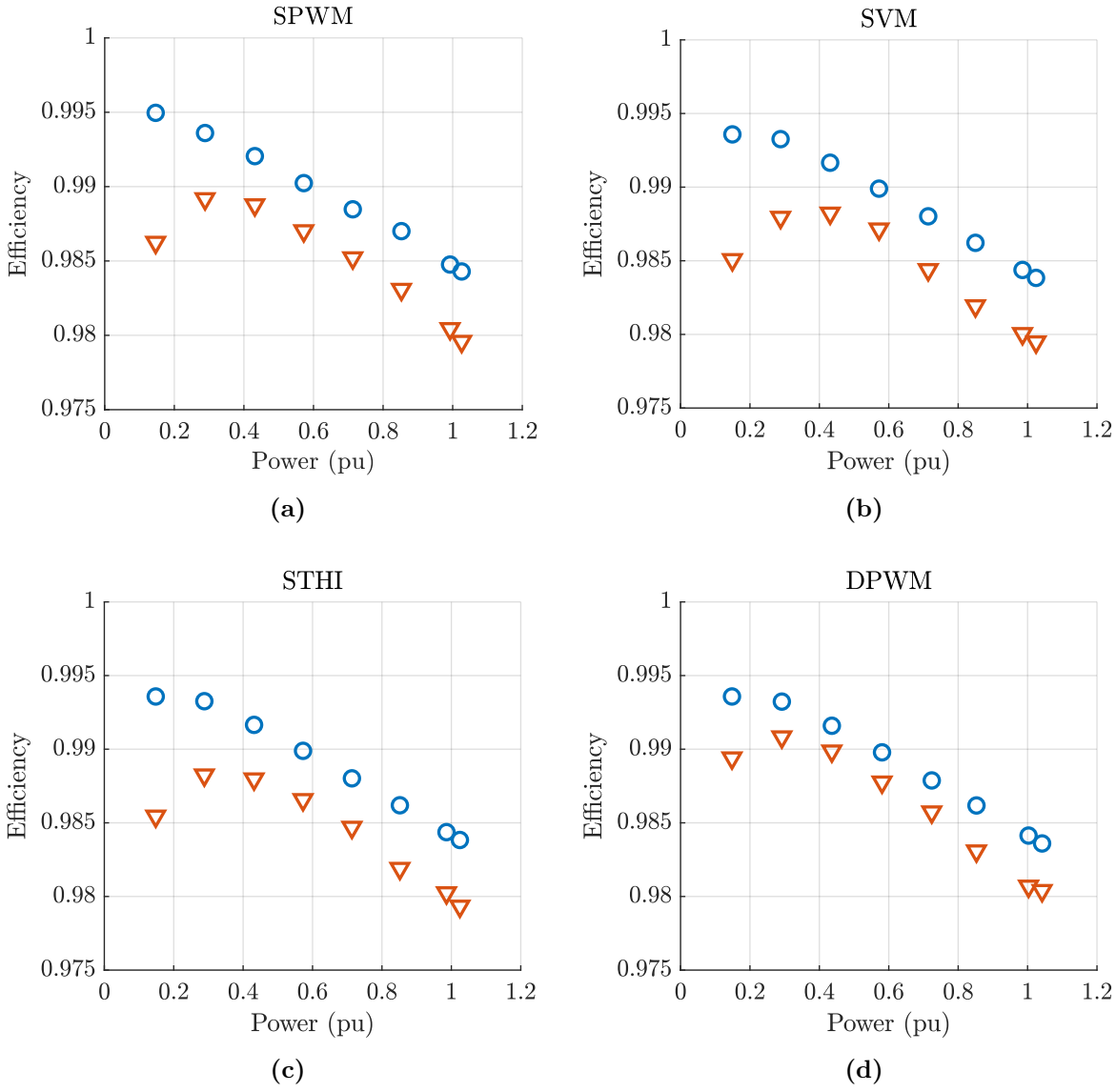


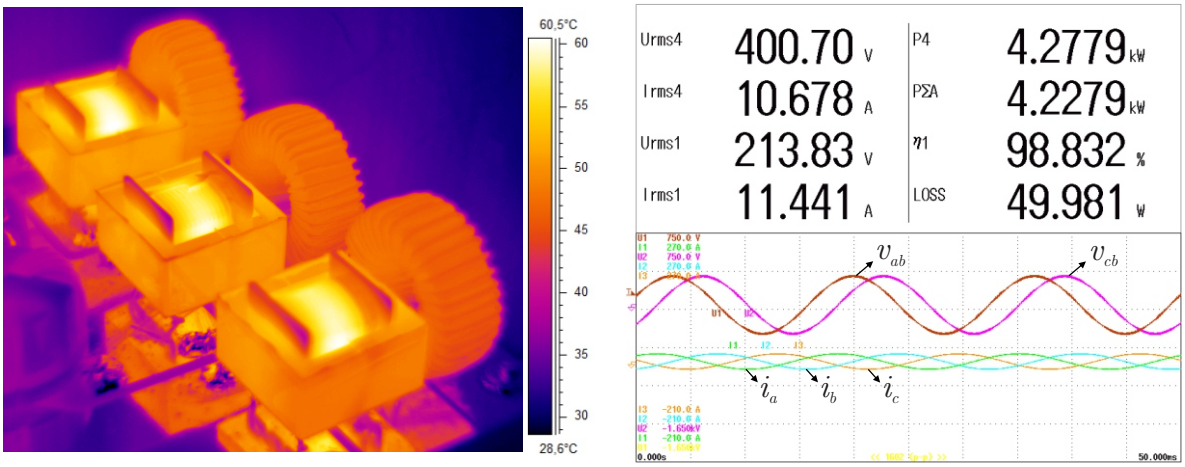
Figure 5.6 – Comparison between theoretical (○) and experimental (▽) efficiency of the converter.

Another limitation of the power losses model is the assessment of the power losses under 40% load. This restraint might be associated to the temperature effect of the power losses in the magnetic elements, as they were not considered in the power loss calculation

per se, only for the total temperature rise estimation.

5.2.2.2 Thermal model

Regarding the proposed thermal model described in Chapter 3, a experiment was conducted in order to observe the temperature rise in the magnetic elements when in thermal steady state. The experiment was carried considering 4.2779 kW, the room temperature was assessed in 31.80°C and the measurements were taken after 45 minutes of the converter functioning. This experiment had to be taken under lighter load due to safety reasons regarding temperature rise of the resistive load used in the experimental setup. Considering this parameters, the model predicted a temperature rise of 15.00°C and 13.72°C for the boost inductor and the interphase transformer respectively. The experimental results are shown in Figure 5.7 and it is observed a temperature of 48.1°C for the boost inductors and 58.1°C for the interphase transformers central limb, which correspond to a temperature rise of 16.3°C and 26.3°C respectively.



(a) **(b)**

Figure 5.7 – Experimental results for thermal assessment of the converter.

It can be seen that the model was accurate to estimate the temperature rise of the boost inductors but presented a large error in the temperature rise estimation of the interphase transformer. This limitation of the model can be associated to many sources of error: the estimation of constants used for the thermal resistances in the model, the radiation effect of the other hot surfaces close to the magnetic elements in the filter PCB, existence of air currents that affect convection heat transfer, presence of other materials in the inductor assembly such as tape and the plastic coil former. Therefore, as the effect of the listed possible causes of discrepancies in the model were neglected, the proposed thermal model is subject to improvement, especially considering the double E core model, which has different temperature rise in the central limb and external limbs.

5.2.3 Closed-loop simulation results

5.2.3.1 DC-link voltage balancing

In this work, the modulation method chosen aims to reduce the current in the neutral-point of the DC-link o by injecting a zero-sequence component in the modulation signals. Consequently, the effect of this method to the DC-link capacitors is a reduction in the voltage oscillation and better voltage balancing. First, considering the T-Type operation modes, the modulation signal $d_{ox,i}$ on the i-th module of phase x that corresponds to the time the zero voltage level is imposed in the phase output is given by:

$$d_{0x,i} = 1 - |m_{x,i}| = 1 - \text{sign}\left(m_{x,i}\right). \tag{5.1}$$

Therefore, the current collected in the neutral-point o considering the three-phase operation of the converter is given by:

$$i_o = \sum_{x=a,b,c} \sum_{i=1}^{n} d_{0x,i} i_{i,x} = - \sum_{x=a,b,c} \sum_{i=1}^{n} m_{i,x} \text{sign}\left(m_{i,x}\right) i_{i,x} \tag{5.2}$$

Considering the zero-sequence component injection to the modulation signals, it is expected that the current on the neutral point will be minimized, and therefore will be assumed equal to zero. These considerations result in the desired zero-sequence component:

$$- \sum_{x=a,b,c} \sum_{i=1}^{n} (m_{i,x} + m_0) \text{sign}\left(m_{i,x}\right) i_{i,x} = 0 \therefore m_0 = - \frac{\sum\limits_{x=a,b,c} \sum\limits_{i=1}^{n} m_{i,x} \,\text{sign}\left(m_{i,x}\right) i_{i,x}}{\sum\limits_{x=a,b,c} \sum\limits_{i=1}^{n} \text{sign}\left(m_{i,x}\right) i_{i,x}}. \tag{5.3}$$

The analysis of Equation 5.3 leads to the conclusion that the zero-sequence component to be added to the modulation signals is a third harmonic component as given by Equation 2.35 and repeated here for clarity:

$$m_0 = m_{cm,sthi} = \frac{M}{4} \sin(3\theta) \tag{5.4}$$

To validate the current i_o minimization method, a simulation in PLECS was performed considering the converter and control strategy parameters presented in Chapter 3 and Chapter 4. The simulation consisted in starting the converter without the third harmonic injection, then apply it at 1.5 s of simulation, as shown by the results in Figure 5.8. It is observable that before the injection of the third harmonic component, the voltage oscillation in the DC-link capacitors voltage reaches a maximum of 15.1427 V, whereas after the third harmonic injection, the maximum oscillation is of 0.7501 V, representing a reduction of 95.05% regarding the voltage for SPWM. Regarding the current i_o, its rms value before the third harmonic injection is 14.9429 A while after the third harmonic injection the rms value is reduced to 5.9201 A, representing a reduction of 60.38%

regarding the current for SPWM.

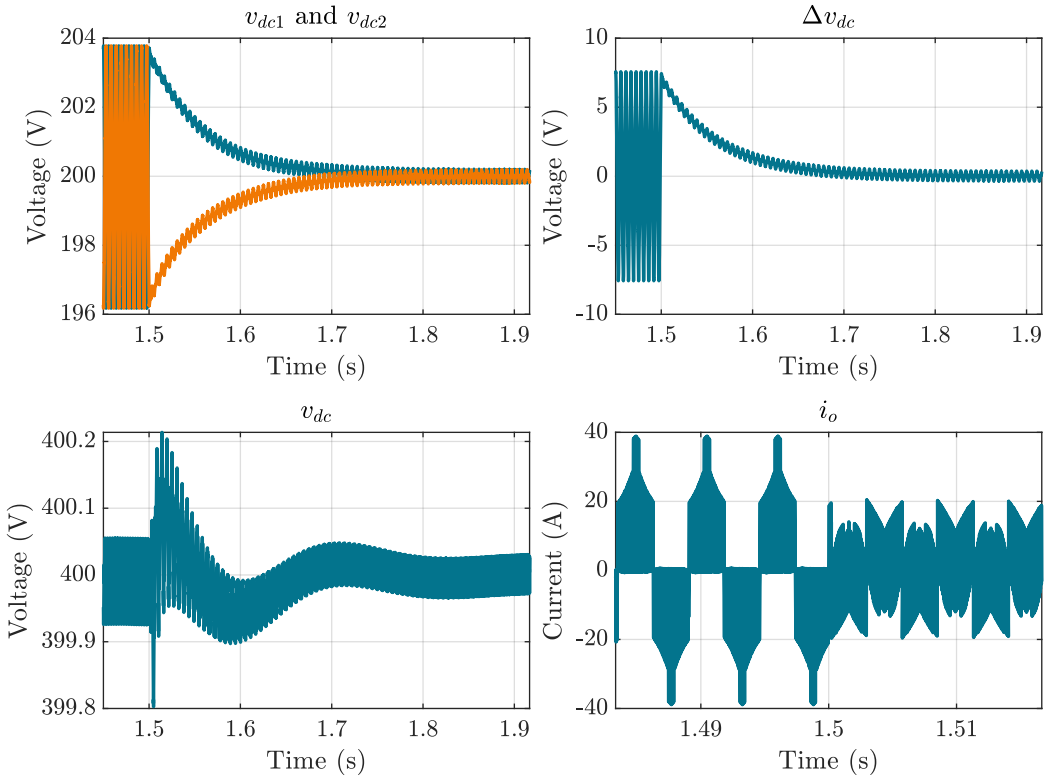


Figure 5.8 – Simulation results for validation of third harmonic injection.

5.2.3.2 Operation with different loads in the DC-link

Converters with split DC-link can feature different power sources connected to each DC-link capacitor, considering the existence of a voltage balancing control. Figure 5.9 illustrates this scenario, where $P_j \leq P_r/2$, $j \in \{1, 2\}$.

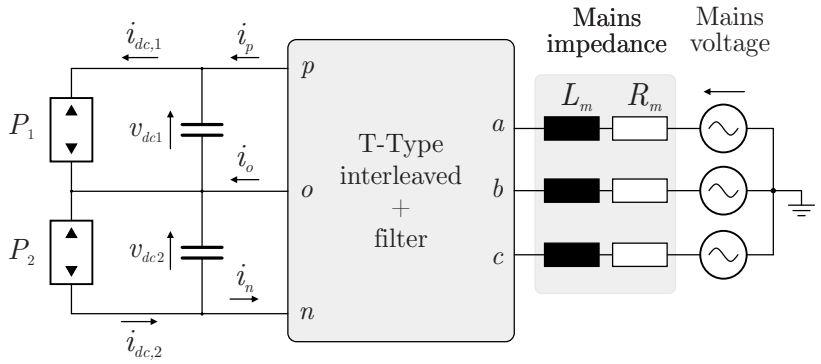


Figure 5.9 – Diagram of different power sources connected to the DC-link.

To validate this operation mode, a simulation was performed in PLECS and the results are shown in Figure 5.10. The simulation consisted in initializing the converter with $P_1 = P_2 = 5$ kW, and beginning at 1.2 s of simulation steps of -500 W were added to P_2. The mains voltage were considered free of harmonics. One can notice that the voltage

balancing control loop is capable of following the reference by inserting a 0-axis component to the current control until it reaches the minimum stable value of $P_2 = 2.5$ kW. The shift in the modulation signal caused by the voltage balance control causes the appearence of harmonics in the current that are not mitigated by the current control, resulting in a raise in the THD of the current in the mains. For nominal load ($P_1 + P_2 = 10$ kW), the THD of the mains current is 0.2078%, while for $P_2 = 2.5$ kW the THD increases to 1.5749%.

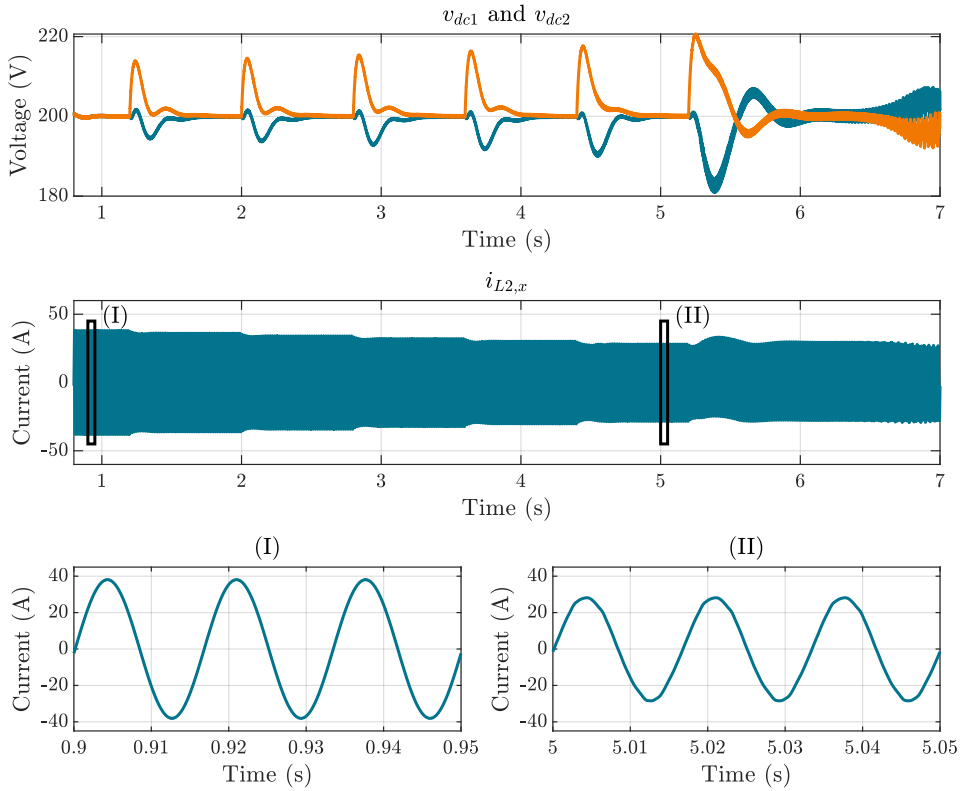


Figure 5.10 – Simulation results of the different loads connected to the DC-link operation mode.

The prediction of the difference between P_1 and P_2 that allows stable operation of the converter depends on a stability analysis of the converter under this specific condition. As stated on Chapter 4, the stability analysis is out of the scope of this work and therefore the precise limit was not be assessed.

5.2.3.3 Operation at weak grids

The proposed voltage compensation method injects reactive power into the mains and therefore when a weak grid is considered (SCR < 3), the required reactive power increases in order to compensate the voltage drop in the mains impedance. To illustrate this dynamic in the converter operation, a simulation was performed considering SCR $= 1.5$ and increasing power in the DC-link with power steps of +1 kW until the rated power of 10 kW. The mains voltage was considered with THD $= 8.73\%$. It can be noticed that the increasing active power requires the converter to inject more reactive power into the

mains in order to maintain the reference voltage over the filter capacitors. Moreover, the simulation showcased the reference tracking capability of the DC-link voltage during the load steps.

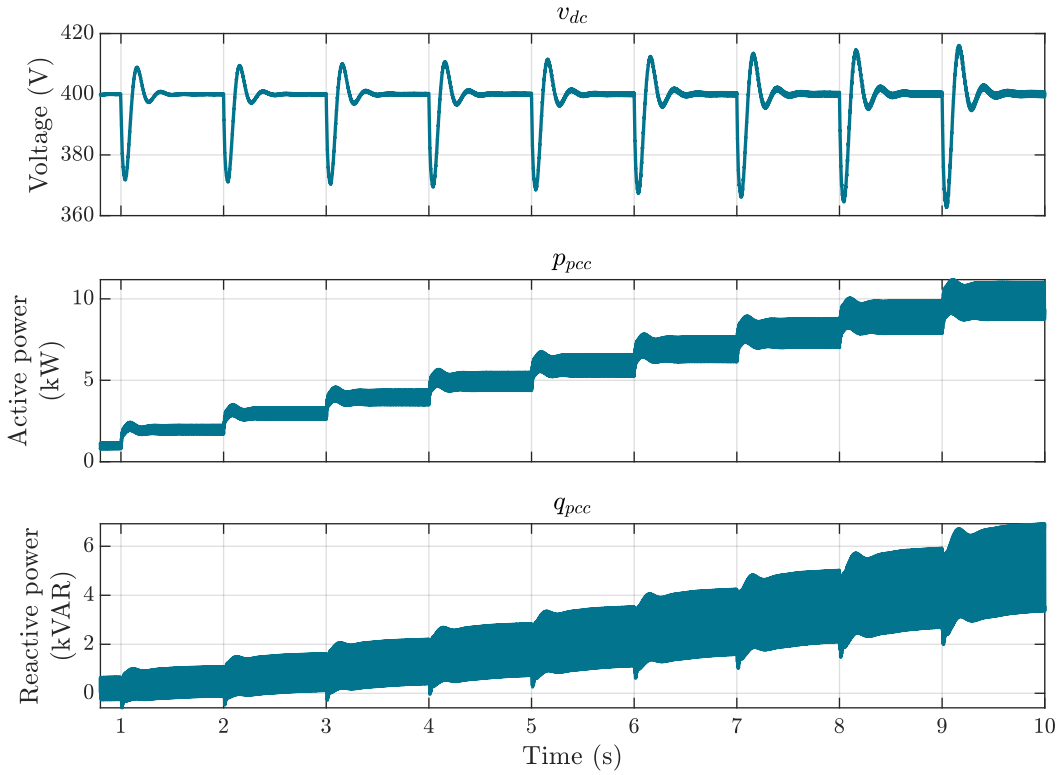


Figure 5.11 – Simulation results for +1 kW load steps to the converter on rectifier operation with SCR = 1.5.

Regarding the current and voltage on the PCC under a weak grid, Figure 5.12 shows the results of a simulation of consecutive load steps from 5 KW to the nominal power of 10 kW, considering SCR = 1.5. The mains voltage was still considered with THD = 8.73%. It can be seen that the increase in he active power causes the power factor to drop as a result of the PCC voltage compensation, reaching and average value of 0.8916 for rated active power.

5.2.4 Conclusion

This chapter presented the experimental results for the interleaved T-Type converter and showcased a comparison between the practical results and the theoretical waveforms. For the studied modulation strategies, the numerical model used to assess the converter was validated as the observed error is negligible and intrinsic to the experimental process. Regarding the comparison between the modulation strategies, DPWM showed slightly better efficiency and smaller current ripple, which suggests that the filter could be more compact if the optimization process considered this modulation strategy instead of the STHI.

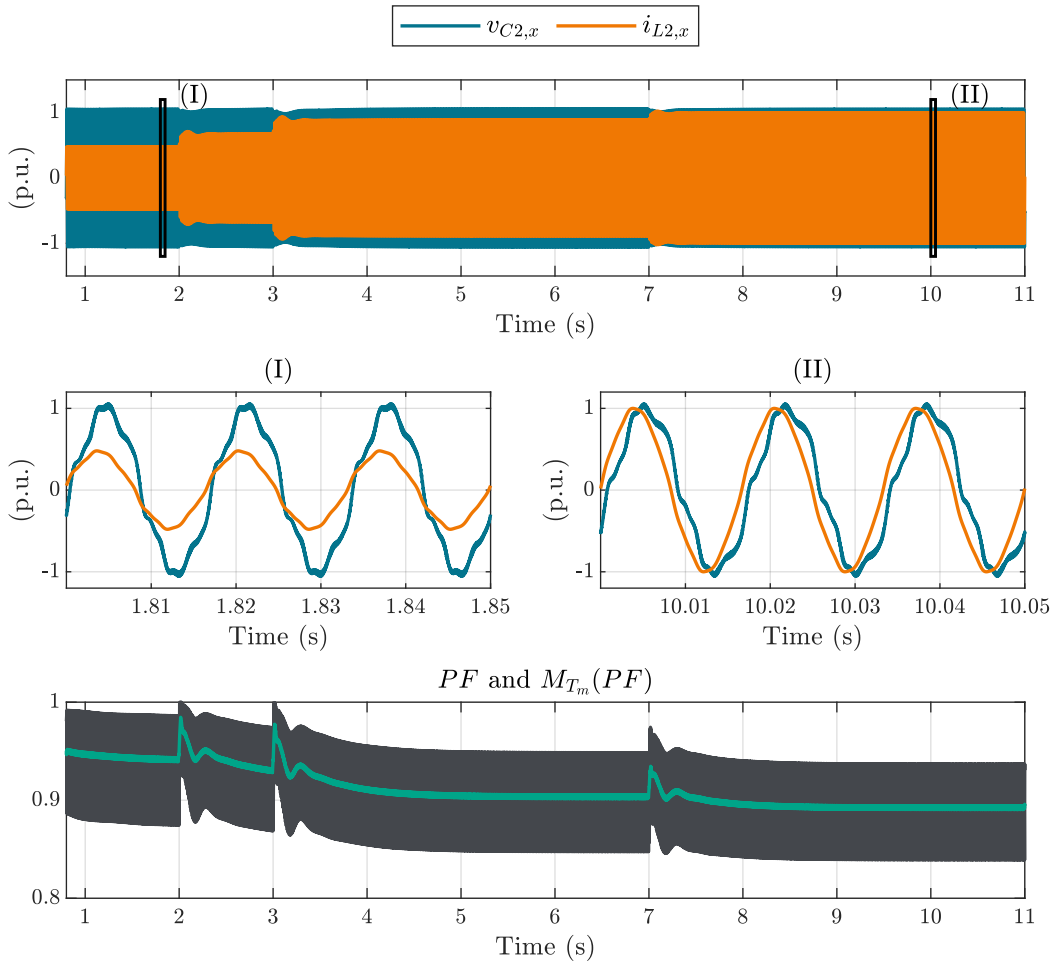


Figure 5.12 – Current and voltage on the PCC and power factor for consecutive load steps to the converter on rectifier operation with SCR = 1.5. On the top graph, the PCC voltage and current are normalized by the nominal phase voltage and current peak value, respectively.

With respect to the thermal assessment of the magnetic elements, it was observed compliance between the model and the experimental result for the boost inductor, whereas it was observed a large error in relation to the interphase transformers. The use of a single model to assess the temperature rise of different types of magnetic elements and the disregard for assembly aspects may have interfered with the accuracy of the model. Therefore, further improvement of the model is required

Chapter

6 Final Considerations

This work addressed several challenges associated with the modeling and design of the T-Type interleaved converter. Throughout the study, tools and methods for achieving a functional and efficcient converter were proposed, and their observed limitations were discussed.

In Chapter 2, a static analysis of the converter was conducted, involving mathematical modeling of electrical quantities for any number of interleaved modules. The proposed switched-level model was validated against established simulation software, demonstrating high fidelity. A limitation of the model was the simulation time, since the numerical integration carries increasing error, which limitates the fidelity of the model. Additionally, considerations were made regarding the coupling of the boost inductor, justifying the implementation choice of the proposed magnetic elements.

The analysis conducted in Chapter 2 was the base for the models used in the optimization process proposed in Chapter 3. This design process required power loss models to quantify the converter's efficiency and maximize it throughout the algorithm. Alongside power loss modeling, a simple thermal model was described and integrated into the optimization process to employ temperature rise of magnetic elements as a design constraint.

Chapter 4 presented a dynamic model of the converter to design an appropriate control strategy. A closed-loop model incorporating the proposed controllers was developed to observe system dynamics without reliance on switched-level simulation software and to tune controllers considering time-domain response. The proposed models demonstrated precision when compared to software simulation. Regarding the application of the proposed model to stability analysis, it was found that the time-variance observed in the model resulted in imprecise stability boundaries, making the models inadequate for such analysis.

Lastly, Chapter 5 showcased the prototype designed in Chapter 3 and experimentally validated the proposed converter under different modulation strategies, considering an open-loop inverter mode setup. Results indicated that the proposed model provided only an approximation of losses, as expected, given that it did not account for other sources

of losses such as damping resistors, common mode choke, and PCB losses. Furthermore, the assessment of the thermal model utilized in the optimization process revealed good compliance with experimental results for the toroidal core, but poor approximation for the double E core. This discrepancy may be caused by assembly choices that were not accounted for in the model, and altered the heat transfer dynamics of the magnetic element, but also by the model itself, which does not consider the whole geometry of the magnetic elements.

Furthermore, Chapter 5 also presented simulations to validate the proposed control strategy under different conditions and to analyze the effect of the third harmonic injection in the converter. The results showed that the converter is able to operate at rated active power under weak and with high harmonic content grid. Even though the proposed converter allows bidirectional power flow, the analysis performed in this section considered only rectifier operation. Therefore, specific control loops associated to inverter operation, such as anti-islanding, were not addressed.

Overall, this work presented models for initial assessment of converter waveforms, demonstrating accuracy with low computational effort. Therefore, the proposed objectives and contributions are considered achieved.

6.1 FUTURE WORK

As discussed in critical analysis in the last section, the presented results are valid but open for improvement. Therefore, the following topics are suggested as future improvements of this work:

- Improve the power loss models in the switching devices and magnetic elements to achieve greater fidelity with practical results;
- Design an EMI filter, required for compliance with related standards;
- Improve the thermal model to assess the temperature rise more accurately in the double E core inductor;
- Implement a modeling technique to make the dynamic model time-invariant without truncating its behavior for stability assessment of the proposed control strategy;
- Study and implement an anti-islanding method, which is mandatory for grid-connected operation;
- Experimentally validate the proposed control strategy using the designed prototype.

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APPENDIX

A Switched-level algorithm for numerical simulation of the T-Type interleaved converter

A.1 INTRODUCTION

This appendix discusses a proposed numerical approach for evaluating the switched waveforms of voltages and currents in the T-Type interleaved converter. The approach outlined here serves as an alternative to using simulation software. The routines presented in this work were implemented using MATLAB®, but they are presented as pseudocode to maintain generality.

A.2 ALGORITHM DESCRIPTION

Algorithm 4 shows how to obtain the phase voltages $\mathbf{v}_{xo}$ and switching functions $\mathbf{S}$ numerically over a mains period $\mathbf{t}$. It should be noted that $\mathbf{S}$ is a multidimensional matrix, where $\mathbf{S}(k, x, n, i)$ denotes the switching function value of the k-th switching device ($k \in \{1, 2, 3, 4\}$) in the phase x of the n-th module during the i-th time step of the simulated time. Moreover, the carriers matrix $\mathbf{c}_{PD}$ is also a multidimensional matrix, where $\mathbf{c}_{PD}(n, j, i)$ denotes the j-th carrier value ($j \in \{1, 2\}$, where 1 denotes the positive carrier and 2 denotes the negative one) for the n-th module in the i-th time step.

Algorithm 4 Phase voltages and switching functions matrices

Input: time vector $\mathbf{t}$, mains voltage matrix $\mathbf{v}_{abc}$, carriers matrix $\mathbf{c}_{PD}$, modulation signal matrix $\mathbf{d}_{abc}$, number of interleaved modules N;
Output: phase voltages matrix $\mathbf{v}_{xo}$ and switching functions matrix $\mathbf{S}$;
for $x = 1, \ldots, 3$ **do**
  for $n = 1, \ldots, N$ **do**
    for $i = 1, \ldots, \text{length}(\mathbf{t})$ **do**
      if $\mathbf{d}_{abc}(x, i) \geq 0$ **then**
        if $\mathbf{d}_{abc}(x, i) \geq \mathbf{c}_{PD}(n, 1, i)$ **then**
          $\mathbf{v}_{xo}((x-1)N + n, i) \leftarrow V_{dc}/2$;
          $\mathbf{S}(1, x, n, i) \leftarrow 1$;
          $\mathbf{S}(2, x, n, i) \leftarrow 0$;
          $\mathbf{S}(3, x, n, i) \leftarrow 0$;

```
                    S(4, x, n, i) ← 1;
                else
                    v_xo((x − 1)N + n, i) ← 0;
                    S(1, x, n, i) ← 1;
                    S(2, x, n, i) ← 0;
                    S(3, x, n, i) ← 0;
                    S(4, x, n, i) ← 1;
                end if
            else if c_PD(n, 2, i) ≥ d_abc(x, i) then
                v_xo((x − 1)N + n, i) ← −V_dc/2;
                S(1, x, n, i) ← 0;
                S(2, x, n, i) ← 1;
                S(3, x, n, i) ← 1;
                S(4, x, n, i) ← 0;
            else
                v_xo((x − 1)N + n, i) ← 0;
                S(1, x, n, i) ← 0;
                S(2, x, n, i) ← 1;
                S(3, x, n, i) ← 0;
                S(4, x, n, i) ← 1;
            end if
        end for
    end for
end for
```

With the phase voltages defined, it is possible to extract the additive and subtractive mode voltages from the phase voltages matrix $\mathbf{v}_{xo}$ by using Lunze's Transformation $\mathbf{T}_L$:

$$\mathbf{T}_L = \frac{1}{n}\begin{bmatrix} n-1 & -1 & \dots & -1 & -1 \\ -1 & n-1 & \dots & -1 & -1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -1 & -1 & \dots & n-1 & -1 \\ 1 & 1 & \dots & 1 & 1 \end{bmatrix}_{n\times n}. \tag{A.1}$$

With the additive and subtractive mode phase voltages, the differential mode voltage in the additive mode can be calculated through the differential transformation,

given by:

$$\mathbf{T}_{dm} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}. \tag{A.2}$$

Consequently, the additive and subtractive mode currents can be also inferred, for a given boost inductor L_b and an IT self-inductance L_s, by applying a numerical integration method. In this work, the Euler method was employed. Therefore, Algorithm 5 shows the numerical method for obtaining the boost inductor and the subtractive mode currents. Since the purpose of the algorithm is to showcase the method, only the boost inductor current in phase a and only one phase of the first subtractive mode equivalent circuit are calculated. The function RearrangeVector() used to rearrange the vector's elements as [23]:

$$\begin{aligned} \mathbf{d}^T_{3n,sm,am} &= [d_{1,sm,a}\ \ d_{2,sm,a}\ldots d_{am,a}\ \ d_{1,sm,b}\ \ d_{2,sm,b}\ldots d_{am,b}\ \ d_{1,sm,c}\ \ d_{2,sm,c}\ldots d_{am,c}]^T \\ &\downarrow \\ \mathbf{d}^T_{3n,sm,am} &= [d_{1,sm,a}\ \ d_{1,sm,b}\ \ d_{1,sm,c}\ \ d_{2,sm,a}\ \ d_{2,sm,b}\ \ d_{2,sm,c}\ldots d_{am,a}\ \ d_{am,b}\ \ d_{am,c}]^T. \end{aligned} \tag{A.3}$$

Algorithm 5 Inductors voltage and current

1: **Input**: phase voltage matrix $\mathbf{v}_{xo}$, Lunze's Transformation $\mathbf{T}_L$, differential mode transformation T_{dm}, mains phase voltage vector $\mathbf{v}_a$, boost inductor L_b, IT self-inductance L_s, number of interleaved modules N, time vector $\mathbf{t}$;
2: **Output**: additive and subtractive mode voltages $\mathbf{v}_{dm,am}$, boost inductor current $\mathbf{i}_{Lb}$, circulation current $\mathbf{i}_{Ls}$;
3: $\mathbf{v}_{sm,am} \leftarrow$ RearrangeVector $[(\mathbf{I}_3 \otimes \mathbf{T}_L)\,\mathbf{v}_{xo}]$;
4: $\mathbf{v}_{am} = \mathbf{v}_{sm,am}(end-2:end,:)$;
5: $\mathbf{v}_{sm,1} = \mathbf{v}_{sm,am}(1:3,:)$;
6: $\mathbf{v}_{dm,am} \leftarrow \mathbf{T}_{dm}\mathbf{v}_{am}$;
7: $\mathbf{v}_{Lb} = \mathbf{v}_a - \mathbf{v}_{dm,am}(1,:)$;
8: **for** $i = 2,\ldots,\text{length}(t)-1$ **do**
9: $\quad \mathbf{i}_{Lb}(k) = \mathbf{i}_{Lb}(k-1) + (\mathbf{t}(k) - \mathbf{t}(k-1))\,\mathbf{v}_{L1}(k)/L_b$;
10: **end for**
11: $\mathbf{v}_{Ls} = \mathbf{v}_{sm,1}(1,:)$;
12: **for** $i = 2,\ldots,\text{length}(t)-1$ **do**
13: $\quad \mathbf{i}_{Ls}(k) = \mathbf{i}_{Ls}(k-1) + (\mathbf{t}(k) - \mathbf{t}(k-1))\,\mathbf{v}_{Ls}(k)/(N-1)/N/L_s$;
14: **end for**

A.3 CONCLUSION

The presented numerical method offers flexibility in terms of parameters and modulation strategies employed, as long as it is a carrier-based modulation. Obtaining the switching functions of semiconductors during the mains period was also essential to the optimization process discussed in Chapter 3. The routine involved calculating FFT to assess winding losses and piece-wise calculation of core losses. By considering only the switching points and disregarding the intermediary ones, the computation effort could be significantly reduced. This feature proved fundamental to the optimization, as it affected directly the convergence time of the routine.

APPENDIX

B

dq0-axes model of the T-Type interleaved converter

$$
\begin{cases}
\mathbf{v}_{dq0} = (R_m + R_{L2})\,\mathbf{i}_{L2,dq0} + (L_m + L_g)\left[D_t\mathbf{i}_{L2,dq0} + \boldsymbol{\Theta}\mathbf{i}_{L2,dq0}\right] + R_{C2}C_2\left[D_t\mathbf{v}_{C2,dq0} + \boldsymbol{\Theta}\mathbf{v}_{C2,dq0}\right] + \mathbf{v}_{C2,dq0} \\
\dfrac{v_{dc}}{2}\mathbf{d}_{dq0,am} = -nR_{L1}\mathbf{i}_{dq0,am} - n\,L_1\left[D_t\mathbf{i}_{dq0,am} + \boldsymbol{\Theta}\mathbf{i}_{dq0,am})\right] + R_{C2}C_2\left[D_t\mathbf{v}_{C2,dq0} + \boldsymbol{\Theta}\mathbf{v}_{C2,dq0}\right] + \mathbf{v}_{C2,dq0} \\
C_2\left[D_t\mathbf{v}_{C2,dq0} + \boldsymbol{\Theta}\mathbf{v}_{C2,dq0}\right] = \mathbf{i}_{L2,dq0} - n\,\mathbf{i}_{dq0,am} - \left[\mathbf{v}_{C2,dq0} + R_{C2}C_2D_t\mathbf{v}_{C2,dq0} + R_{C2}C_2\boldsymbol{\Theta}\mathbf{v}_{C2,dq0} - \mathbf{v}_{C1,dq0}\right]\dfrac{1}{R_d + R_{C1}} \\
C_1\left[D_t\mathbf{v}_{C1,dq0} + \boldsymbol{\Theta}\mathbf{v}_{C1,dq0}\right] = \left[\mathbf{v}_{C2,dq0} + R_{C2}C_2D_t\mathbf{v}_{C2,dq0} + R_{C2}C_2\boldsymbol{\Theta}\mathbf{v}_{C2,dq0} - \mathbf{v}_{C1,dq0}\right]\dfrac{1}{R_d + R_{C1}} \\
\dfrac{v_{dc}}{2}\mathbf{d}_{i,dq0,sm} = \dfrac{(n-2)\,L_b + n\,L_s}{n-1}\left(D_t\mathbf{i}_{i,dq0,sm} + \boldsymbol{\Theta}\mathbf{i}_{i,dq0,sm}\right) + r_{w,bs}\mathbf{i}_{i,dq0,sm} \\
C_bD_tv_{dc} = -2\,\dfrac{P_r}{v_{dc}} + \mathbf{d}_{3n,sm,am,dq0}^{T}\left[(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})^T(\mathbf{I}_3 \otimes \boldsymbol{\Gamma})_R(\mathbf{I}_n \otimes \mathbf{T}_P^{-1}) - \dfrac{\Delta v_{dc}}{v_{dc}}(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})^T\boldsymbol{\Lambda}_R(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})\right]\mathbf{i}_{3n,sm,am,dq0} \\
C_bD_t\Delta v_{dc} = -\mathbf{d}_{3n,sm,am,dq0}^{T}\left[(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})^T\boldsymbol{\Lambda}_R(\mathbf{I}_n \otimes \mathbf{T}_P^{-1}) - \dfrac{\Delta v_{dc}}{v_{dc}}(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})^T(\mathbf{I}_3 \otimes \boldsymbol{\Gamma})_R(\mathbf{I}_n \otimes \mathbf{T}_P^{-1})^T\right]\mathbf{i}_{3n,sm,am,dq0}
\end{cases}
$$

The matrix $\mathbf{\Theta}$ represents the coupling between the d and q axes caused by Park's Transformation and is given by:

$$\mathbf{\Theta} = \mathbf{T}_P \, D_t \, \mathbf{T}_P^{-1} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

where ω is the mains angular velocity.

In the presented model, the boost inductor and its associated series resistance are denoted by L_1 and R_{L1} respectively. This notation ensures generality regarding the implementation of the boost inductor. Consequently, whether a single winding or a coupled boost inductor is employed, its equivalent can be substituted into the model without requiring further modifications.

APPENDIX

C

Closed-loop model validation

C.1 INTRODUCTION

This appendix is dedicated to the validation of the closed-loop model of the T-Type interleaved converter developed in Chapter 4, considering the proposed control strategy and controllers design. In this context, the model is compared to switched-level PLECS® simulations in different scenarios: Load steps, DC-link voltage reference step and q-axis additive current reference step. Figures of merit such as THD and harmonic profile are compared to endorse the analysis. One should notice that the presented model consider SPWM and, therefore, the PLECS® simulations were designed in accord. The simulations started at rated load and with the mains voltage configured to have THD = 8.69% and present 5-th, 7-th and 11-th order positive sequence harmonics unless said otherwise.

C.2 SIMULATIONS

C.2.1 Load steps

The simulation consisted of adding a load step of -1 kW at 1 s of simulation and another step of +1 kW at 1.5 s. The results of the simulation for the mains side current i_{L2} are shown in Figure C.1, highlighting the dynamic behavior of i_{L2} during the load steps.

To further endorse the validity of the model, the harmonic profile in both simulations is compared in Figure C.2, where the model presents THD = 1.69% and the PLECS® simulation result presents THD = 1.81%. The difference observed in the THD can be assigned to the presence of high frequency harmonics associated with the switching process in the PLECS® simulation result whereas the model is free of these components as it results from a dynamic average model considering the switching frequency period the averaging window. Also, for the low frequency harmonics, the model fidelity is limited to the employed simulation step and computational capacity available.

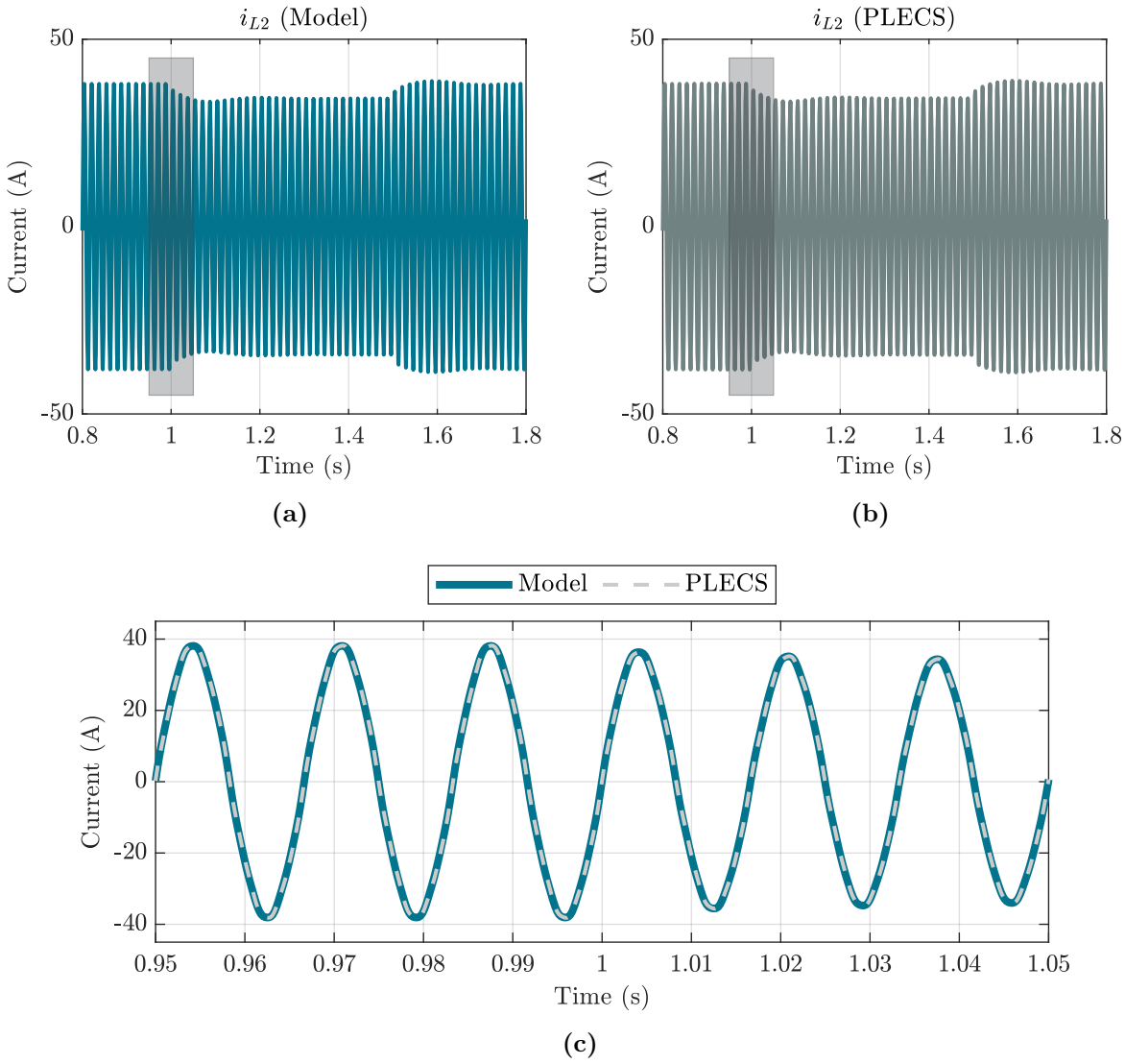


Figure C.1 – Grid side current i_{L2} from model (a) and from PLECS simulation (b) for -1 kW load step at 1 s and +1 kW load step at 1.5 s of simulation. Detail of highlighted area comparing both model and PLECS results during the -1 kW load step (c).

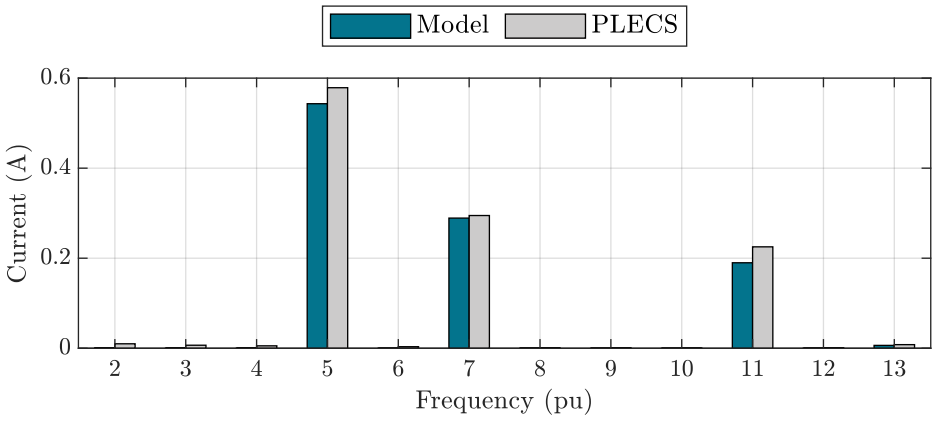


Figure C.2 – Comparison between the harmonic profile of i_{L2} from the model and from PLECS simulation considering the low frequency harmonics, where the base frequency is the mains frequency, i.e. $f_{base} = 60$ Hz.

Regarding the DC-link voltage dynamic behavior during the load steps Figure C.3 depicts the comparison between the model and the PLECS® simulation result. In relation to the voltage unbalance between the DC-link capacitors Δv_{dc}, Figure C.4 illustrates the results. One can infer that for load steps, the presented model is capable of represent the T-Type interleaved converter with fidelity in the low frequency part of the spectrum.

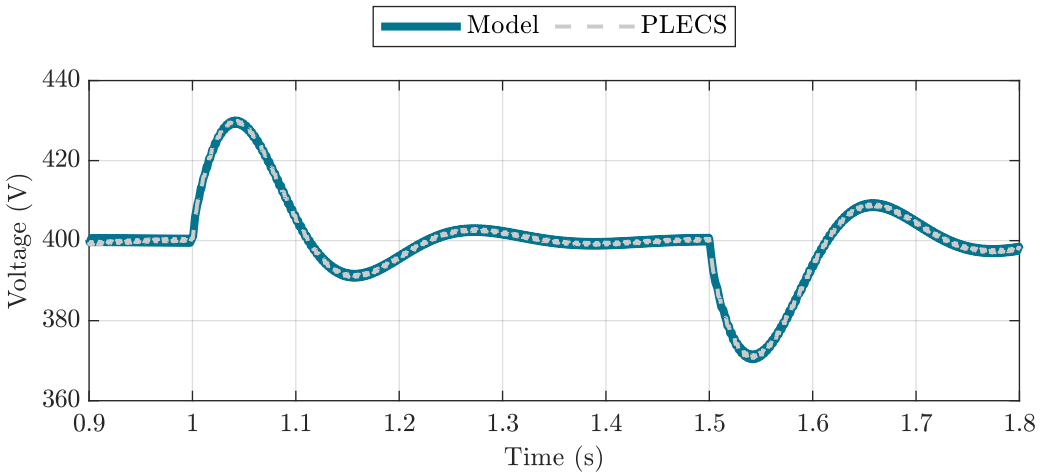


Figure C.3 – Comparison between the dynamic behavior of v_{dc} from the model and from PLECS simulation for -1 kW load step at 1 s and +1 kW load step at 1.5 s of simulation.

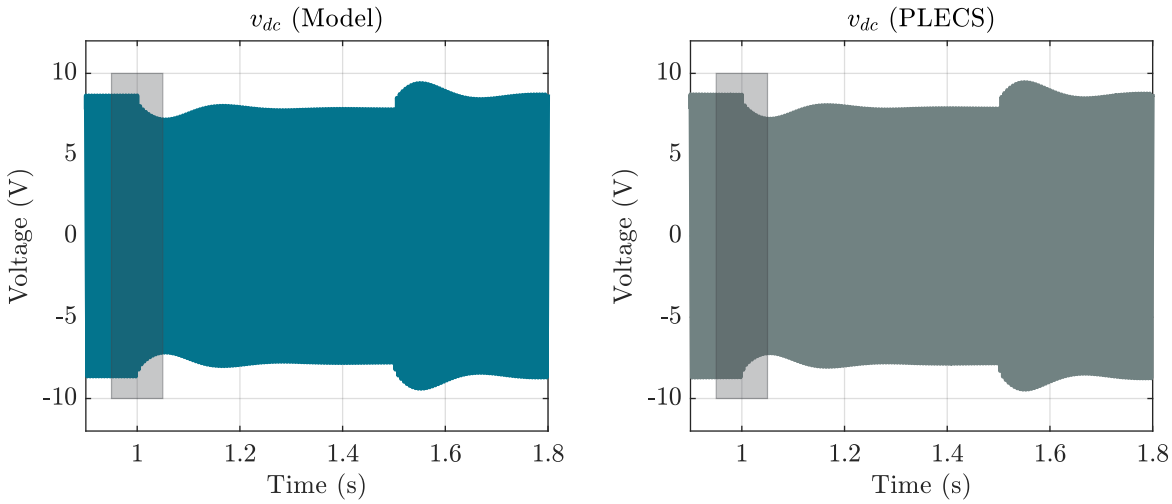
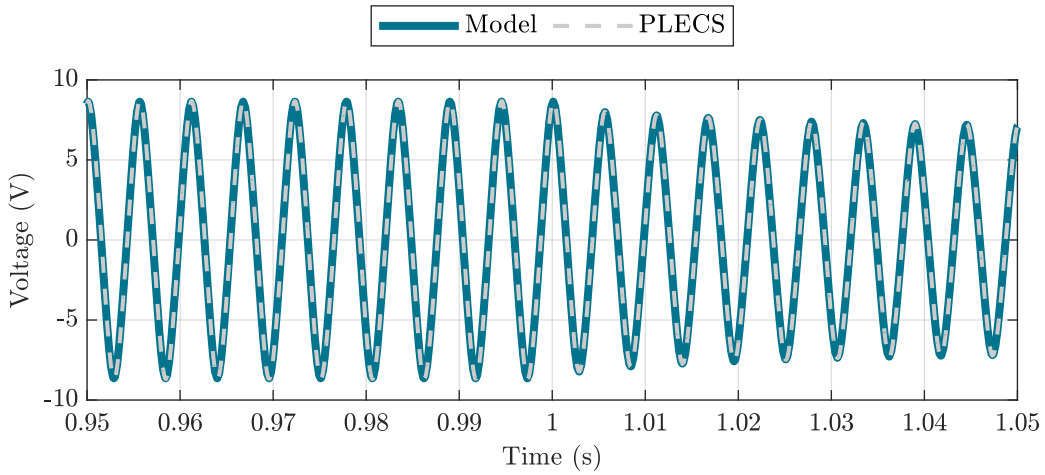


Figure C.4 – Voltage unbalance Δv_{dc} from model (a) and from PLECS simulation (b) for -1 kW load step at 1 s and +1 kW load step at 1.5 s of simulation. Detail of highlighted area comparing both model and PLECS results during the -1 kW load step (c).

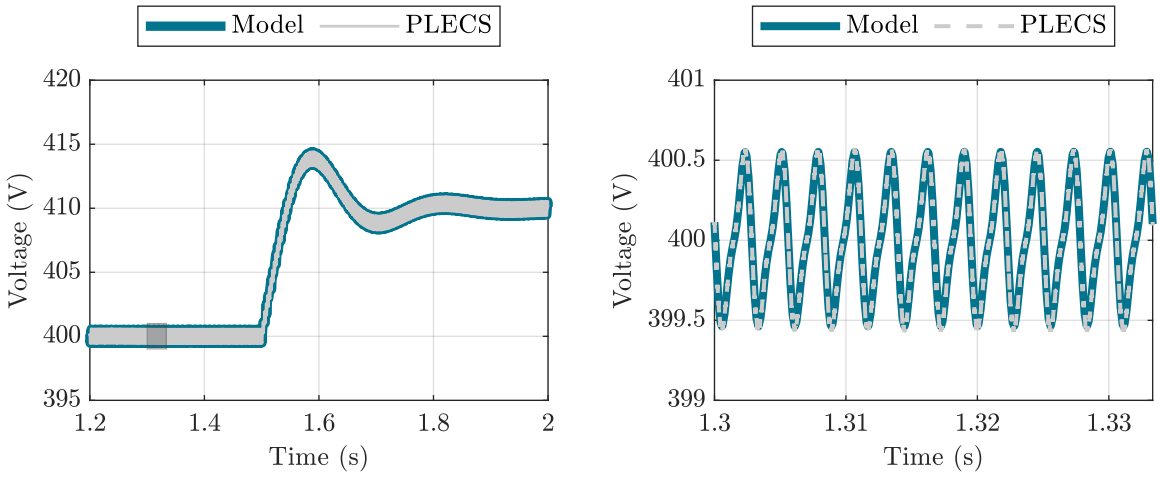


(c)

Figure C.4 – Voltage unbalance Δv_{dc} from model (a) and from PLECS simulation (b) for -1 kW load step at 1 s and +1 kW load step at 1.5 s of simulation. Detail of highlighted area comparing both model and PLECS results during the -1 kW load step (c).

C.2.2 DC-link voltage reference steps

The simulation consisted of adding a DC-link voltage reference step of +10 V at 1.5 s of simulation. The results of the simulation for the DC-link voltage v_{dc} are shown in Figure C.5, highlighting the dynamic behavior of v_{dc} during the reference step.



(a) **(b)**

Figure C.5 – Comparison between the dynamic behavior of v_{dc} from the model and from PLECS simulation for 10 V step at the DC-link voltage reference at 1.5 s of simulation.

C.2.3 Q-axis additive mode current reference step

The simulation consisted of adding a q-axis additive mode current reference step of +10 A at 1.2 s of simulation. The results of the simulation for the DC-link voltage v_{dc}

are shown in Figure C.5.

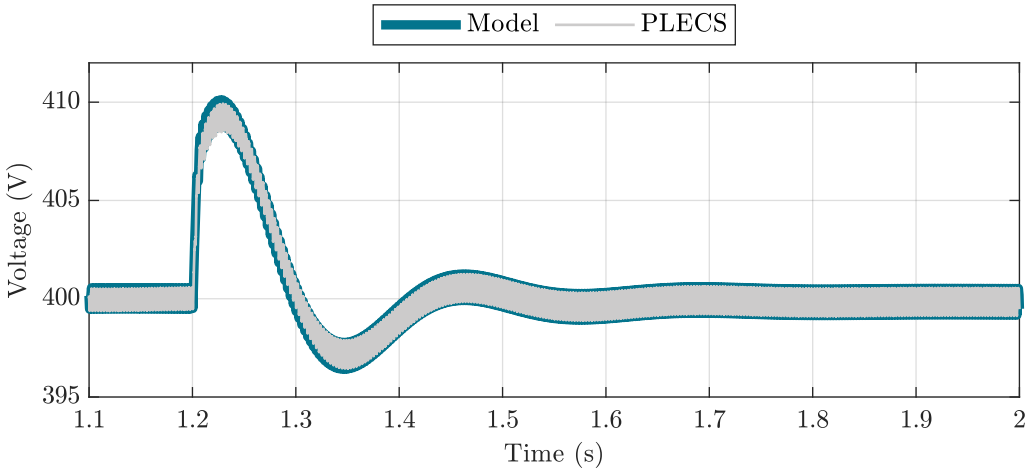
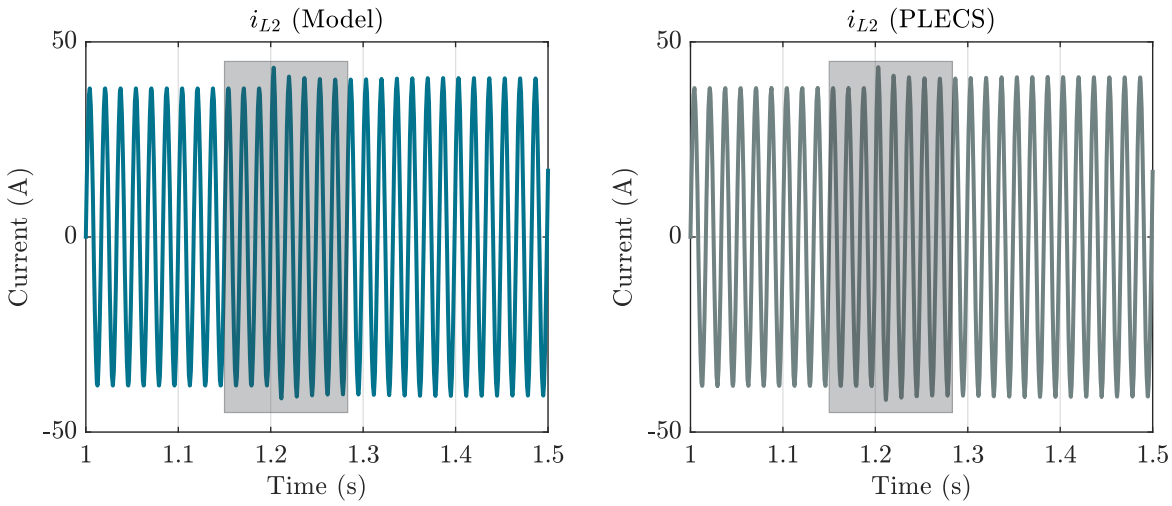


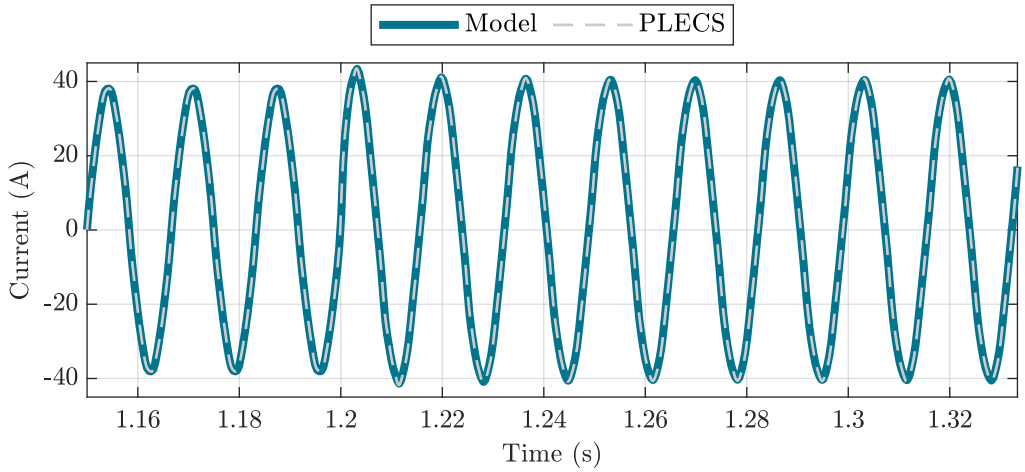
Figure C.6 – Comparison between the dynamic behavior of v_{dc} from the model and from PLECS simulation for +10 A q-axis additive mode current reference step at 1.2 s of simulation.

Regarding the mains side current i_{L2}, Figure C.7 depicts the comparison between the model and the PLECS® simulation result, highlighting the dynamic behavior of i_{L2} during the reference step.



(a) **(b)**

Figure C.7 – Grid side current i_{L2} from model (a) and from PLECS simulation (b) for +10 A q-axis additive mode current reference step at 1.2 s of simulation. Detail of highlighted area comparing both model and PLECS results during the reference step (c).



(c)

Figure C.7 – Grid side current i_{L2} from model (a) and from PLECS simulation (b) for +10 A q-axis additive mode current reference step at 1.2 s of simulation. Detail of highlighted area comparing both model and PLECS results during the reference step (c).

C.3 CONCLUSION

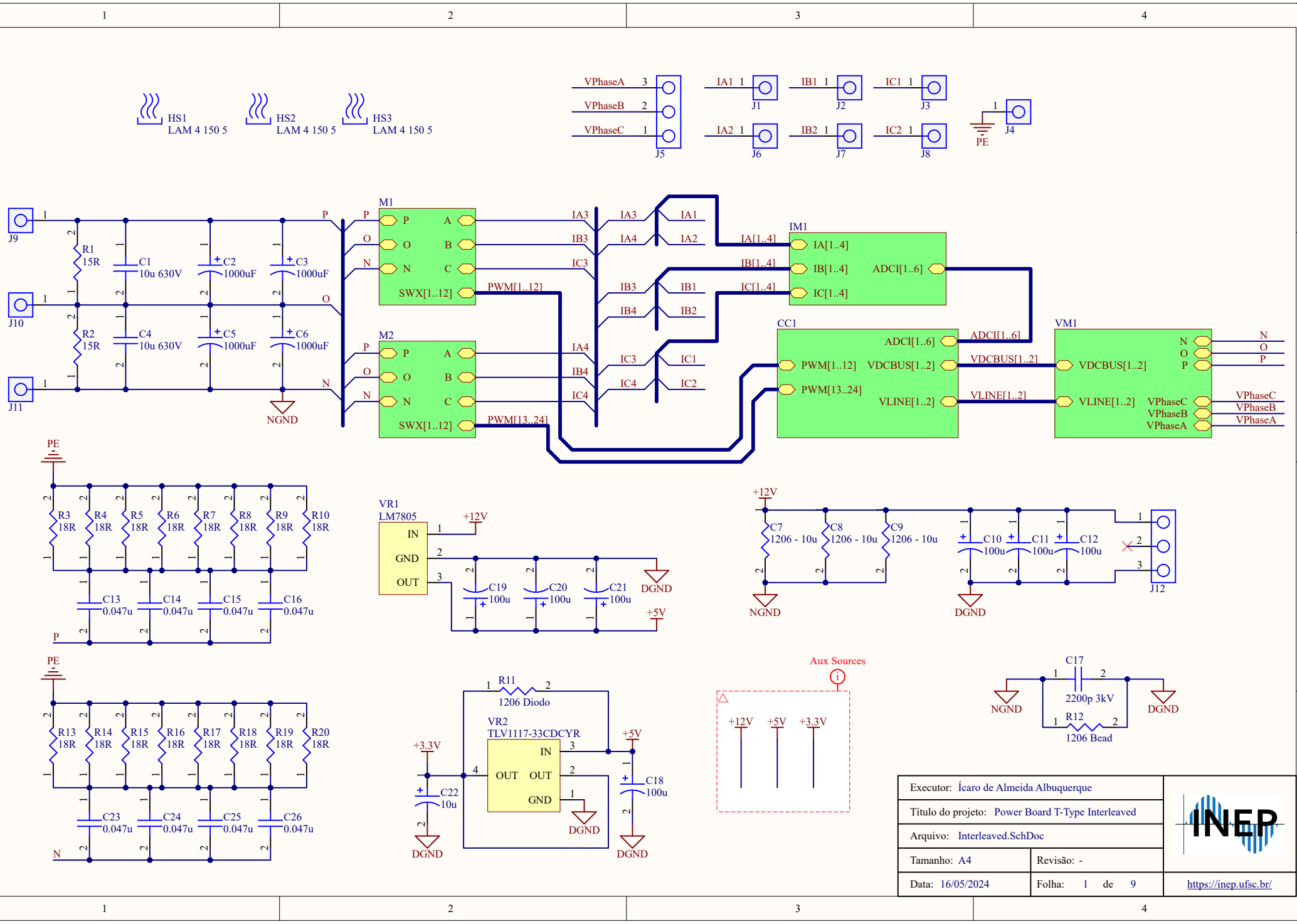
This appendix presented the validation of the closed-loop model developed alongside with the control strategy and controllers designed in Chapter 4 and the results endorse the fidelity of the model in comparison to a switched-level simulation developed in PLECS®. The limitations of the presented model in representing the behavior of the converter are: the exclusion of the high-frequency content of the converter, as it derives from a dynamic-average model and the computational burden required to use the model with high fidelity regarding harmonic content. Another modeling methods, such as Dynamic Phasors (DP) or Harmonic State-Space (HSS) could be employed to compensate this mitigation [65]. Another limitation that could be pointed in the model is the dynamics on the Dc-link unbalance voltage, witch are consistent around the rated point where $\Delta v_{dc,ref} = 0$, but loses fidelity for different points, as the switched-level simulation cannot impose different voltages for each mains half-cylce without generating a DC component in the mains current. However, as the model was developed for control tuning and empirical stability analysis purposes, it was considerate validated.

APPENDIX

D

Prototype schematics

This appendix is dedicated to the schematics of the prototype boards developed to experimentally test the T-Type interleaved converter that was designed in this work, namely, the power board, the filter and gate driver. Since the prototype consisted in the first version, some practical issues were identified during testing phase, and thus the employed solutions are commented throughout the schematics.



Executor: Ícaro de Almeida Albuquerque	
Título do projeto: Power Board T-Type Interleaved	
Arquivo: Interleaved.SchDoc	
Tamanho: A4	Revisão: -
Data: 16/05/2024	Folha: 1 de 9

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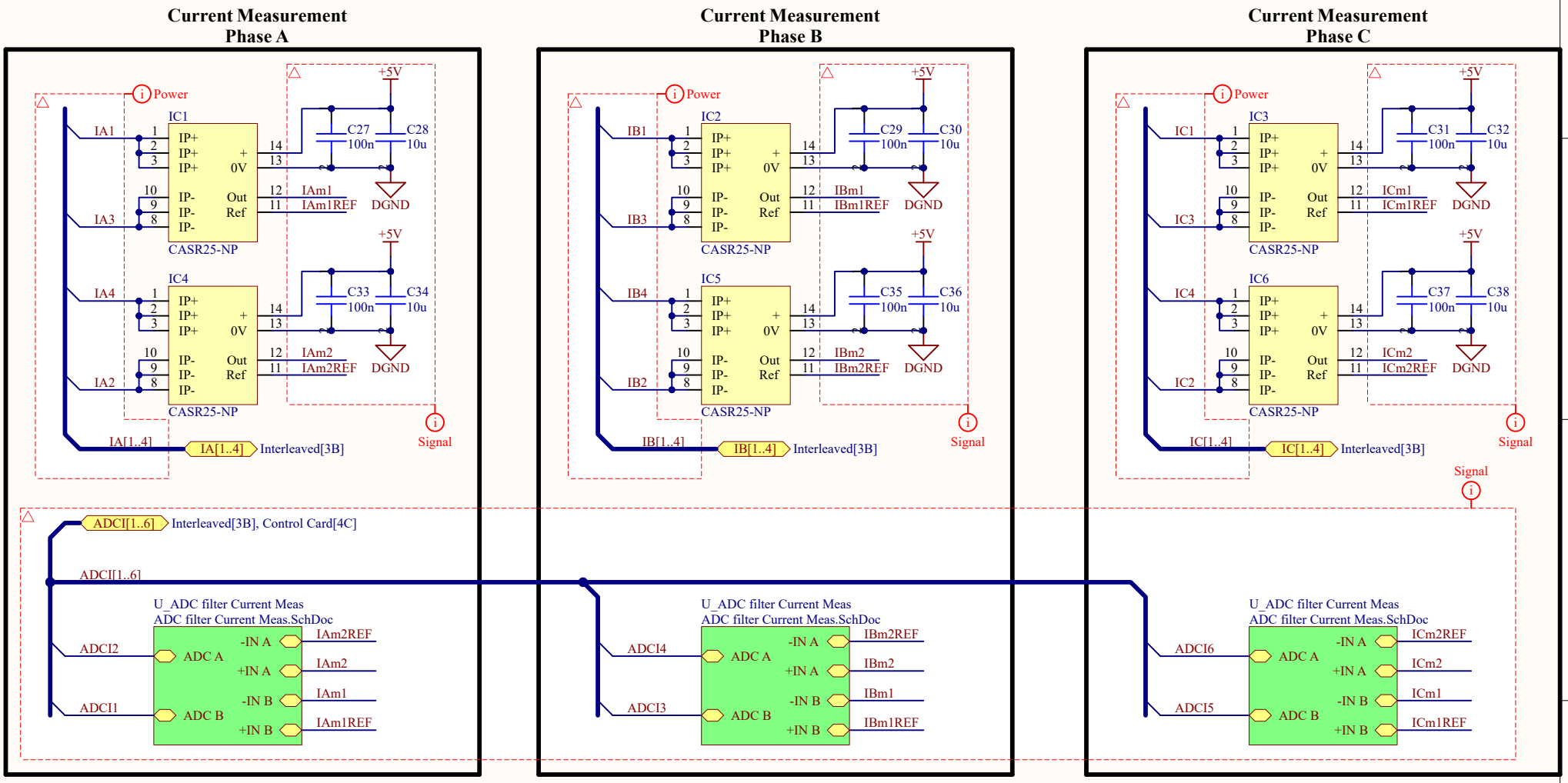
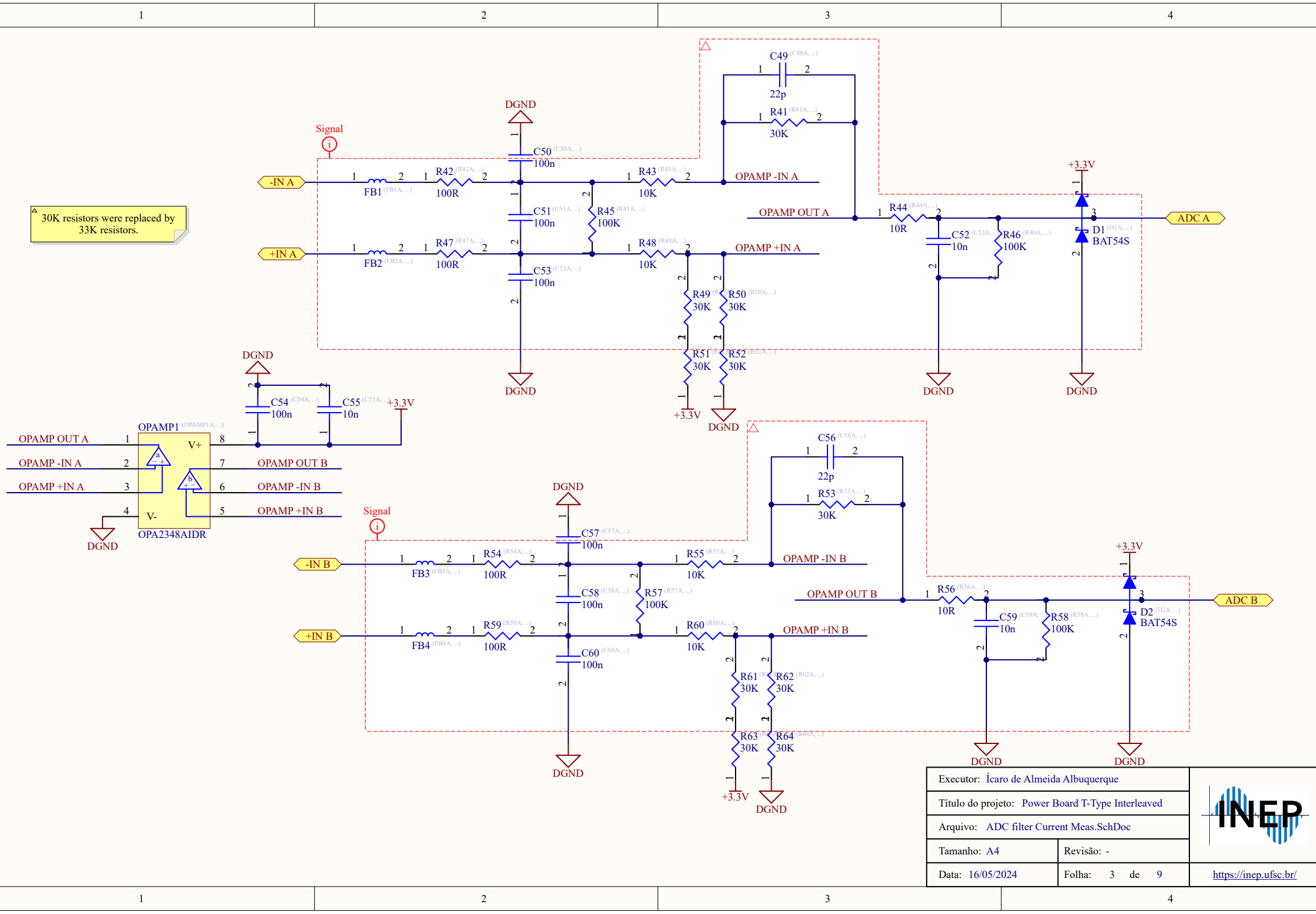
The current sensors have negative readings: the input and reference pins are swapped. Compensation in code is required.



Executor: Ícaro de Almeida Albuquerque		INEP
Título do projeto: Power Board T-Type Interleaved		
Arquivo: Current Measurement.SchDoc		
Tamanho: A4	Revisão: -	
Data: 16/05/2024	Folha: 2 de 9	https://inep.ufsc.br/


30K resistors were replaced by 33K resistors.
Signal
-IN A
+IN A
FB1
FB2
R42
R43
R47
R48
100R
10K
C50
C51
C53
100n
R45
100K
C49
22p
R41
30K
OPAMP -IN A
OPAMP +IN A
OPAMP OUT A
R44
10R
C52
10n
R46
100K
D1
BAT54S
ADC A
+3.3V
DGND
R49
R50
R51
R52
30K
C54
C55
OPAMP1
OPAMP OUT A
OPAMP -IN A
OPAMP +IN A
V+
V-
OPAMP OUT B
OPAMP -IN B
OPAMP +IN B
OPA2348AIDR
Signal
-IN B
+IN B
FB3
FB4
R54
R55
R59
R60
C57
C58
C60
R57
OPAMP -IN B
OPAMP +IN B
C56
R53
OPAMP OUT B
R56
C59
R58
D2
BAT54S
ADC B
R61
R62
R63
R64
Executor: Ícaro de Almeida Albuquerque
Título do projeto: Power Board T-Type Interleaved
Arquivo: ADC filter Current Meas.SchDoc
Tamanho: A4
Revisão: -
Data: 16/05/2024
Folha: 3 de 9
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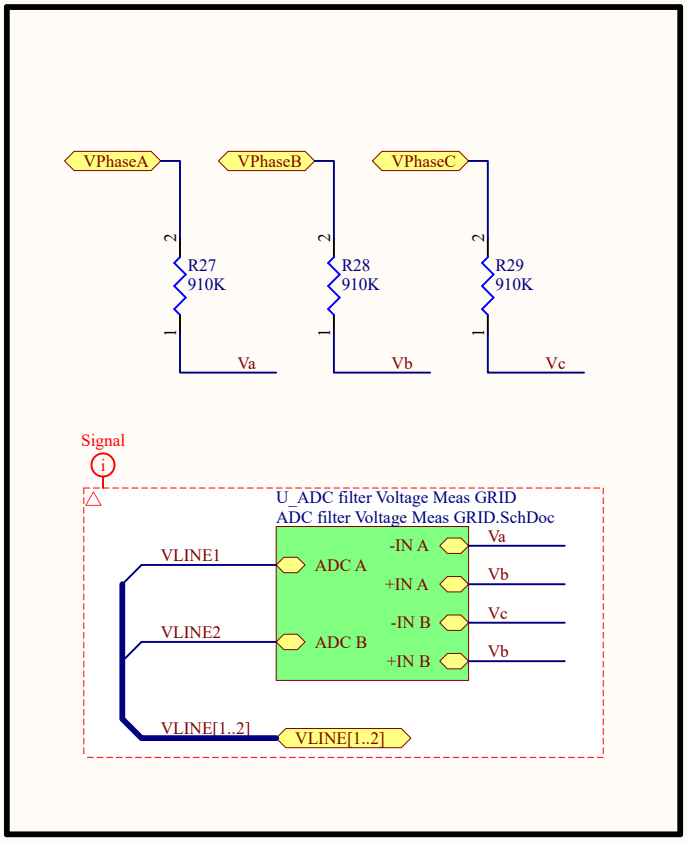
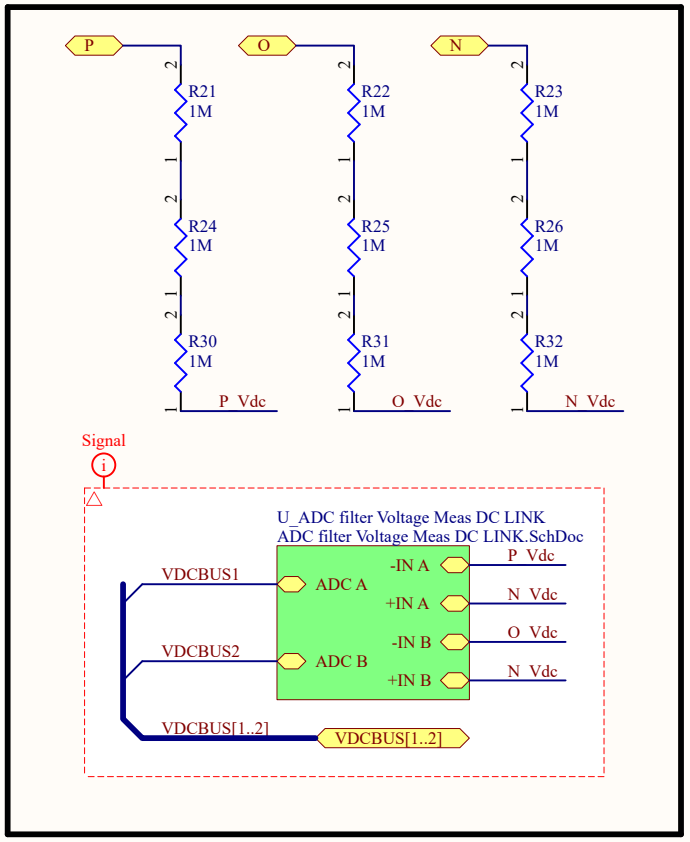
Grid Line Voltage Measurement

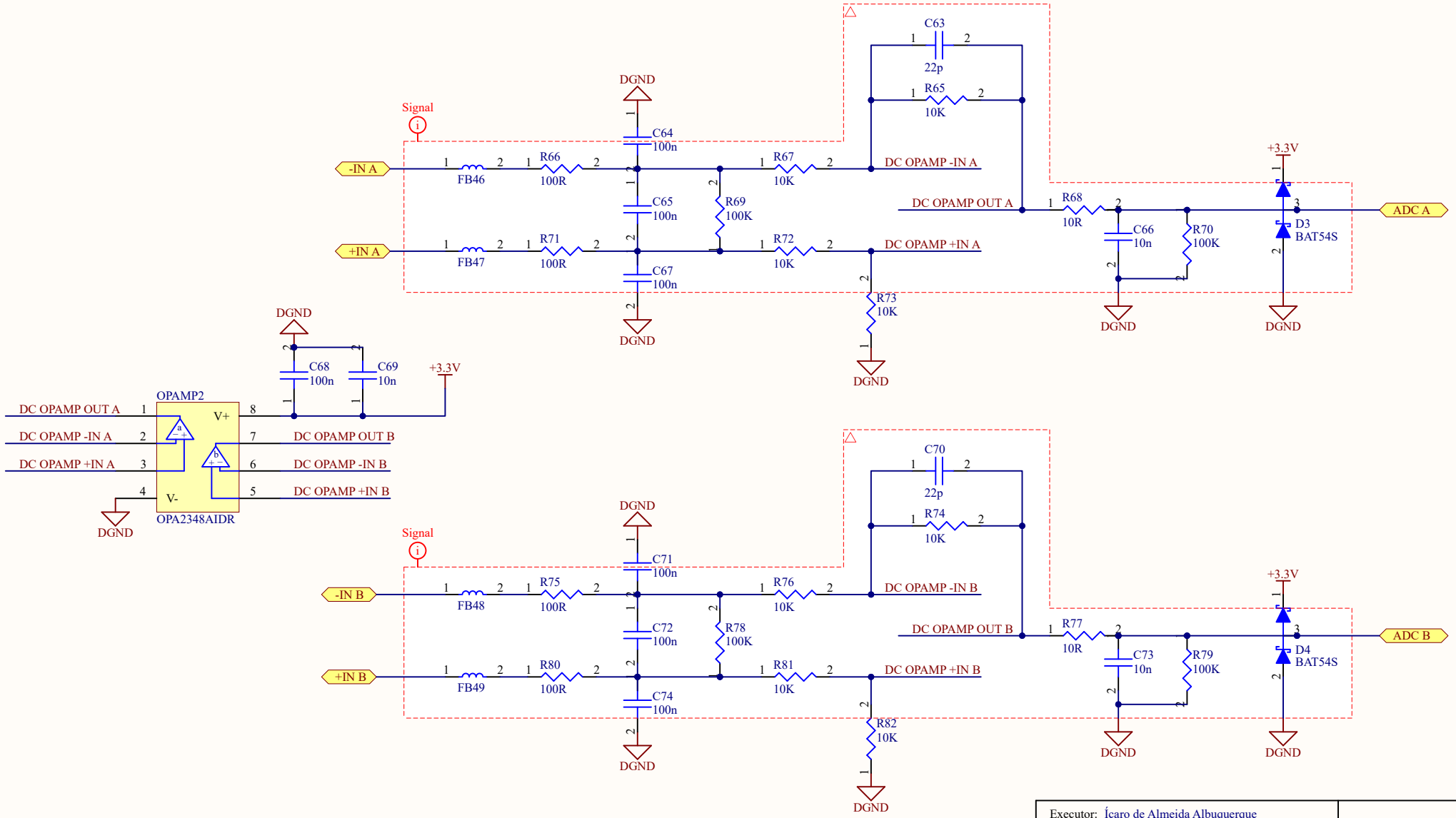


DC-Link Voltage Measurement



Obs.: DC-link voltage measurement is inverted and required practical intervention on PCB.

Executor: Ícaro de Almeida Albuquerque		INEP
Título do projeto: Power Board T-Type Interleaved		
Arquivo: Voltage Measurement.SchDoc		
Tamanho: A4	Revisão: -	
Data: 16/05/2024	Folha: 4 de 9	https://inep.ufsc.br/



Executor: Ícaro de Almeida Albuquerque	
Título do projeto: Power Board T-Type Interleaved	
Arquivo: ADC filter Voltage Meas DC LINK.SchDoc	
Tamanho: A4	Revisão: -
Data: 16/05/2024	Folha: 5 de 9

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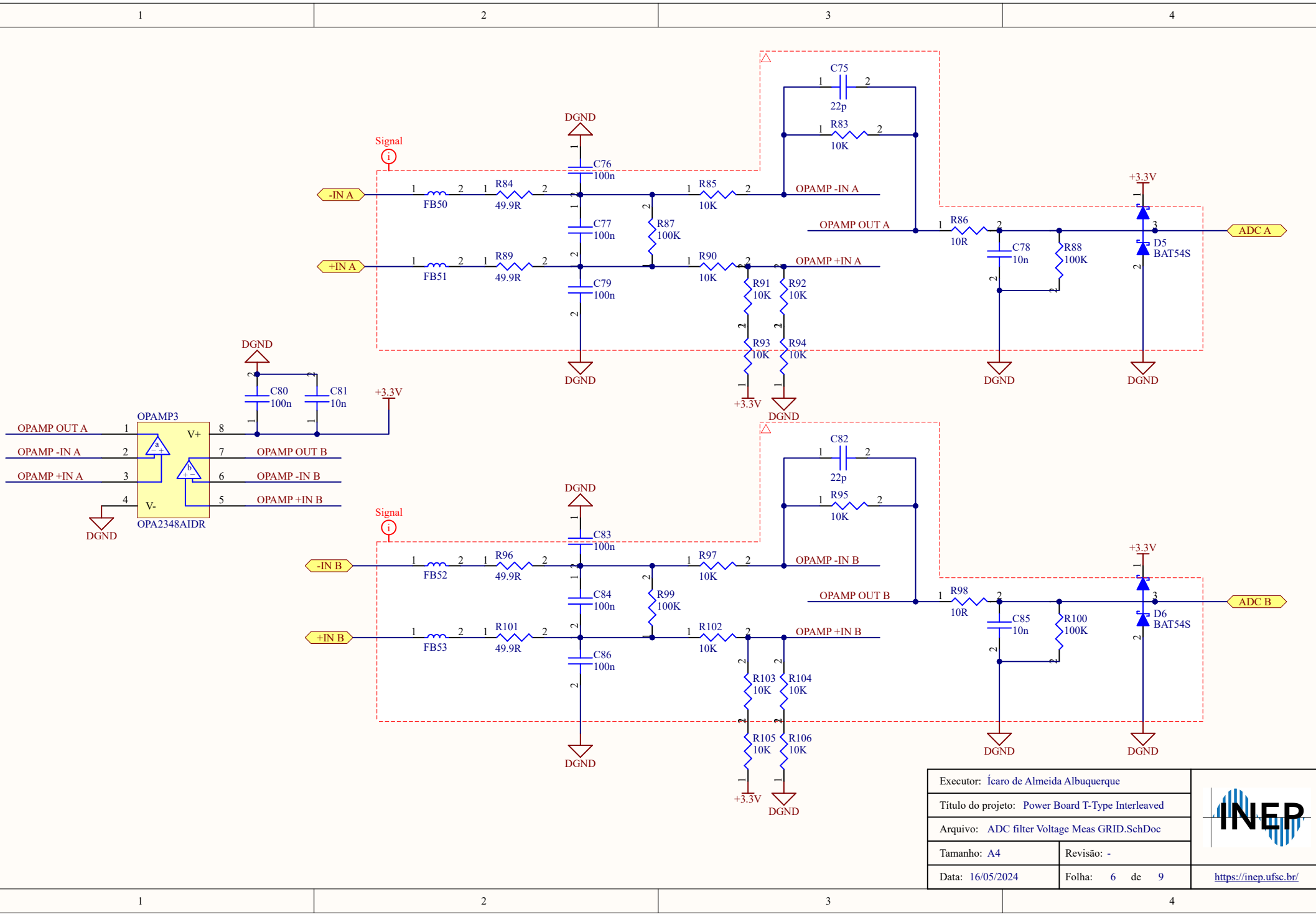

Executor: Ícaro de Almeida Albuquerque	
Título do projeto: Power Board T-Type Interleaved	
Arquivo: ADC filter Voltage Meas GRID.SchDoc	
Tamanho: A4	Revisão: -
Data: 16/05/2024	Folha: 6 de 9

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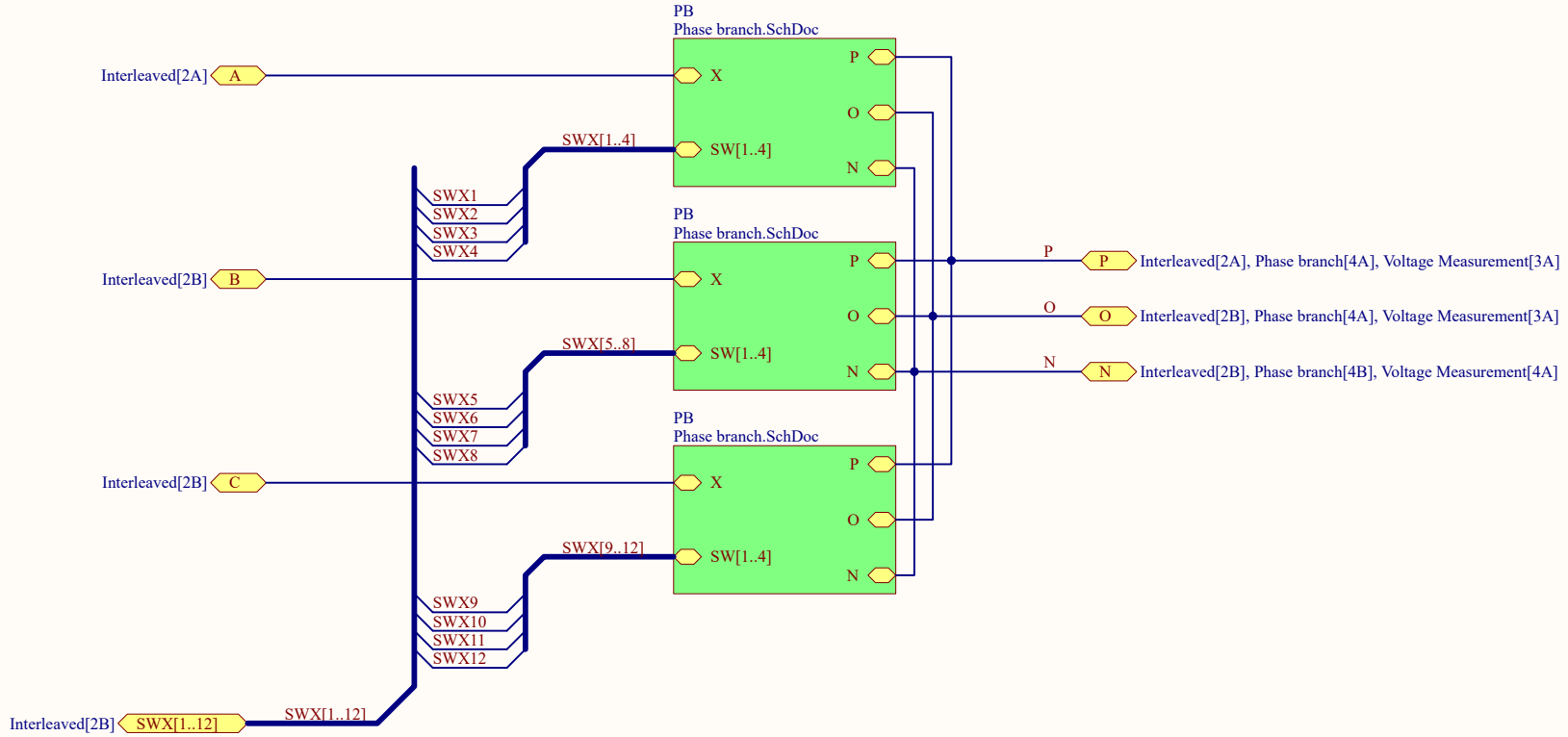
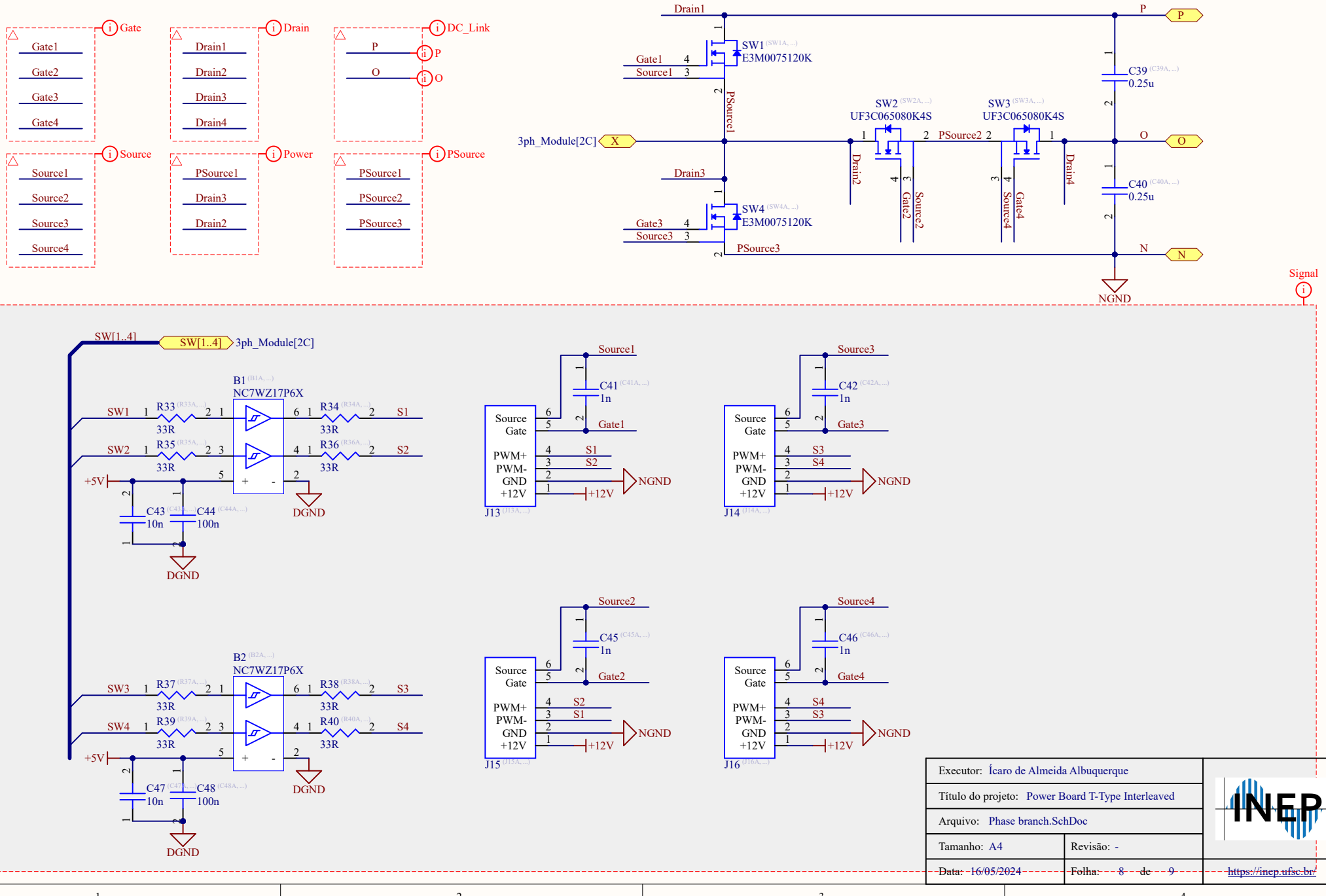
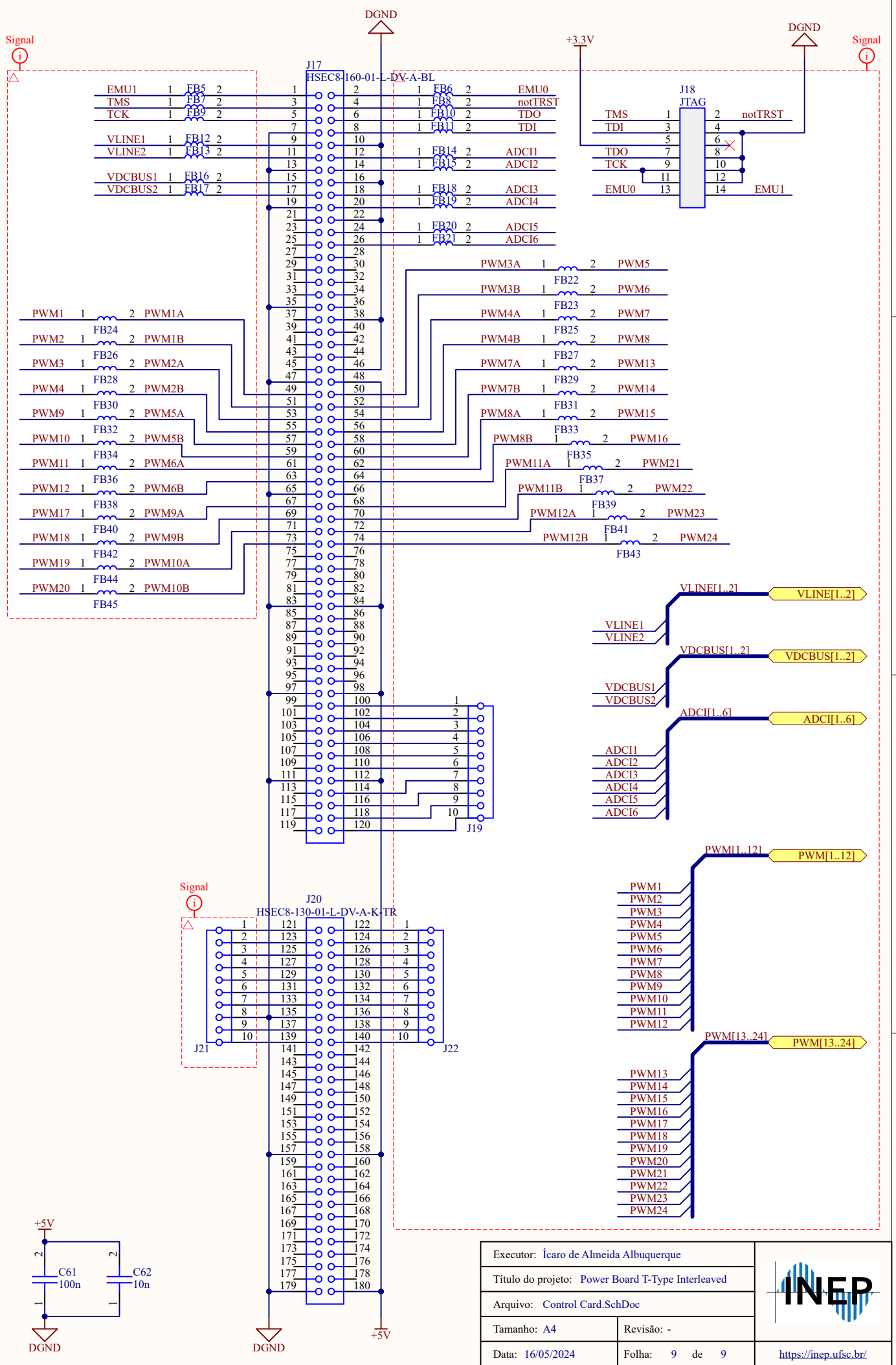


Executor: Ícaro de Almeida Albuquerque		INEP
Título do projeto: Power Board T-Type Interleaved		
Arquivo: 3ph_Module.SchDoc		
Tamanho: A4	Revisão: -	
Data: 16/05/2024	Folha: 7 de 9	https://inep.ufsc.br/



Executor: Ícaro de Almeida Albuquerque		
Título do projeto: Power Board T-Type Interleaved		
Arquivo: Phase branch.SchDoc		
Tamanho: A4	Revisão: -	
Data: 16/05/2024	Folha: 8 de 9	https://inep.ufsc.br/



Executor: Ícaro de Almeida Albuquerque	
Título do projeto: Power Board T-Type Interleaved	
Arquivo: Control Card.SchDoc	
Tamanho: A4	Revisão: -
Data: 16/05/2024	Folha: 9 de 9

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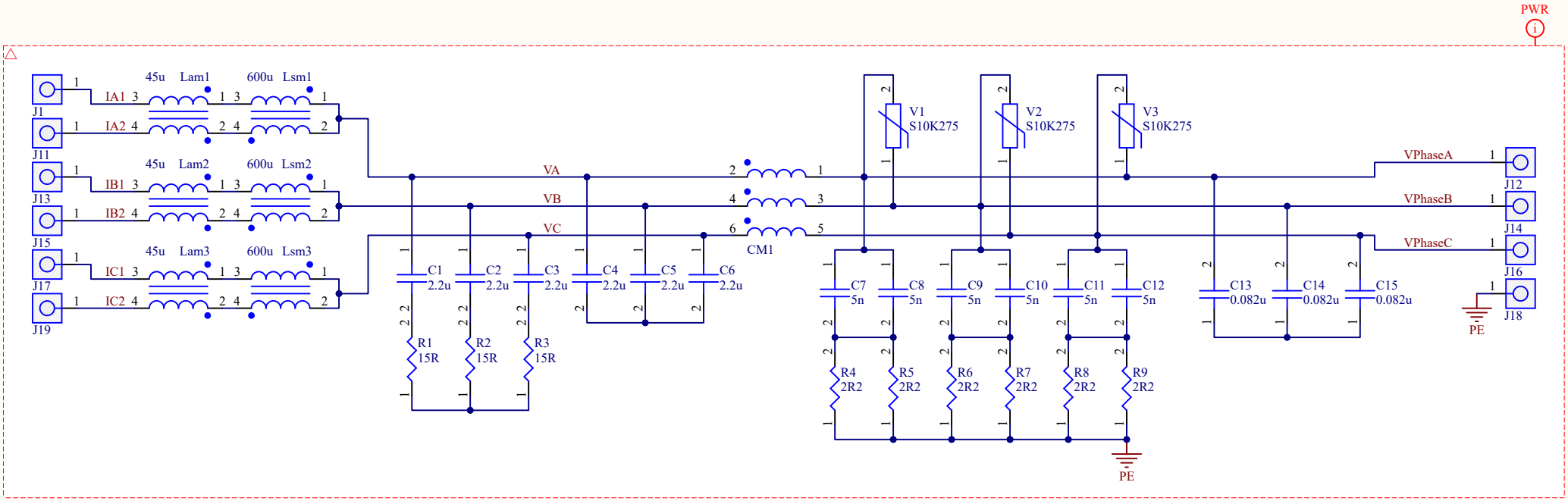
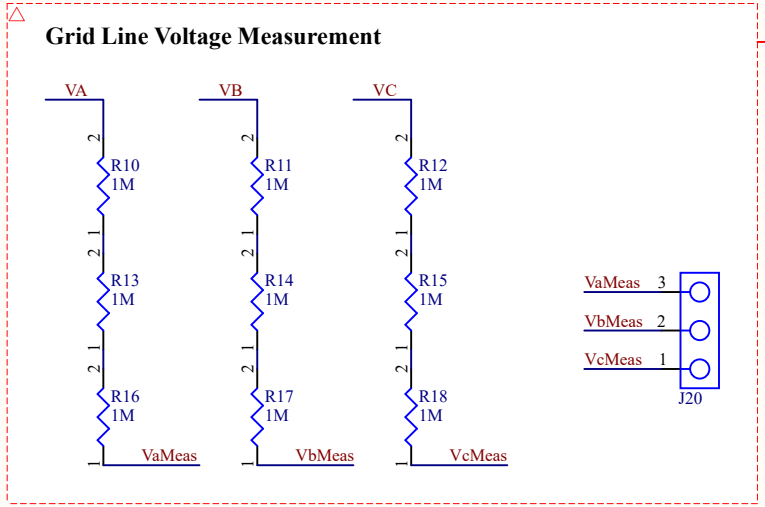
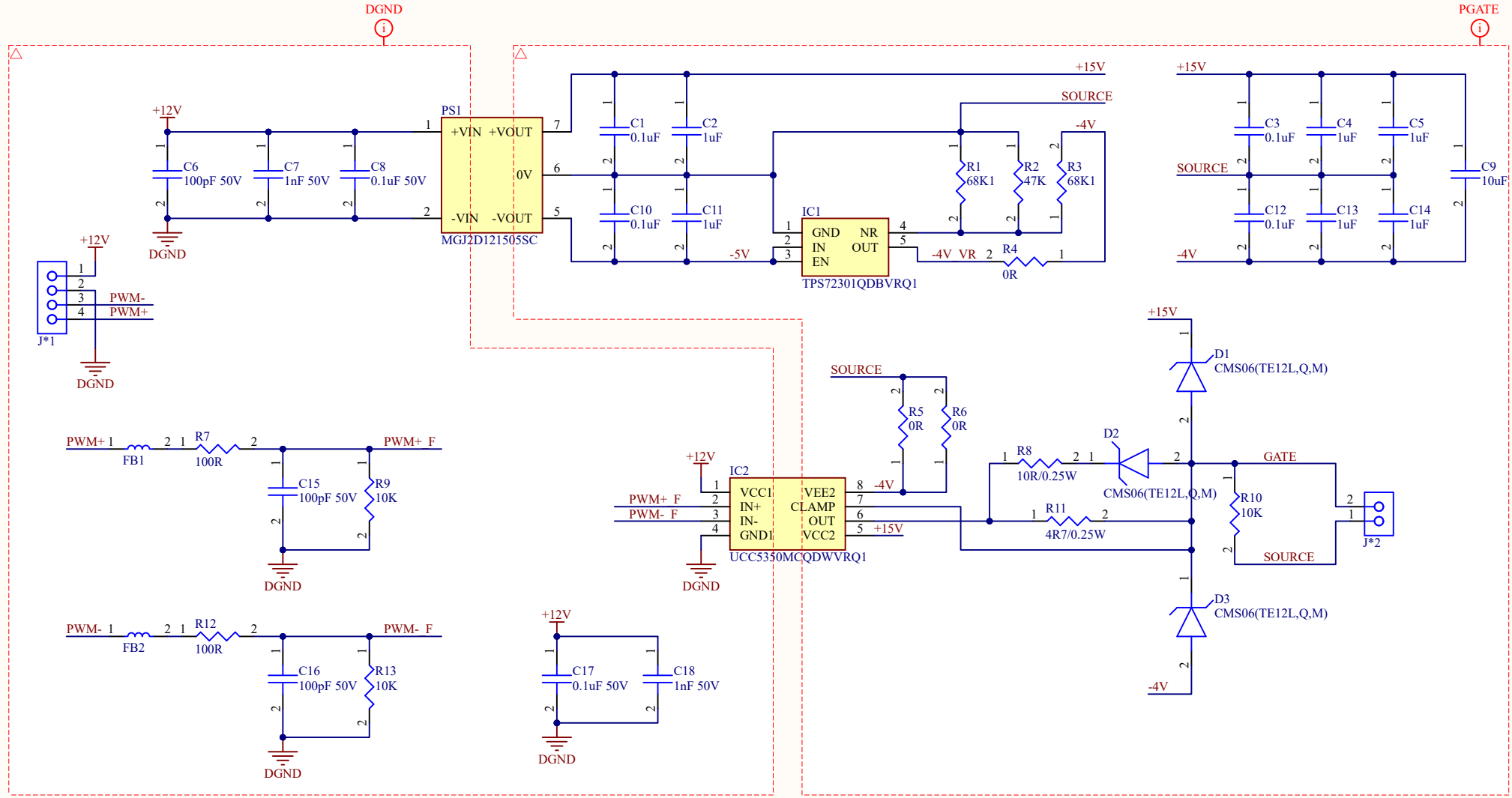
https://inep.ufsc.br/





Executor: Ícaro de Almeida Albuquerque		INEP
Título do projeto: Filter Board		
Arquivo: Filter.SchDoc		
Tamanho: A4	Revisão: -	
Data: 16/05/2024	Folha: 1 de 1	https://inep.ufsc.br/



The buffers output voltage in the main PCB is 5 V and thus the supply voltage of the gate driver's IC had to be adjusted to this voltage level using resistors.

Executor: Ícaro de Almeida Albuquerque	
Título do projeto: Gate Driver	
Arquivo: Gate_Driver_V1.SchDoc	
Tamanho: A4	Revisão: -
Data: 16/05/2024	Folha: 1 de 1

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