UNIVERSIDADE FEDERAL DE SANTA CATARINA
DEPARTAMENTO DE ENGENHARIA ELÉTRICA E ELETRÔNICA
CURSO DE GRADUAÇÃO EM ENGENHARIA ELETRÔNICA

Yan Romano

Design and Analysis of a 25GHz Mach-Zehnder Driver with a Programmable Continuous-Time Linear Equalizer for High-Speed Optical Communications Using CMOS 65nm Technology

Florianópolis
2024

Yan Romano

Design and Analysis of a 25GHz Mach-Zehnder Driver with a Programmable Continuous-Time Linear Equalizer for High-Speed Optical Communications Using CMOS 65nm Technology

Trabalho de Conclusão do Curso de Graduação em Engenharia Eletrônica do Centro Tecnológico da Universidade Federal de Santa Catarina como requisito para a obtenção do título de Bacharel em Engenharia Eletrônica
Orientador: Prof. Fernando Rangel de Sousa, Dr.
Coorientador: Eng. Rodrigo Eduardo Rottava, Msc.

Florianópolis
2024

Ficha catalográfica gerada por meio de sistema automatizado gerenciado pela BU/UFSC.
Dados inseridos pelo próprio autor.

Romano, Yan
Design and Analysis of a 25GHz Mach-Zehnder Driver with a Programmable Continuous-Time Linear Equalizer for High Speed Optical Communications Using CMOS 65nm Technology / Yan Romano ; orientador, Fernando Rangel de Sousa, coorientador, Rodrigo Eduardo Rottava, 2024.
79 p.

Trabalho de Conclusão de Curso (graduação) - Universidade Federal de Santa Catarina, Centro Tecnológico, Graduação em Engenharia Eletrônica, Florianópolis, 2024.

Inclui referências.

1. Engenharia Eletrônica. 2. Comunicação óptica de alta velocidade. 3. Mach-Zehnder. 4. Drivers. 5. CTLE. I. de Sousa, Fernando Rangel. II. Rottava, Rodrigo Eduardo. III. Universidade Federal de Santa Catarina. Graduação em Engenharia Eletrônica. IV. Título.

Design and Analysis of a 25GHz Mach-Zehnder with a Programmable Continuous-Time Linear Equalizer for High-Speed Optical Communications Using CMOS 65nm Technology

Este Trabalho Conclusão de Curso foi julgado adequado para obtenção do Título de Bacharel em Engenharia Eletrônica e aprovado em sua forma final pelo Curso de Engenharia Eletrônica.

Florianópolis, 16 de Dezembro de 2024.

Documento assinado digitalmente
Daniela Ota Hisayasu Suzuki
Data: 20/12/2024 12:25:03-0300
CPF: ***.397.389-**
Verifique as assinaturas em https://v.ufsc.br

Prof. Daniela Ota Hisayasu Suzuki, Dra.
Coordenador(a) do Curso

Documento assinado digitalmente
Fernando Rangel de Sousa
Data: 20/12/2024 14:12:44-0300
CPF: ***.649.114-**
Verifique as assinaturas em https://v.ufsc.br

Prof. Fernando Rangel de Sousa, Dr.
Orientador (EEL - UFSC)

Banca Examinadora:

Documento assinado digitalmente
RODRIGO EDUARDO ROTTAVA
Data: 20/12/2024 13:12:50-0300
CPF: ***.787.159-**
Verifique as assinaturas em https://v.ufsc.br

Eng. Rodrigo Eduardo Rottava, Msc.
Coorientador (Chipus Microeletrônica S.A.)

Documento assinado digitalmente
Fabian Leonardo Cabrera Riano
Data: 20/12/2024 13:26:07-0300
CPF: ***.071.638-**
Verifique as assinaturas em https://v.ufsc.br

Prof. Fabian Leonardo Cabrera Riano, Dr.
Avaliador (EEL - UFSC)

Documento assinado digitalmente
VICTOR HUGO BUENO PREUSS
Data: 20/12/2024 12:25:31-0300
CPF: ***.215.639-**
Verifique as assinaturas em https://v.ufsc.br

Eng. Victor Hugo Bueno Preuss, Msc.
Avaliador (Chipus Microeletrônica S.A.)

ACKNOWLEDGEMENTS

I express my profound gratitude to my parents, Carmen Lúcia Silva da Luz Fontes and Paulo Antônio Romano, who did everything possible to provide me with a quality education and gave me life lessons that have been fundamental throughout my journey in life.

I am also grateful for my stepfather and fellow engineer Fernando Orofino da Luz Fontes for his guidances and advices throught my journey at UFSC.

To my relatives, Rosemari Dilma da Silva and Alcino Tives Schlichting Filho, thank you for all the support you have provided me with regard to studies since I was little.

I extend my sincere thanks to Chipus Microelectronics for offering me an immersive internship experience, full of invaluable insights and learning opportunities in the field of microelectronics. Without their support, this work would not have been possible.

I am deeply appreciative of the co-advisor of this work, Rodrigo Rottava, whose crucial involvement throughout the development of this project provided essential guidance, innovative ideas, and solutions to numerous challenges.

To the advisor of this work, Fernando Rangel, I am grateful for his mentorship and commitment to fostering critical and analytical thinking, which has been a great influence in the production of this project.

Lastly, to all my close friends, who supported me through the difficult moments in this course, thank you. Your encouragement and companionship made all the difference.

ABSTRACT

This work aims to design and analyze a laser driver used for high-speed optical signal transmission. Throughout this study, the selected topologies, design choices, trade-offs, bandwidth extension techniques, and obtained results will be examined. The project is integrated using 65nm CMOS technology, targeting PAM4 modulation signals of 28 Gbaud/s. The driver output incorporates a CML driver with a swing of 2.2 Vpp,d and features a programmable continuous-time equalizer that can quantitatively adapt to different channel losses, providing up to 6dB of pre-equalization. Performance measurements indicate a gain of 8dB with a bandwidth of 25 GHz. In tests with PAM4 input signals, the output eye diagram showed an eye opening of 288 mV and an eye width of 14.43 ps at 2.2 Vpp,d output. The driver exhibits low distortion, characterized by a THD of 5% at 2.2 Vpp,d. The circuit operates with a 3V power supply, a 1mA current source, and has a power consumption of 506 mW.

Keywords: Mach-Zehnder, Laser driver, Optical communication, High-speed, Transmitters, CMOS 65nm.

RESUMO

Este trabalho tem por objetivo o design e análise de um laser driver utilizado para transmissão de sinais ópticos de alta velocidade. No decorrer deste trabalho, serão analisadas as topologias selecionadas, as decisões de desenvolvimento adotadas, trade-offs enfrentados, técnicas aplicadas para extensão de banda e os resultados obtidos. O projeto é integrado com a tecnologia CMOS 65nm, visando a transmissão de sinais de modulação PAM4 a 28 Gbaud/s. Em sua saída o circuito incorpora um driver em lógico de modo corrente com excursão de 2.2 Vpp,d , além de constar com um equalizador de tempo contínuo programável, capaz de se adequar quantitativamente a diferentes perdas de canal, fornecendo uma pré-equalização de até 6dB. As medições de desempenho indicam um ganho de 8dB, com uma banda de 25 GHz. Em testes com sinais de entrada PAM4, o diagrama de olho do sinal de saída apresentou uma abertura de olho de 288 mV e uma largura de olho de 14.43 ps em 2.2 Vpp,d na saída. O driver possui baixa distorção, caracterizada por um THD de 5% a 2.2 Vpp,d. O circuito opera com uma fonte de tensão de 3V, fonte de corrente de 1mA e possui um consumo de potência de 506 mW.

Palavras-chave: Mach-Zehnder, Laser driver, Comunicação óptica, Alta velocidade, Transmissores, CMOS 65nm.

List of Figures

List of Tables

Contents

1 Introduction

1.1 Motivation

In recent years, global data traffic has surged, with projections indicating sustained and significant growth. This trend necessitates advancements in telecommunications networks to efficiently manage increasing data volumes. As traditional electrical I/O throughput approaches bandwidth limitations due to severe high-frequency losses, optical communication emerges as a promising solution, offering energy-efficient, high-bandwidth, and cost-effective transmission. Silicon-based high-speed integrated circuits, particularly for wired communications, have become essential for their cost advantages and seamless integration potential, enabling high data rates within network backbones. The potential for all-silicon fabrication is especially appealing due to its compatibility with standard CMOS technology, facilitating integration with large-scale digital signal processing systems. In this context, optical communication has gained renewed interest, driven by the widespread need for high-speed optical and electronic components, circuits, and systems [1].

Optical systems, however, present unique challenges: achieving transmission speeds in the tens of gigabits per second necessitates specialized circuit techniques to manage the wide spectrum and random nature of data signals. Additionally, the extensive high-speed digital circuitry required for optical transceivers can complicate full integration efforts.

In this context, a robust and efficient optical transmission system is crucial as a foundational component in transmission circuits. This project seeks to address some of these challenges by designing a Mach-Zehnder modulator driver integrated into 65nm CMOS technology. The design includes a programmable pre-emphasis circuit to adapt to varying channel loss specifications and incorporates a high-swing amplification circuit suitable for high-frequency applications [1].

1.2 Related works and state of the art review

The article [2] introduces a low-power linear driver for coherent optical transmitters, utilizing a stacked current-mode architecture to reduce power consumption with a single supply voltage. This topology allows shared current across components like the variable gain amplifier (VGA) and equalizer (VEQ), optimizing energy without sacrificing signal integrity. By stabilizing the intermediate supply node (VM) with constant current sources, the design reduces noise and maintains stable differential output. The driver achieves 2.25 mW/Gb/s efficiency at 80 Gb/s (PAM4) with a 2.9 Vpp swing at 50 Gb/s (NRZ), offering a efficient solution for high-speed optical communication.

Paper [3] presents a high-speed, configurable distributed feedback (DFB) laser diode driver (LDD) in 65nm CMOS, supporting 32Gb/s NRZ and 15GBaud/s

PAM4 modulation. Using a balanced-input, single-ended-output topology with active back-termination (ABT), it minimizes reflections and improves signal integrity in the presence of PCB-laser impedance mismatches. A tunable pre-emphasis circuit and inductive shunt-peaking further boost bandwidth, achieving a 25.78Gb/s data rate. The driver consumes 550mW making it an efficient option for long-reach fiber applications.

The article [4] describes a 65nm CMOS linear driver IC with a 48GHz bandwidth and 225mW per-channel power consumption, designed for high data rates beyond 400Gb/s in coherent optical transmitters. Using a stacked current-reuse architecture, the driver reduces power demands. Bandwidth is extended from 7GHz to 48GHz through shunt and series multi-peaking with compact 3D inductors, while integrated amplifiers and equalizers offer gain and emphasis control along with temperature stability. The design minimizes total harmonic distortion (THD) and crosstalk, achieving 64GBaud DP-32QAM modulation at 640Gb/s and a power efficiency of 1.4mW/Gb/s, a leading performance metric for coherent systems.

In the article [5], a power-efficient 32 Gb/s driver for Mach-Zehnder (MZM) and electro-absorption (EAM) modulators, using a push-pull CML architecture with a double cascode structure to handle over-voltage stress and achieve a 4 Vpp differential swing is introduced. Compactly integrated shunt-peaking inductors enhance bandwidth and maintain a stable group delay. Fabricated in 65 nm CMOS, the driver reaches extinction ratios of 4.53 dB (MZM) and 4.17 dB (EAM) with 201 mW power consumption, achieving 6.28 mW/Gb/s efficiency, suitable for high-speed, silicon photonic applications due to its compact 0.086 mm^2 footprint.

A table summarizing key parameters from the selected articles is provided in Table 21. While variations in topology, modulation formats, and some missing parameters may limit direct comparisons, the table still allows for meaningful performance assessment, offering valuable insight into how this project measures up to the state of the art.

1.3 Dissertation organization

This dissertation is structured as follows: Chapter 2 covers essential topics for understanding the design, operation, and implementation of the devices, circuits, and techniques used in this project. Key areas include optical communication systems, Mach-Zehnder Modulators (MZM), Current-Mode Logic (CML) drivers, Programmable Continuous-Time Linear Equalization (CTLE), and various bandwidth extension techniques.

In Chapter 3, building on the theoretical foundations established in the previous chapter, the project design is detailed. This includes a focus on key equations, selected topologies, and design methodologies that underpin the approach, culminating in a presentation and analysis of the simulation results.

Table 1: Selected work on high-speed transmitters

Reference	**Circuit Topology**	**Modulation Format**	**Bandwidth (GHz)**	**Output Swing ($V_{pp,d}$)**	**THD (%)**	**Gain (dB)**	**Data Rate (Gbaud)**	**Data Rate (Gb/s)**	**DC Power (mW)**	**Energy Efficiency (pJ/b)**	**Technology**	**Measurement Scope**
[2]	Stacked current-mode, VGA, VEQ	PAM4	32	2	6 (for 2 $V_{pp,d}$)	24	40	80	180	2.25	65nm CMOS	Fabricated
[4]	Stacked current, MZM, GC, EMP, peaking	DP-32QAM	43	1.5	2.2 (for 1.5 $V_{pp,d}$)	13-22.5	64	640	225	1.41	65nm CMOS	Fabricated
[5]	Push-pull CML, MZM, EAM, shunt-peaking	PAM4	17	4	3	3	16	32	201	6.28	65nm CMOS	Fabricated
[3]	Balanced input, single-ended output, tunable pre-emphasis, back-termination	NRZ/PAM4	18	-	-	-	16	32	550	17.18	65nm CMOS	Fabricated

2 Theoretical background

This chapter will focus on the essential theoretical foundation for understanding the high-speed optical communication system that is designed and simulated in this work. It begins with an overview of optical transmission systems and signal modulation choices. The main topologies and devices that compose the project are discussed, such as Mach-Zehnder modulators, along with the current-mode logic (CML) driver and continuous time linear equalization.

Lastly, CMOS-compatible bandwidth extension techniques, including shunt and series peaking, source degeneration, cascode amplification, and interstage buffers, are presented to address high-frequency operation.

This background prepares the reader for design choices and performance expectations in optical communication systems.

2.1 Optical transmission systems

Depicted in Fig. 1, a basic optical communication system relies on three core components: an electro-optical transducer (such as a laser diode), which converts electrical signals into optical signals; an optic channel (such as a fiber optic cable), which transports the laser-generated light; and a photodetector (like a photodiode), positioned at the channel's receiving end, where it detects the incoming light and reconverts it into an electrical signal.

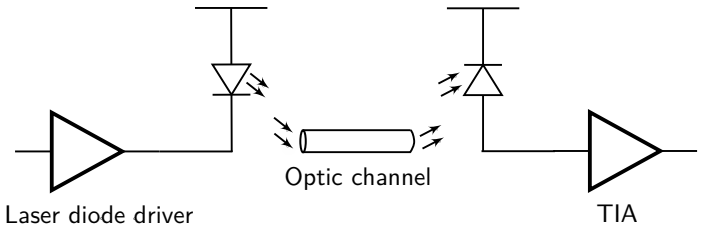

Figure 1: A basic optical communication system.

Source: Author

As light travels through the channel, it can experiences considerable attenuation. Thus, the laser on the transmitter end must produce a high light intensity to compensate for this loss. On the receiver side the photodiode must exhibit a high sensitivity to light, and the electrical signal generated by the received light on the photodiode typically requires low-noise amplification, often achieved with a transimpedance amplifier (TIA), which is also used because the photodiode output is a current signal. [1].

Direct drive systems, like the one exemplified above, modulate the light by directly driving the laser diode with an electrical signal. This method simplifies the overall design allowing for a more straightforward, compact setup. How-

ever, directly modulating a laser diode presents limitations in achieving higher data rates due to the diode's limited bandwidth and non-linear response at high speeds. Additionally, directly driven laser diodes can suffer from reduced signal quality, such as increased chirp and degraded extinction ratio, which can impact long-distance signal transmission.

Another way of electro-optical (E/O) conversion is the use of silicon photonic modulators which are employed to encode the desired information onto a continuous-wave (CW) light source generated by an external laser. These modulators include Electro-Absorption Modulators (EAM), Ring Resonator Modulators (RRM), and Mach-Zehnder Modulators (MZM), each with distinct operational characteristics and benefits.

Mach-Zehnder Modulators, which are the selected type of E/O for this project, modulate light by introducing interference between two optical paths, controlled by an applied voltage that changes the phase of light in each arm. MZMs are highly valued for their wide optical bandwidth and thermal stability, making them well-suited for high-speed, long-distance communications. Due to their larger size and higher driving voltage requirements compared to EAMs and RRMs, MZMs require robust driver circuits capable of delivering sufficient voltage swings for effective modulation.

This work focuses on the transmitter side of an optical communication system. The primary objective is to adequately drive the MZM, ensuring that the emitted light intensity is strong enough to offset the attenuation that occurs as it travels through the channel. Figure 2 represents a driver with a MZM load.

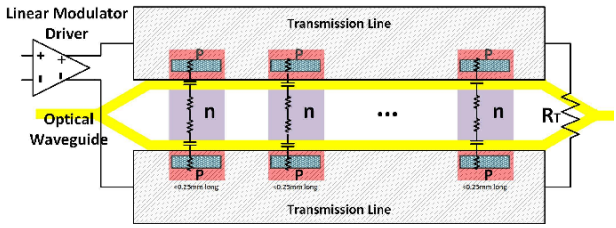

Figure 2: MZM driver illustration.

Source: Zandieh, 2017 [6].

In optical communication, the choice of modulation format (the method used to encode and decode data) is also important to system design. This format can vary, with options including NRZ, DP-QPSK, DP-QAM, QAM, and PAM4, each offering distinct advantages for different performance and transmission requirements.

For this project, PAM4 modulation is selected (Fig. 3) instead of other modulation types like NRZ. The contrast of PAM4 to NRZ is that it employs four distinct signal levels to represent data. Each symbol in PAM4 carries two bits, corresponding to the logical states 00, 01, 10, or 11. This dual-bit-per-symbol structure effectively augments the data rate in gigabits per second, enabling high

data throughput even at lower frequencies. Consequently, PAM4 facilitates high-speed data transmission while operating at reduced high frequencies compared to NRZ.

PAM4 modulation tends to require relatively high power consumption due to the equalization and pre-compensation needed at both the transmitter and receiver ends to reduce bit error rate (BER). Additionally, the closely spaced signal levels in PAM4 make it more vulnerable to noise , distortion, and dispersion than other modulations, all of which contribute to intersymbol interference and degrade signal quality.

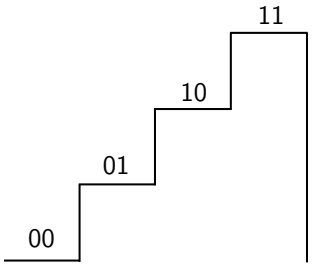

Figure 3: PAM4 signal illustration.

Source: Author.

Having this in mind, the project must not only counteract the channel loss within a high frequency range delivering a high-swing to the MZM, it need to account for distortion due to the use of a PAM4 modulation and it's sensitivity.

2.2 Mach-zehnder modulators

A Mach-Zehnder Modulator (MZM) operates by utilizing the electro-optic effect to modulate light signals. The modulator splits incoming light into two paths, or arms, and later recombines them. An applied electric field on one arm changes the carrier density, inducing a phase shift in the light traveling through that arm. This phase shift leads to constructive or destructive interference when the light from both arms is combined, modulating the light's output intensity.

If the phase shift between the two waves is 0°, maximum constructive interference occurs, resulting in the highest output intensity. Conversely, if the phase shift between the two waves is 180°, maximum destructive interference is achieved, leading to the lowest output intensity. Assuming no loss and a perfect 50/50 splitter/combiner, the relationship between the output power (P_{out}) and the input power (P_{in}) is given by:

$$\frac{P_{\text{out}}}{P_{\text{in}}} = \frac{1 + \cos(\Delta\phi)}{2} \tag{1}$$

where $\Delta\phi$ represents the phase difference between the two arms.

The structure and principle of operation of a Mach-Zehnder can be seen in Figure 5. Due to the size of the Mach-Zehnder Interferometer (MZI), the electrical signal is distributed to individual optical modulating elements using coplanar

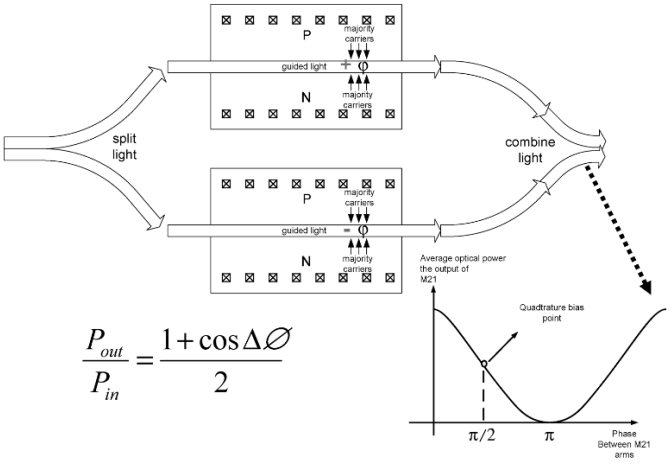

Figure 4: MZM structure and principle of operation.

Source: Analui, 2006 [7]

transmission lines of equal impedance. Each optical modulating element comprises a reverse-biased p-n junction integrated with a waveguide, which presents a lumped capacitive load. To maintain impedance continuity and avoid reflections that could disrupt the signal, numerous small modulating elements are uniformly distributed along the transmission lines. The transmission lines' dimensions are optimized to achieve a desired characteristic impedance, also matching the distributed junction capacitance [7].

Ensuring the propagation velocity of the electrical signal aligns with the speed of light in the waveguide is crucial for maintaining signal integrity. To prevent inter-symbol interference (ISI) in the optical output caused by signal reflections, dual termination can be employed. The modulator receives a continuous-wave (CW) light beam from a laser, which is coupled into the on-chip waveguide, enabling effective optical modulation.

This work will consider a travelling wave MZM with double 50 Ohms termination, tranmission lines with $Z_0 = 50\Omega$ characteristics and shared VDD bias with the driver as the load.

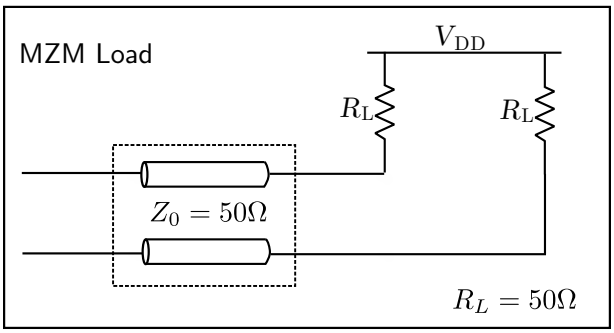

Figure 5: Equivalent circuit of the MZM load of this project.

Source: Author.

2.3 Current-mode logic driver

What makes current mode logic driver a good candidate for a Mach-Zender modulator is that they provide high-speed operation, wideband impedance matching, and ability to deliver large voltage swings.

Current mode drivers work by switching a constant current source of several mA to produce an output differential voltage over a termination resistance. The termination resistance can have several configurations, such as single-ended, differential, parallel and series. Because of the expected configuration of the MZM load, we will focus on a parallel single-ended double termination for the CML driver topology, represented at the circuit on Figure 6.

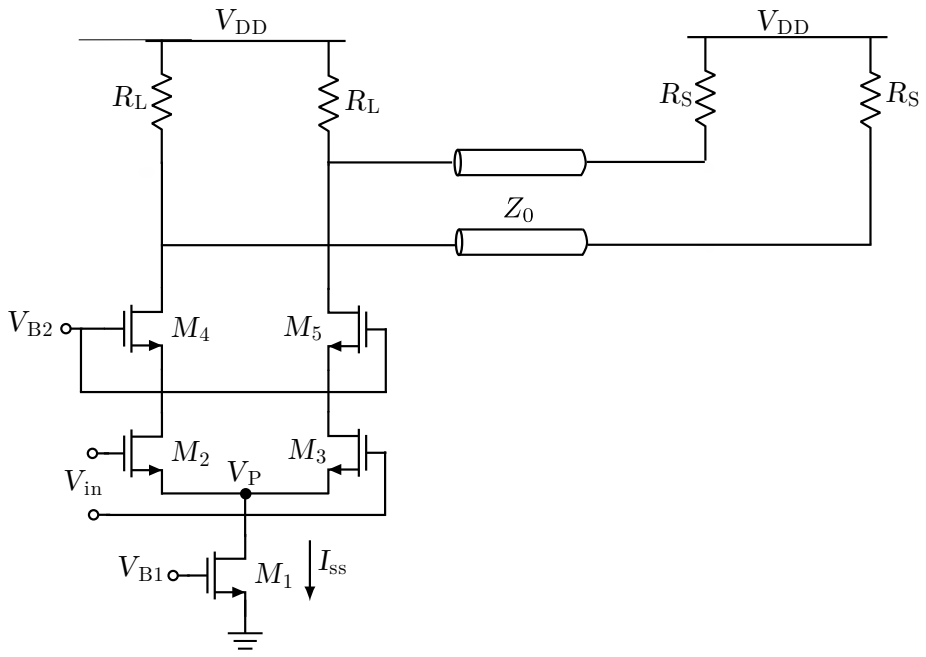

Figure 6: CML circuit with double parallel termination

Source: Author.

The topology of the circuit consists of a differential pair, where a cascode structure is added in order to alleviate the over-voltage stress while achieving a sufficiently large voltage swing. It also serves to enhance the circuit bandwidth because of Miller Effect reduction, which will be discussed in section 2.6.

2.3.1 Output swing

One key parameter of this topology is the voltage swing provided by the current-mode logic driver. The voltage swing can be calculated to understand the maximum variation in output voltage that the driver can achieve during operation.

The minimum voltage at the output is the needed voltage to maintain all transistors in saturation, which is sum of the overdrive voltages of the stacked transistors:

$$V_{\text{out,min}} = V_{\text{ov(M1)}} + V_{\text{ov(M2,3)}} + V_{\text{ov(M4,5)}} \tag{2}$$

Considering the common biasing voltage of the cascode transistor, V_{B2}, provides enough voltage to maintain M2 and M3 saturated, the minimum output voltage equation can be rewritten in regards of this biasing condition:

$$V_{\text{out,min}} = (V_{\text{B2}} - V_{\text{GS(M4,5)}}) + V_{\text{ov(M4,5)}} \tag{3}$$

The single-ended common mode voltage at the outputs is going to be the output voltage at equilibrium, which is detoned as:

$$V_{\text{out,scm}} = V_{\text{DD}} - \frac{I_{\text{SS}}}{2} R_L || R_S \tag{4}$$

To calculate the voltage swing we can look at the extreme current steering conditions of the CML. In the given circuit, the maximum current in one branch occurs when the total bias current I_{SS} flows entirely through one side , while the other side has no current flowing through it, remaining at V_{DD}. This condition results in the maximum voltage swing. The voltage drop across R_L when I_{SS} flows through it is $V_{RL} = I_{SS} \cdot R_L$. However, when considering the transmission line termination with an impedance R_S, the effective load seen by I_{SS} becomes the combination of R_L and R_S. Thus, the single-ended output voltage swing is influenced by this configuration, leading to the equation

$$V_{\text{pp,s}} = I_{SS} \cdot \frac{R_L R_S}{R_L + R_S} \tag{5}$$

This relationship shows that the maximum swing is determined not only by I_{SS} and R_L but also by the impedance matching with R_S, which impacts the voltage distribution at the output.

Considering a matched termination, the single-ended voltage swings becomes $V_{\text{pp,s}} = I_{SS} \cdot \frac{R_L}{2}$, making the differential output swing:

$$V_{\text{pp,d}} = 2 \cdot I_{SS} \cdot \frac{R_L}{2} = I_{SS} \cdot R_L \tag{6}$$

So, for a desired $V_{\text{pp,d}}$, we must assure there is enough voltage headroom at the output to drive the modulator without changing the saturation condition of any of the transistors, this condition is the equivalent to:

$$V_{\text{DD}} = \frac{V_{pp,d}}{2} + (V_{\text{B2}} - V_{\text{GS(M4,5)}}) + V_{\text{ov(M4,5)}} \tag{7}$$

2.3.2 Power consumption

The analysis of the current-defined swing in the previous section highlights a trade-off with power consumption in CML topologies, particularly when driving high-swing loads. This can result in power inefficiency due to the requirement

for a high supply voltage (V_{DD}) to maintain the necessary voltage headroom for the output swing.

The power consumption of a CML driver is given by $\mathrm{Power}_{\mathrm{CML}} = V_{\mathrm{DD}} \cdot I_{\mathrm{SS}}$, by combining this with equations 3, 6 and 7, the power consumption can be expressed in terms of the differential output swing::

$$\mathrm{Power}_{\mathrm{CML}} = (\frac{V_{pp,d}}{2} + V_{\mathrm{out,min}}) \cdot \frac{V_{pp,d}}{R_L} \tag{8}$$

This equation illustrates a quadratic relationship between the differential output swing and power consumption, emphasizing that increasing the output swing results in a significant rise in power usage [8]. This trade-off is visually represented in Figure 7.

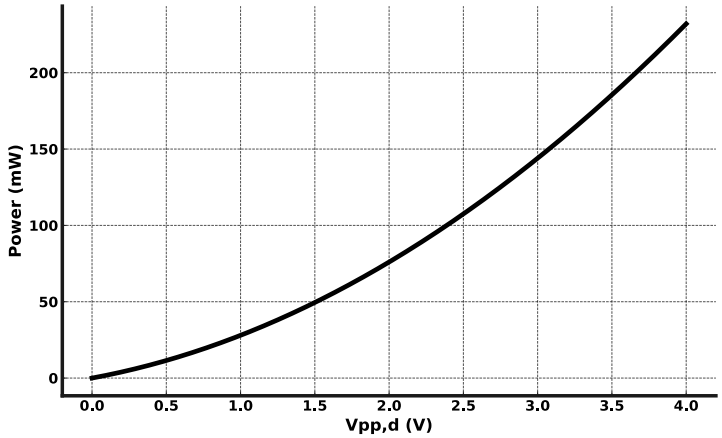

Figure 7: CML driver trade-off between power consumption and differential output swing ($R_L = 50\Omega$, $V_{\mathrm{out,min}} = 0.9$).

Source: Author.

2.3.3 Current source biasing trade-offs

When designing the current source for biasing the CML differential pair, several considerations must be taken into account.

Firstly, the choice of using a single-transistor (M1) current source provides minimal headroom consumption of $V_{\mathrm{DS,M1}}$, which is advantageous for maintaining the required high output swing. In contrast, more accurate current source topologies often employ stacked transistors, which offer improved current mirroring accuracy and PSRR/CMRR but at the expense of increased voltage headroom requirements. This trade-off impacts the overall accuracy of the output swing, with single-transistor current sources prioritizing swing at the cost of precision.

Additionally, as illustrated in Fig. 8, there are challenges related to switching transients and voltage excursions at node P. There is a parasitic capacitance on C_P at this node, and variations in V_P can arise from process variations and mismatch. This can create a parasitic current defined by $i_{C_P} = \frac{dV_P}{dt}$ within C_P,

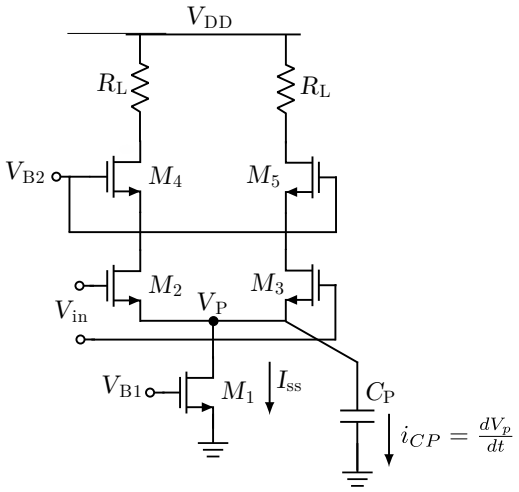

Figure 8: Parasitic capacitance at CML current-source node

Source: Author.

which, when subject to significant voltage excursions, can lead to inter-symbol interference (ISI) in the output signal.

To mitigate these issues, the current source should be designed to minimize parasitic capacitances.

2.4 Continuous-time linear equalizer

At very high data rates, issues such as parasitic capacitances within circuits, channel losses, and other inherent challenges can lead to intersymbol interference (ISI) and significant signal attenuation at high frequencies. These factors degrade performance and increase the bit error rate (BER) in communication systems, presenting significant challenges for high-speed interfaces. To mitigate these issues, equalization techniques are often employed in high-speed circuit design.

Various methods have been developed to counteract signal degradation along transmission paths. To further extend transmission capabilities at multi-Gb/s speeds, pre-drivers are typically used to equalize and reshape distorted signals, ensuring that receiving devices meet BER specifications without failure.

Signal loss levels vary depending on the specific channel, such as the Mach-Zehnder modulator channel, and other application-specific factors. Fixed-gain Continuous-Time Linear Equalizers (CTLEs) are suitable for certain platforms and specific loss levels, but programmable CTLEs offer greater versatility. These equalizers can be adjusted to compensate for losses in different environments.

Most transmission channels exhibit low-pass filter characteristics, where low-frequency signals experience minimal attenuation, while higher-frequency components face significant attenuation. This behavior poses a major challenge in high-speed applications, where the transmission of high-frequency signals is essential. The primary function of an equalizer is to implement a transfer function that effectively inverses the channel's transfer function $1/H_{\mathrm{ch}}(s)$. By doing so,

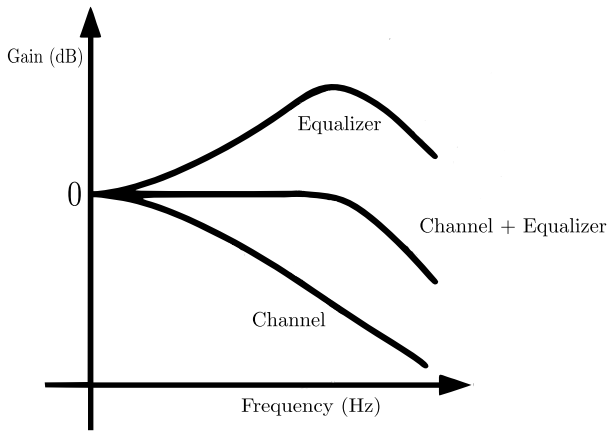

Figure 9: Channel equalization illustration

Source: Author.

the equalizer enhances the high-frequency components and creates a combined flat response up to a specified frequency. This concept is illustrated in Figure 9.

In a CTLE, AC gain is defined as absolute high frequency peak gain with respect to 0dB and DC gain is defined as low frequency gain with respect to 0dB. Peaking gain is defined as difference between AC gain and DC gain.

2.4.1 Conventional CTLE

In a traditional CTLE, peaking gain is achieved by lowering the DC gain and introducing a zero at a frequency of interest that counteracts the circuit portion responsible for this lowering. This means that more gain may be needed elsewhere after that to compensate for the added DC loss.

A conventional Continuous-Time Linear Equalizer (CTLE) with first-order capacitive source degeneration, depicted in Figure 10, provides one zero and two poles in its frequency response. The source degeneration introduces peaking by creating a low-frequency zero through the parallel capacitance, enhancing both the linearity, because of the source resistance, and bandwidth of the differential pair. The DC gain, zero, poles, and the transfer function of this CTLE can be expressed as follows:

$$\omega_z = \frac{1}{R_S C_S} \tag{9}$$

$$\omega_{p1} = \frac{1}{R_L C_L} \tag{10}$$

$$\omega_{p2} = \frac{1 + g_m R_S/2}{R_S C_S} \tag{11}$$

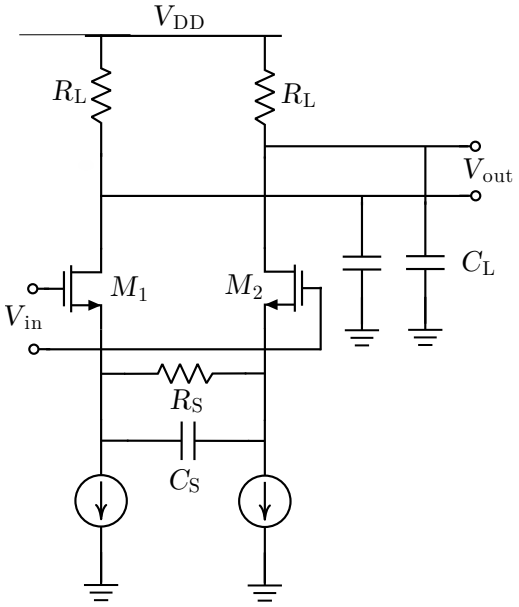

Figure 10: Conventional linear equalizer with source degeneration peaking

Source: Author.

$$A_{DC} = \frac{g_m R_L}{1 + g_m R_S/2} \tag{12}$$

$$H(s) = A_{DC} \frac{1 + s/\omega_z}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{13}$$

When the condition $w_{z1} < (w_{p1}, w_{p2})$ is met, peaking occurs, resulting in a frequency response that facilitates signal equalization. The peaking frequency is determined by the lower value between w_{p1} and w_{p2}. A Bode plot, depicted in Figure 11, can be used to approximate and provide insight into the circuit's frequency response behavior, offering a clear visualization of its performance characteristics.

The source degeneration resistance R_S directly impacts the DC gain and sets the zero frequency, ω_z, which also shifts with changes in R_S, leading to variations in peaking behavior. Moreover, R_S influences the high-frequency pole w_{p2}, which also impacts the peaking behavior of the circuit, depending if w_{p2} is lower or higher than w_{p1}.

Capacitive source degeneration, defined by C_S, influences the location of the zero frequency and the peak gain frequency.

The load resistance R_L influences in the DC gain and peaking gain, as shown by the equations 10, 12. An increase in R_L can be beneficial for signal amplification but impacts the peaking frequency w_{p1}, limiting high-speed performance, it also influences circuit biasing. This trade-off requires careful consideration to maintain the desired gain without negatively affecting the bandwidth.

The load capacitance C_L is typically not a design variable, as it is determined by the circuit layout and the components connected to it. Nevertheless,

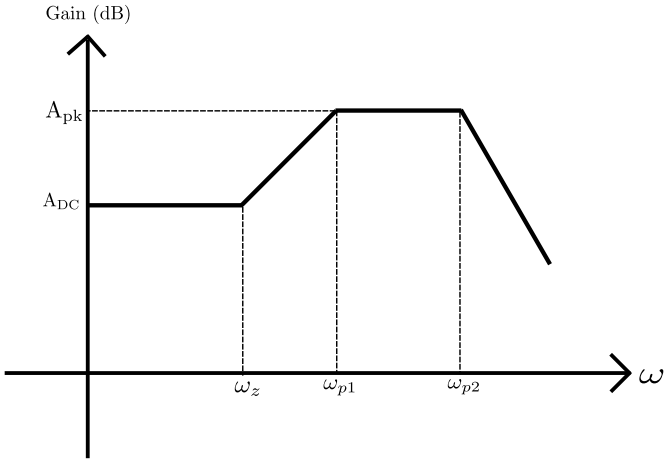

Figure 11: Bode magnitude plot of conventional source-degenerated CTLE frequency response.

Source: Author.

it plays an essential role in defining the pole frequency w_{p1}, usually limiting the high-frequency response of the CTLE. This constraint highlights the importance of optimizing other design parameters, to achieve the desired circuit behavior without relying on changes to C_L.

Designing this CTLE circuit involves balancing various trade-offs. A table containing trade-off cenarious is presented at Table 2 .

Table 2: Source-degenerated CTLE design trade-offs

$\omega_{p1} < \omega_{p2}$			
Increasing	A_{DC}	A_{pk}	**Peak Freq.** ω_{p1}
R_L	Increases	Increases	Decreases
R_S	Reduces	No Change	No Change
C_S	No Change	Increases	No Change
$\omega_{p2} < \omega_{p1}$			
Increasing	A_{DC}	A_{pk}	**Peak Freq.** ω_{p2}
R_L	Increases	Increases	No Change
R_S	Reduces	Reduces	Reduces
C_S	No Change	Increases	Reduces

Several design constraints need to be considered when working with this CTLE circuit. The load capacitance C_L is not a design parameter, making it necessary to work within its limitations, as it limits the boost factor ($A_{\text{pk}} - A_{\text{DC}}$). The selection of R_L is influenced by factors such as the common-mode output voltage ($V_{\text{cm,out}}$), bias current, and targeted DC gain. Adjusting R_S and C_S allows tuning of the CTLE response to balance peaking, gain, and bandwidth.

2.4.2 Programmable CTLE

Figure 13 illustrates the architecture of the implemented Programmable Continuous-Time Linear Equalizer, which is designed with two parallel signal paths. The

upper path is responsible for delivering low-frequency gain, commonly referred to as the 'flat band', and it exhibits a low-pass characteristic. In contrast, the lower path contributes the peaking gain essential for the CTLE's high-frequency response, having the same characteristics of the upper path with the addition of the peaking response. Both signals meet each other at a common node where they are summed into the output.

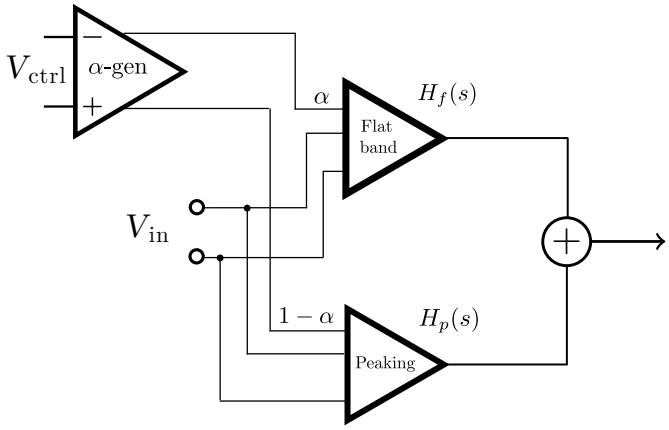

Figure 12: Diagram of the programmable CTLE top architecture.

Source: Author.

To manage how much peaking is utilized a circuit, nominated the α-gen circuit, controls how much of each signal passes through it's path's output. Algebricaly, the output response of the block will be:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \alpha H_f(s) + (1-\alpha)H_p(s) \tag{14}$$

where $H_f(s)$ represents the flat gain path and $H_p(s)$ denotes the peaking gain path. By adjusting the weighting factors α and $(1-\alpha)$, which control the distribution of the signal between the two parallel paths, the CTLE's peaking gain can be programmed to vary from a flat band response to the maximum peaking gain [9].

The choosen topology to create this programabble equalization is shown in Figure 13. The circuit is composed of two Gilbert cells. Consider the following composition of transistors for each Gilbert-cell stage:

- **Transconductance stages:** Transistors M1 to M4
- **Switching stages:** Transistors M5 to M12
- **Load stages:** Resistances R_L connected to the output

In the Gilbert cell responsible for the flat-band response, the transconductance stage is implemented using a simple differential pair with source degeneration. The cell representing the peaking response incorporates source degeneration

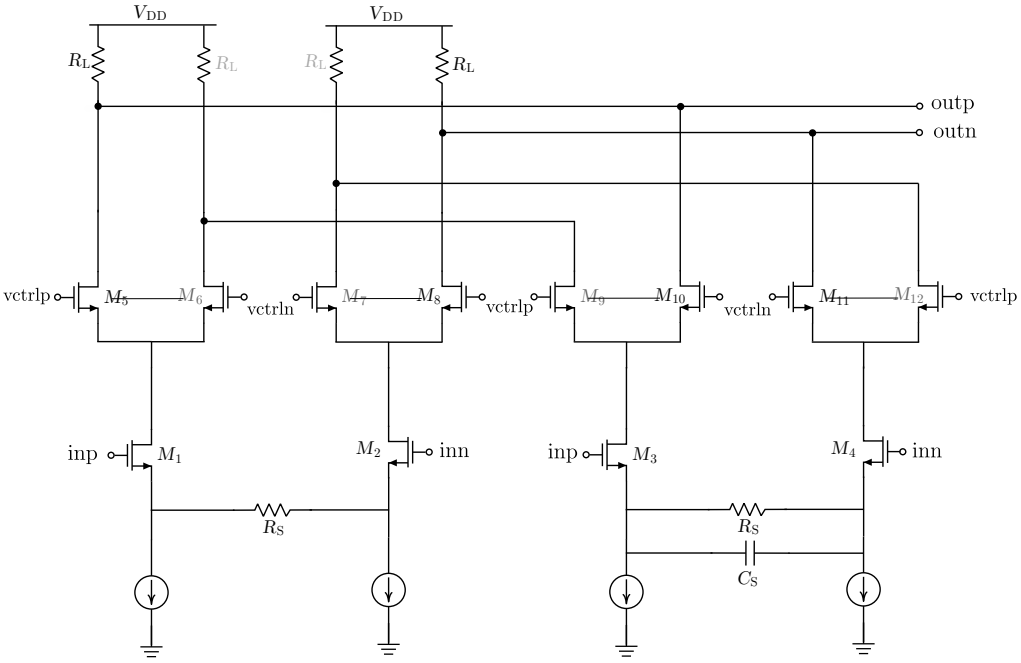

Figure 13: Programmable CTLE circuit topology.

Source: Author.

with capacitive peaking, introducing a zero to the response through the parallel capacitance, as discussed in the conventional CTLE topology.

The programmable nature of this design is achieved by combining the switching stages of these Gilbert cells. The transistors connected to the positive control voltage of one cell are paired with those linked to the negative control voltage of the other. The two additional switching transistors are connected to a branch leading to V_{DD}, ensuring that their current does not contribute to the output.

This arrangement allows modulation of the contributions from the flat-band and peaking currents by adjusting the gate voltages of the switching transistors. The voltage difference between vctrlp and vctrln controls the current steering from the transconductance stages.

When the condition (vctrlp > vctrln) is true by a sufficient margin, the current in the flat-band cell is predominantly directed to the branches connected to the output, resulting in a response that emphasizes the flat-band characteristic. Conversely, when (vctrln > vctrlp), the current in the peaking cell is steered towards the output while the current in the flat-band cell flows to V_{DD}, enhancing the peaking response. This mechanism provides programmable control over the equalization characteristics of the circuit.

It is important to highlight a few considerations regarding the circuit design. Firstly, resistances are included in the branches not connected to the output (drains of M6, M7, M8, and M12). This is necessary to prevent significant mismatches in the V_{DS} of the switching transistors, which could otherwise result in substantial variations in the A_{DC} when adjusting the peaking response. Al-

though some change in A_{DC} is unavoidable, the inclusion of these resistances mitigates the extent of such variations.

As the current distribution through each branch of the switching stage varies from adjustments in the transistors gate voltages V_G, the source voltage V_S of the switching transistors also changes. Considering the transconductance transistors, whose gate voltage V_G and drain current I_D are fixed by the biasing conditions, any alterations in their drain voltage(V_D—which corresponds to the source voltage V_S of the switching transistors—require changes in their own source voltage to sustain the set I_D.

This, in turn, impacts the overdrive voltage V_{ov} of these transconductance transistors. Since the transconductance gain is defined by $g_m = \frac{2I_D}{V_{\text{ov}}}$, fluctuations in V_{ov} lead to changes in the overall gain of the circuit. These variations in gain are an inherent characteristic of the design and must be managed to ensure consistent circuit performance.

To calculate the frequency response of the flat band and peaking cells, consider the conditions where the output is fully composed by only one of the cells and analyze the AC half-circuit of each one of them. To do this, the ideal current sources will be replaced with a transistor that is mirroring the current.

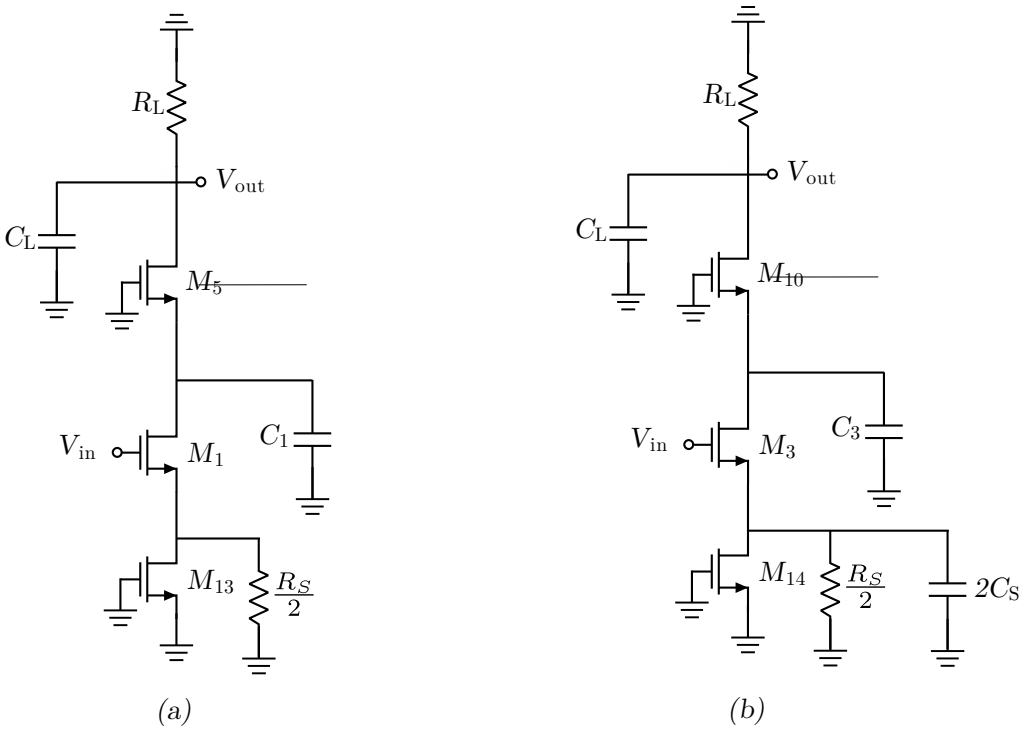

Figure 14: (a) Flat band cell AC half-circuit, (b) Peaking cell AC half-circuit

Source: Author.

Looking at Figure 14 (a) a pole-node approximation can be made to approximate the circuit's frequency response. It is important to note that no capacitance was added in the drain of M_{13}, that is because the parasitics at that node are not high enough to create a zero at a reasonable frequency.

At the V_{out} node, the capacitance C_L, composed of the input capacitance of the subsequent stage plus the parasitics of M5, and the parallel between the load resistance R_L and the resistance seen looking at M5's drain form a pole. Because the resistance looking at the drain of M5 is very high, R_L is the dominant resistance in the association and renders a good approximation.

$$\omega_{p5} = \frac{1}{C_L \cdot R_L} \tag{15}$$

The capacitance C_1 also creates a pole with the parallel of the resistances looking at M5's source and M1's drain.

$$\omega_{p1} = \frac{1}{C_1 \cdot \frac{1}{gm_5} || (gm_1 \cdot ro_1 \cdot ro_{13})} \approx \frac{g_{m5}}{C1} \tag{16}$$

The DC gain, because of the cascode stage characteristcs of a current buffer, can be approximated by using a degenerated common-source stage transconductance:

$$A_{\text{DC,f}} = \frac{g_{m1} R_L}{1 + g_{m1} R_S/2} \tag{17}$$

In the technology being used, there is a isolated deep well in the bulk area of the transistors, which will be used in all of them for gain enhancement, this makes source-to-bulk capacitances short-circuited and thus not considered.

The capacitance C_L can be decomposed by the association of the M1 parasitics and the load capacitance:

$$C_L = C_{DB5} + C_{GD5} + C_{\text{Load}} \tag{18}$$

The total capacitance C_1 is roughly equal to:

$$C_1 = 2C_{GD1} + C_{DB1} + C_{GS5} \tag{19}$$

Considering matching between both circuits, by analogy, the poles and gain of the peaking cell are:

$$\omega_{pl} = \omega_{p10} = \omega_{p5} = \frac{1}{C_L R_L}$$

$$\omega_{pc} = \omega_{p3} = \omega_{p1} \approx \frac{g_{m5}}{C1}$$

$$A_{\text{DC}} = A_{\text{DC,f}} = A_{\text{DC,p}} = \frac{g_{m1} R_L}{1 + g_{m1} R_S/2}$$

The difference is in the zero that the peaking circuit introduces, which is composed basically by the combination of the source degeneration resistance $R_S/2$ and the parallel capacitance $2C_S$

$$\omega_z = \frac{1}{C_S R_S} \tag{20}$$

Parameter	Formula
ω_{pl}	$\frac{1}{C_L R_L}$
ω_{pc}	$\frac{g_{m5}}{C_1}$
ω_z	$\frac{1}{C_S R_S}$
A_{DC}	$\frac{g_{m1} R_L}{1+g_{m1} R_S/2}$

Table 3: Programmable CTLE frequency response parameters and formulas.

Table 3 can be used as reference to design each of the following frequency response equations:

$$H_f(s) = A_{\mathrm{DC}} \cdot \frac{1}{(1 + s/\omega_{pl}) + (1 + s/\omega_{pc})} \tag{21}$$

$$H_p(s) = A_{\mathrm{DC}} \cdot \frac{1 + s/\omega_z}{(1 + s/\omega_{pl}) + (1 + s/\omega_{pc})} \tag{22}$$

2.4.3 α-generator circuit

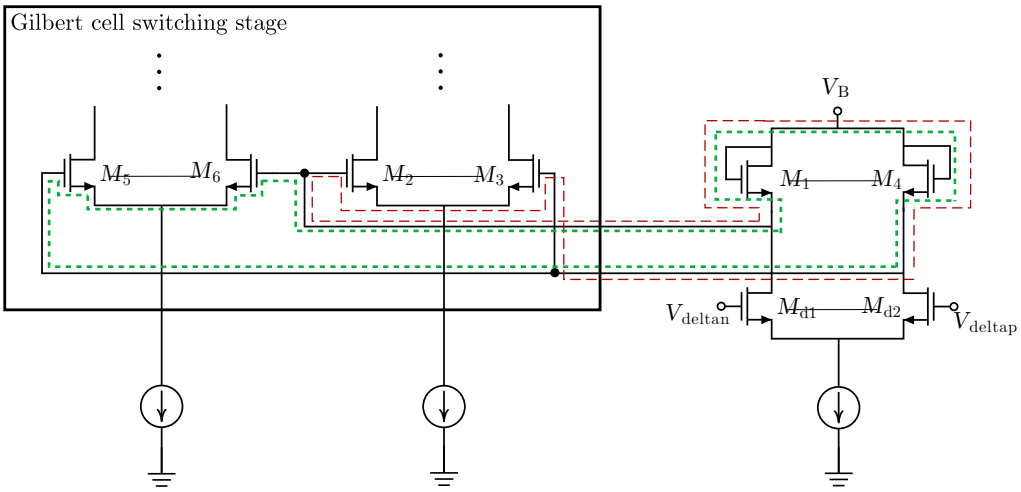

Figure 15: α-generator circuit topology.

Source: Author.

Figure 15 depicts the circuit used to precisely steer the current on the switching stages of the Gilbert Cell of the CTLE, for the sake of easier understanding this block will be called "α-generator" regarding the generation of a so called α in equation 14. The circuit works by utilizing two diode-connected transistors to form translinear loops with the switching stage pairs of the CTLE. A translinear loop is an analog circuit configuration that leverages the properties of MOSFETs to create specific current and voltage relationships.

In a translinear loop composed of four NMOS transistors, which is the case

for each CTLE switching pair when connected to this circuit, the transistors are connected in such a way that their gate-source voltage drops (V_{GS}) form a continuous loop. The core principle of this configuration is that the sum of V_{GS} voltages in one direction around the loop must equal the sum of V_{GS} voltages in the opposite direction. Mathematically, this equilibrium is represented as:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{23}$$

This condition ensures that the loop remains balanced in terms of voltage drops.

The translinear principle also states that the product of the drain currents flowing through the transistors in one direction around the loop must equal the product of the currents flowing in the opposite direction. For a loop of four NMOS transistors, this current relationship can be expressed, for a exponential MOSFET operating region as:

$$I_{D1} \cdot I_{D2} = I_{D3} \cdot I_{D4} \tag{24}$$

For a quadratic MOSFET operating region, it can be expressed as:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \tag{25}$$

This property allows the circuit to maintain a consistent relationship between the currents, enabling precise current scaling.

When analyzing changes in such a loop, suppose I_{D1} decreases by a small amount ΔI_D and I_{D4} increases by the same ΔI_D. To maintain the voltage balance, V_{GS1} will decrease while V_{GS4} increases. Consequently, V_{GS2} and V_{GS3} must adjust to keep the overall sum of gate-source voltages consistent.

By understanding this principle of operation, the balancing characteristics of these loops can be used to steer the current between the desired gilbert cell branches by modifying V_{GS1} and V_{GS4} of the diode-connected transistors. This modification can be achieved by introducing a unbalanced ($V_{\text{deltap}} - V_{\text{deltan}}$) signal in the input of the differential pair, creating a difference in the current passing through each branch. Because of the diode-connected characteristic of these transistors, $V_{GS} = f^{-1}(I_D)$, these differences in the currents translate directly to a V_{GS} difference between the diode-connected transistors and provokes a proportional difference in the switching transistors that respects their limitations, making the current between them steer from one branch to another.

2.5 Bandwidth extension techniques for CMOS circuits

In high-speed circuits, any parasitic capacitance created by the devices used in the circuit significantly reduce bandwidth, to counteract this bandwidth extension techniques must be used to the specified bandwidth can be achieved.

2.5.1 Shunt-inductive peaking

Shunt peaking is a technique used to extend bandwidth by connecting an inductor L in series with a load resistor R to shunt the output capacitance C. This setup can be analyzed through the circuit in Figure 16, where the gain is approximately given by the transconductance of the transistor multiplied by the output impedance: $H(s) = g_m \cdot Z(s)$.

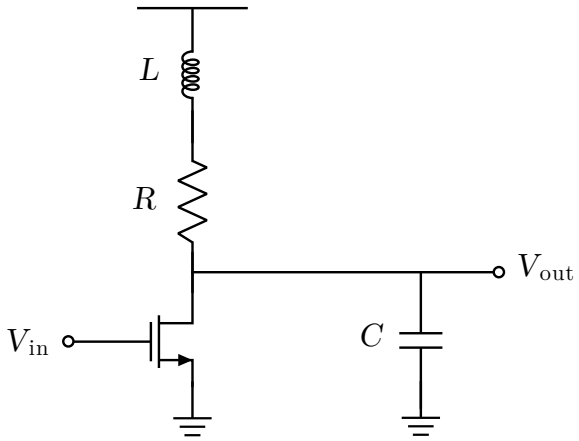

Figure 16: Shunted inductive peaking circuit.

Source: Author.

$$Z(s) = \left(\frac{1}{sC}\right) \parallel (R + sL) = \frac{R + sL}{1 + sRC + s^2LC} \tag{26}$$

Looking at the output impedance it shows that the inductor creates a zero in $Z(s)$, which increases impedance at higher frequencies, counteracting the falling impedance of C and thereby broadening the bandwidth. Another way to understand this bandwidth enhancement is through the concept of reduced rise-time: the inductor temporarily delays current flow into the resistive branch, allowing more initial current to charge C, thus reducing the rise-time [10].

2.5.2 Series-inductive peaking

In circuit designs where the drain parasitic capacitance is significant, achieving an improved bandwidth can be accomplished through capacitive splitting. This technique involves inserting an inductor L to divide the total load capacitance into two separate components. To illustrate this effect, consider the circuit shown in Figure 6. Looking at the load impedance $Z(s) = (R||Z_{C_1})||(Z_L + Z_{C2})$, the formula is given by:

$$Z(s) = \frac{R + s^2RLC_2}{s^3RLC_1C_2 + s^2LC_2 + sR(C_1 + C_2) + 1} \tag{27}$$

By separating the output capacitance C_1 from the input capacitance of the next stage, C_2, an additional pole is introduced into the system, which can be

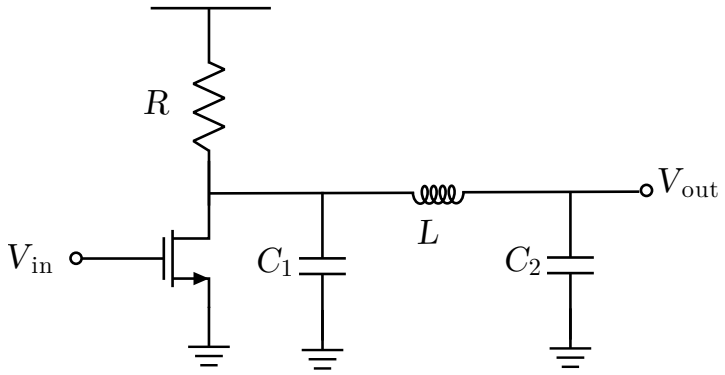

Figure 17: Series inductive peaking circuit.

Source: Author.

confirmed by the numerator of $Z(s)$.

To gain further understanding of the increased bandwidth provided by capacitive splitting, the charging scenario without the inductor L can be analyzed, in this configuration the transistor charges the entire load capacitance $C_1 + C_2$, which can slow down the response. However, when L is included, it initially delays the current flow to the main load capacitance $C_1 + C_2$, causing only the stage's output capacitance C_1 to be charged at first. This delay allows for a faster rise time at the drain, effectively enhancing the bandwidth of the amplifier [10].

2.5.3 Source-degeneration and capacitive degeneration peaking

A well-known technique to speed up the input pole of a transistor is the use of series feedback. A source degeneration resistance introduces a series feedback which lowers the input capacitance of transistor by the virtue of Miller Effect. Figure 18 shows how the parasitic capacitance C_{GS}, with the addition of the source resistance R_S, is now susceptible to a gain between the nodes V_G and V_S, because V_S is no longer connected to ground.

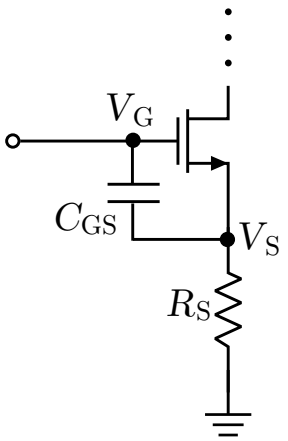

Figure 18: Degenerative resistance miller effect scenario.

Source: Author.

The $\frac{V_G}{V_S}$ gain is easily calculated equating V_S to the voltage drop on R_S.

$$g_m(V_G - V_S)R_S = V_S$$

$$A = \frac{V_G}{V_S} = \frac{g_m R_S}{1 + g_m R_S}$$

The capacitance seen at the input of the transistor is now:

$$C_{\text{in}} = C_{GS}(1 - \frac{g_m R_S}{1 + g_m R_S})$$

Simplifiying the terms we have:

$$C_{GS,in} = \frac{C_{GS}}{1 + g_m R_S} \tag{28}$$

This way, a degenerative resistance lowers the input capacitance of the driver by a factor of $(1 + g_m R_S)$ improving it's bandwidth.

Adding a capacitance in parallel to the degenerative resistance, as previous analyzed in section 2.4.2, and depicted in Figure 14, adds a zero to the circuit which can counteract the pole provided by the output capacitance [1].

2.5.4 Cascode amplifier

To reduce the influence of the C_{GD} capacitance on the bandwidth of a common-source topolgy, the cascode configuration can be employed. The cascode amplifier, illustrated in Figure 19 (b), can be interpreted as a common-source stage with its output connected to a common-gate amplifier. The gain of the first stage is determined by the transconductance g_{m1} multiplied by the impedance seen at the drain.

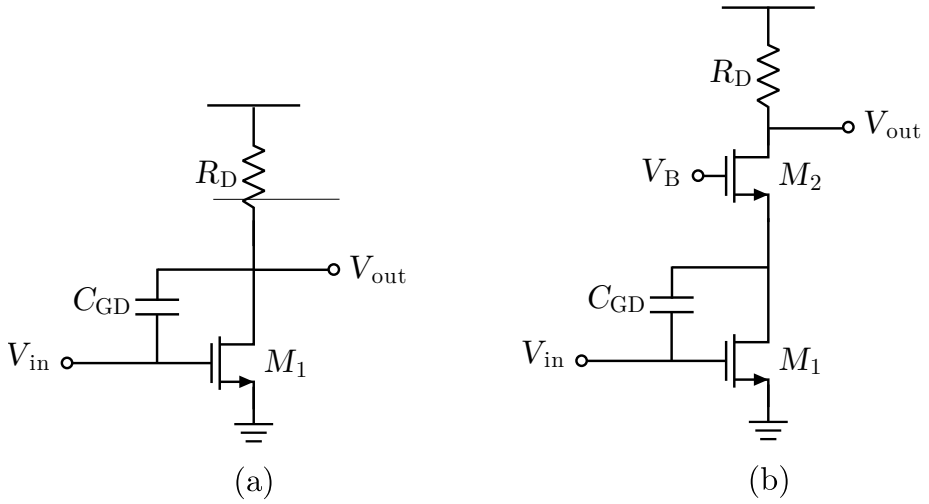

Figure 19: (a) Common-source stage (b) Cascode stage.

Source: Author.

This impedance is calculated as the impedance seen at the source of M_2. The impedance seen at the source in this scenario can be approximated to $1/g_{m2}$.

Compared to the gain $A = \frac{V_D}{V_G}$ before the introduction of the cascode transistor, which was $A = -g_{m1}R_D$, the new gain with the introduction of this cascode transistors will be

$$A = \frac{-g_{m1}}{g_{m2}}$$

.

Considering $g_{m1} \approx g_{m2}$, this will equate to $A \approx -1$. With this gain reduction, the Miller effect in the common-source stage is significantly diminished. Consequently, the capacitance seen at the input because of C_{GD} can be represented as:

$$C_{\text{GD,in}} = C_{GD}(1 - A) = +2C_{GD} \tag{29}$$

Which is lower than the capacitance of a pure common source stage, represented in Figure 19, granted that $g_m R_D > 1$.

$$C_{\text{GD,in}} = (1 + g_m R_D)C_{GD}$$

Thus, the input capacitance is reduced compared to a single-transistor amplifier. Also, because the cascode device acts as a buffer for current, the transconductance of the common-source stage travels to the output, making the amplifier have the same simplified gain of $-g_{m1}R_D$ [1].

This technique can be combine with source-degeneration, making the gain even lower. With a resistance at the source, the transconductance of the common-source will equal to $G_m = g_{m1}/(1 + g_{m1}R_S)$, which will change the gain to

$$A = \frac{-g_{m1}/g_{m2}}{1 + g_{m1}R_S}$$

This will reduce even more the contribution of the C_{GD} to the input

$$C_{\text{GD,in}} = C_{GD}(1 - A) = C_{GD} \cdot \left(1 + \frac{g_{m1}}{g_{m2}(1 + g_{m1}R_S)}\right) \tag{30}$$

2.5.5 Capacitance suppresion by interstage buffers

Consider two consecutive stages as shown in Figure 20 (a). The total load capacitance seen by the first stage consists of two main components: the stage self-loading output capacitance, C_{out},and the next-stage input loading capacitance, C_{in}. For simplicity, we ignore the interconnect capacitance in the following analysis. This load capacitance determines the speed of the first stage's output pole(s). For example, if the first stage has a simple resistive load, the frequency

of the output pole is about

$$\frac{1}{2\pi \cdot R_D(C_{\text{in}} + C_{\text{out}})}$$

where R_D is the load resistor.

The next-stage loading can be reduced by inserting buffers in between the stages. Figure 20 (b) shows how two stages can be decoupled with a source-follower buffer. The buffer has an input capacitance, $C_{\text{in'}}$, which is κ times smaller than the load capacitance, C_{in}, it is designed to drive:

$$C_{\text{in'}} = \frac{C_{\text{in}}}{\kappa}. \tag{31}$$

Because the buffer's input capacitance is a fraction of the load capacitance, whereas (ideally) the input and output voltages are the same, the buffer can be regarded as a capacitance transformer. But note that a change in the load capacitance requires the resizing of the buffer to realize the corresponding change in input capacitance (and to maintain the same buffer bandwidth). We can conclude [11] that inserting the buffer increases the bandwidth due to the output pole(s) to

$$\text{BW'} = \frac{1 + C_{\text{in'}}/C_{\text{out}}}{1 + (C_{\text{in}}/C_{\text{out}})/\kappa} \cdot \text{BW} \tag{32}$$

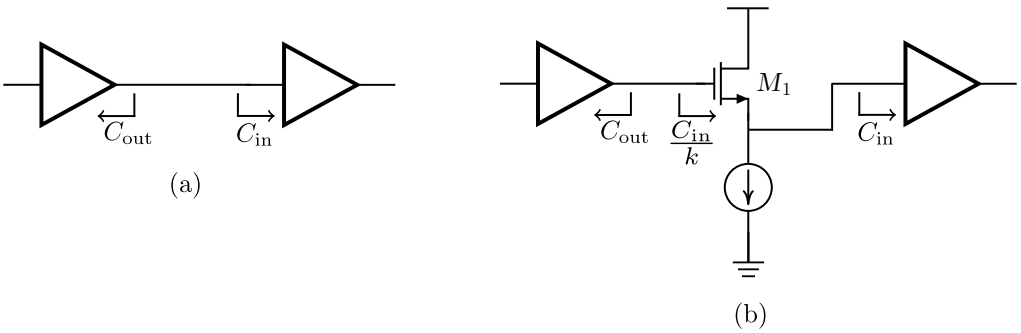

Figure 20: (a) Two consecutive stages without interstage buffer (b) Two consecutive stages with interstage buffer

Source: Author.

In practice, the bandwidth gained by this technique is partially offset by the bandwidth lost because of the finite buffer bandwidth and signal attenuation in the buffer. In particular, there is a trade-off between the capacitance transformation ratio, κ, and the buffer bandwidth, BW_B: a large source follower with a large g_m has a high bandwidth but also a fairly large input capacitance and thus a low κ, whereas a small source follower, which is easily loaded down by the output capacitance, has a low bandwidth but also a small input capacitance and thus a high κ [11].

3 Design of a MZM driver with programmable continuous-time linear equalizer on 65nm CMOS

This chapter presents the design of the MZM driver in 65nm CMOS technology, detailing its operation and providing an in-depth description and mathematical modeling of each block's desired parameters, considerations and trade-offs. A methodology is established to achieve the desired specifications, followed by a discussion of the simulation results obtained.

3.1 Specifications and top-level topology

This project is a collaborative effort between Chipus Microelectronics and the LRF (UFSC). Through joint discussions, an agreement was reached to design a Mach-Zehnder Modulator (MZM) driver for high-speed optical communications, utilizing 65nm CMOS technology. The project aims to meet the following agreed minimum specifications displayed in Table 4.

Parameter	**Value**
Modulation Format	PAM4
Minimum Bandwidth (GHz)	23
Minimum Output Swing (Vpp,d)	1.2
Maximum THD (%) at Vpp,d	6
Minimum Voltage Gain (dB)	6.5
Maximum DC Power Consumption (mW)	650
Data Rate (Gbaud)	28
Data Rate (Gb/s)	56
Maximum Energy Efficiency (Consumption) (pJ/bit)	11.6
CTLE Min./Max. Peaking Gain (dB)	0 - 6
CTLE Maximum Peaking DC Gain Variation (dB)	0.4
Temperature Range (ºC)	0 - 60
Voltage Source (V)	3
Current Source (mA)	1
Technology	65nm CMOS
Measurement Scope	Simulated

Table 4: Minimum design specifications for the MZM driver with programmable equalization.

Based on the topologies discussed in the previous sections, along with the bandwidth extension techniques, a preliminary top-level circuit is evaluated as a solution for driving a Mach-Zehnder modulator, with the added capability of programmable equalization to achieve the wanted specifications. As shown in Figure 21, the top-level circuit comprises of an input buffer, which maintains matching between the signal-generating block and the driver through R_{in}, followed by a programmable CTLE. Between these stages, a series inductor peaking technique is used. This approach is particularly suitable because the input of the CTLE contains four transistors, as seen in Figure 13. These transistors form

the transconductance and gain of the block, meaning they are sizable and have significant parasitic capacitances. Consequently, the highest capacitance in the circuit is found at these nodes, making peaking an effective choice for bandwidth extension.

Following the CTLE, an interstage buffer is used to reduce the capacitance seen by the transistors. This is because the load resistance of the CTLE, to achieve significant peaking and gain, must have a high value. Thus, it is advantageous to suppress the capacitance at the CTLE output to ease its pole. Finally, the driver circuit connects to the load, which is the equivalent circuit of a Mach-Zehnder modulator. The driver's output resistance R_{out} should aim to match the terminations of the Mach-Zehnder modulator for optimal signal transmission. Additionally, to counteract parasitic and channel capacitances, bandwidth is further enhanced through inductive peaking in these resistors. Other techniques, such as resistive and capacitive degeneration, can also be applied in the driver to ensure high-speed operation and bandwidth stability.

This design provides a robust approach to address the established requirements and specifications.

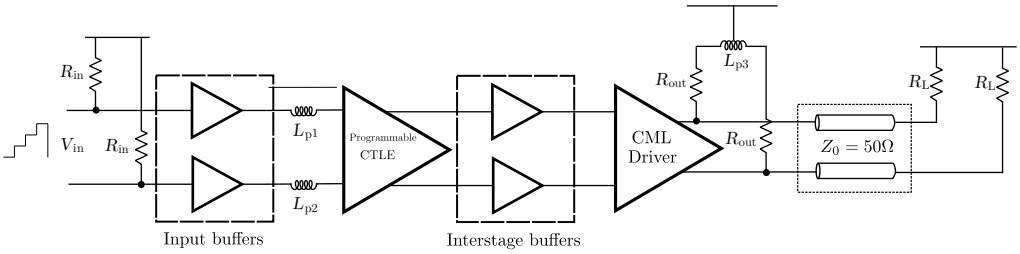

Figure 21: Top-level circuit topology

Source: Author

3.2 Design of the source-follower buffers

3.2.1 Input buffer

The primary, and most critical, buffer serves two main purposes. First, it ensures that the input maintains a buffered impedance close to 50 Ω, thereby minimizing reflections in the incoming PAM4 signal. Second, as previously mentioned, series-inductive peaking is applied at the output of this buffer, as this node accumulates the highest parasitic capacitance among the blocks due to its connection to the CTLE. A source-follower topology was chosen for the buffer function.

It is important to note that the 65nm technology transistors have a maximum voltage tolerance of 1.2V between their terminals. Therefore, to keep these transistors within their Safe Operating Area (SOA), voltage drops must be induced to enable safe operation of the source-follower. Additionally, the technology includes an isolated well for the bulk, allowing it to be connected to the source, which enhances gain by eliminating the body effect on V_{TH}.

The circuit configuration is shown in Figure 22.

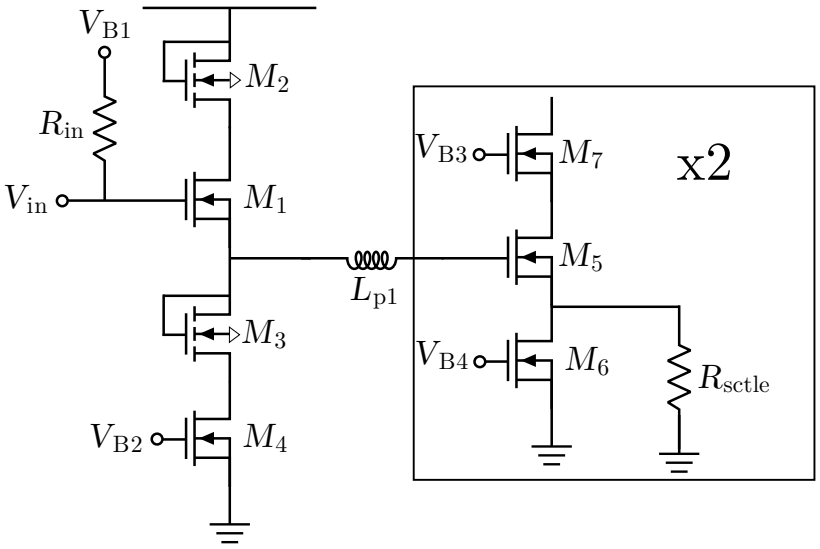

Figure 22: Input buffer circuit

Source: Author

It is noted that the CTLE circuit's biasing comes from the input buffer's bias voltage, V_{B1}, which must be selected to allow saturation of transistors $M5$ and $M6$.

To analyze the frequency response of this circuit, we refer to Figure 23, where the capacitances creating the dominant poles are shown. In the AC model, transistors $M2$, $M3$, and $M4$ can be represented as resistances with values:

$$R_{D,\text{buff}} = \left(\frac{1}{g_{m2}} || r_{o2}\right) \tag{33}$$

$$R_{S,\text{buff}} = \left(\frac{1}{g_{m3}} || r_{o3}\right) + r_{o4} \tag{34}$$

The source impedance of this circuit, denoted by $Z_S(s)$, is analogous to that in equation 27. The gain $A(s)$ is given by:

$$A(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_{m1} Z_S(s)}{1 + g_{m1} Z_S(s)}$$

Thus, the frequency response of the circuit, with a detailed derivation provided in Appendix A.1, is:

$$A(s) = \frac{g_{m1} R_S \left(1 + s^2 L_p C_{\text{in}}\right)}{1 + g_{m1} R_S + s R_S \left(C_{\text{in}} + C_{\text{out}}\right) + s^2 L_p C_{\text{in}} \left(1 + g_{m1} R_S\right) + s^3 R_S L_p C_{\text{out}} C_{\text{in}}} \tag{35}$$

The zeros of $A(s)$ occur when its numerator $N(s) = 0$, leading to:

$$g_{m1} R_S \left(s^2 L_p C_{\text{in}} + 1\right) = 0$$

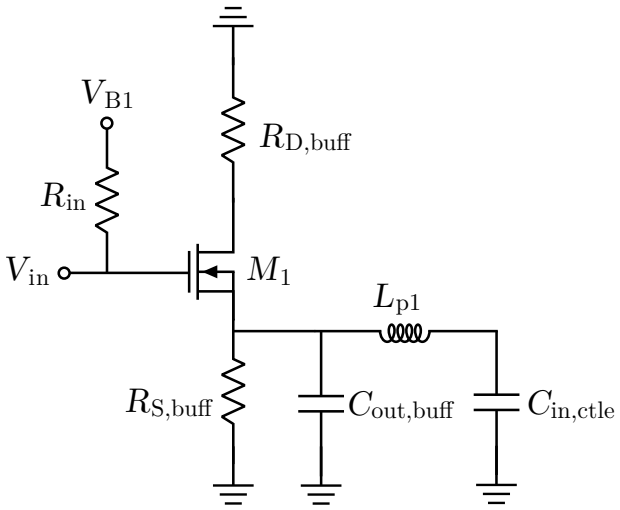

Figure 23: AC model of the input buffer circuit

Source: Author

Since g_{m1} and R_S are positive constants, the zero occurs when:

$$s^2 L_p C_{\text{in}} + 1 = 0 \Rightarrow s^2 = -\frac{1}{L_p C_{\text{in}}}$$

This indicates the presence of zeros at:

$$s = \pm j\omega_z, \quad \omega_z = \frac{1}{\sqrt{L_p C_{\text{in}}}} \tag{36}$$

At low frequencies ($s \to 0$), higher-order terms can be neglected, resulting in the low-frequency gain:

$$A(0) = \frac{g_{m1} R_S}{1 + g_{m1} R_S} \tag{37}$$

At high frequencies ($s \to \infty$), higher-order terms dominate, causing the gain to roll off as:

$$A_{high}(s) \approx \frac{g_{m1} C_{\text{in}}}{s C_{\text{out}}} \tag{38}$$

The capacitances of interest, C_{in} and C_{out}, can be approximated as:

$$C_{\text{out}} = C_{\text{DS1}} + C_{\text{DB1}} + C_{\text{DB3}} \tag{39}$$

$$C_{\text{in}} \approx 2 \cdot \left(C_{\text{GD5}} \left(1 + \frac{g_{m5}/g_{m7}}{1 + g_{m5} R_{\text{sctle}}} \right) + \frac{C_{\text{GS5}}}{1 + g_{m5} R_{\text{sctle}}} \right) \tag{40}$$

This capacitance calculation assumes that the CTLE source resistance, R_{sctle}, is the dominant resistance at the node. Consequently, the gains used in the Miller effect analysis for calculating C_{in} approximate the resistance to R_{sctle}. Additionally, it is assumed that the inverse of the common-gate gain of transistor

$M7$ is much less than one. This allows us to neglect the Miller effect on the drain-source capacitances, as the gain factor $\left(1-\frac{1}{A}\right) = \left(1-\frac{1}{\text{Common-gate gain}}\right) \approx 1$ results in the full presence of the drain-source capacitance at the source node.

Furthermore, it is assumed that the gain of the source-follower stage is sufficiently close to unity, effectively minimizing the Miller effect at the output. This can be further understood by examining the current through the gate-source capacitance C_{GS}, given by:

$$i_{C_{GS}} = C_{GS}\left(\frac{dv_G}{dt} - \frac{dv_S}{dt}\right) \tag{41}$$

Since, under small-signal operation, $\frac{dv_G}{dt} \approx \frac{dv_S}{dt}$, it follows that $i_{C_{GS}} \approx 0$, meaning that the gate-source capacitance C_{GS} has negligible effect on the output.

Note in the equation for the CTLE's input capacitance how the use of cascode transistors and degeneration resistance reduces the input node capacitance.

A couple tables summarizing key design equations, important design considerations, and trade-offs associated with varying circuit parameters are presented. These resources aim to assist in the systematic design of the input buffer circuit. Table 5 summarizes the key equations that can be used to approximate the design parameters. Table 6 displays some of the considerations that should be taken into account while designing this buffer, and Table 7 summarizes the trade-offs of the design.

Table 5: Key design equations for Input Buffer design

Parameter	**Equation**
Source Resistance of Buffer ($R_{S,\text{buff}}$)	$R_{S,\text{buff}} = \left(\frac{1}{g_{m3}} \parallel r_{o3}\right) + r_{o4}$
Low-Frequency Gain ($A(0)$)	$A(0) = \frac{g_{m1}R_S}{1+g_{m1}R_S}$
Zero Frequency (ω_z)	$\omega_z = \frac{1}{\sqrt{L_p C_{\text{in}}}}$
High-Frequency Gain Approximation	$A_{high}(s) \approx \frac{g_{m1}C_{\text{in}}}{sC_{\text{out}}}$
Input Capacitance (C_{in})	$C_{\text{in}} \approx 2 \cdot \left(C_{\text{GD5}}\left(1+\frac{g_{m5}/g_{m7}}{1+g_{m5}R_{\text{sctle}}}\right) + \frac{C_{\text{GS5}}}{1+g_{m5}R_{\text{sctle}}}\right)$
Output Capacitance (C_{out})	$C_{\text{out}} \approx C_{\text{DS1}} + C_{\text{DB1}} + C_{\text{DB3}}$

Table 6: Design considerations for the Input Buffer

Consideration	**Description**
Safe Operating Area (SOA) Compliance	The 65nm technology transistors have a maximum voltage tolerance of 1.2V between their terminals. Voltage drops must be induced to keep transistors within their Safe Operating Area (SOA).
Bulk Connection	The technology includes an isolated well for the bulk, allowing it to be connected to the source. This enhances gain by eliminating the body effect on V_{TH}.
Bias Voltage V_{B1}	The CTLE circuit's biasing comes from the input buffer's bias voltage V_{B1}, which must be selected to ensure saturation of transistors $M5$ and $M6$.

Table 7: Design Trade-offs for the Input Buffer design

Parameter	**Increasing Value**	**Decreasing Value**
Transconduc. g_{m1}	Gain approaches unity; Bandwidth increases; Power consumption or parasitics increases;.	Gain decreases; Bandwidth decreases; Power consumption or parasitics decreases;
Inductance L_p	Bandwidth extension via inductive peaking; Potential peaking in frequency response; Integration difficulty due to size.	Reduced peaking effect; Bandwidth may be limited; Simplifies circuit integration.
Source Resistance $R_{S,\text{buff}}$	Higher linearity; Lower pole frequencies.	Lower linearity; Higher pole frequencies;.
Transistor Sizing (Width W**)**	Increases g_m and capacitances; Improves gain and bandwidth; Increases parasitic capacitance.	Decreases g_m and capacitances; Reduces gain and bandwidth; Lowers parasitic capacitance.
Bias Current I_D	Increases g_m; Higher power consumption; Potential thermal issues.	Decreases g_m; Lower power consumption; Reduced thermal stress.

3.2.2 Interstage Buffer

The interstage buffer, as discussed in Section 2.5.5, serves to present a lower load capacitance to the CTLE stage than would be observed with a direct connection to the driver. Like the input buffer, a source-follower topology is employed to implement this buffer, adhering to the same considerations regarding the 1.2V SOA limitation of the transistors. The source is connected to the bulk through the isolated well available in the 65nm CMOS technology, allowing an increase in the transistor's g_m by eliminating the body effect in V_{TH}. Consequently, the design of this buffer must focus on delivering a low capacitance at the input while maintaining adequate bandwidth and minimizing any degradation of the overall gain. The topology of this buffer is similar to the input buffer but does not

employ inductive peaking, as shown in Figure 24. An important consideration in this design is that the gate-source voltage V_{GS1} must be sufficient to maintain the transistors $M5$ and $M6$ in saturation. Although the common-mode input voltage of this circuit is not a design parameter of this block, beign a CTLE design parameter instead, careful attention must be given to ensure proper biasing.

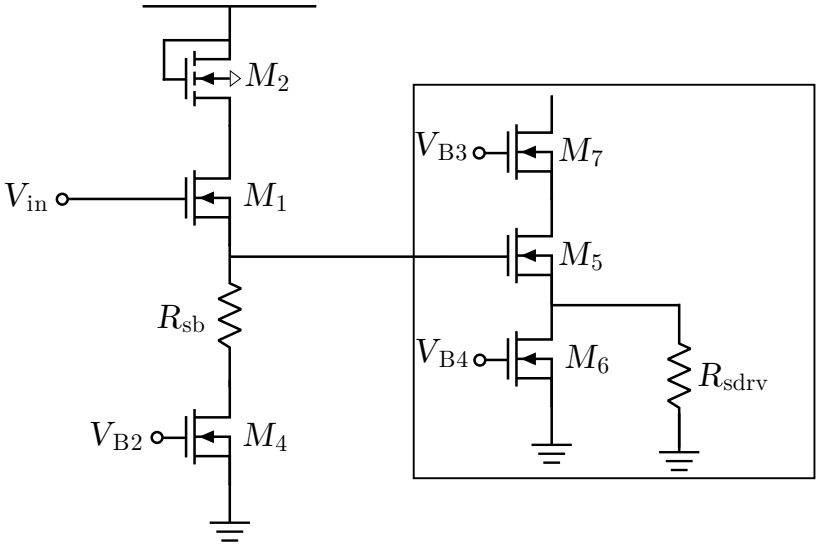

Figure 24: Interstage buffer circuit

Source: Author

Two primary design differences exist in this buffer. First, rather than using a diode-connected transistor to create the voltage drop between the source-follower transistor and its current source, a resistor is employed. This simplifies the design and nominally controls the source impedance of the amplifier, thereby facilitating control over the capacitance at its input. Figure 25 shows the equivalent AC model of the circuit, highlighting the capacitances of interest.

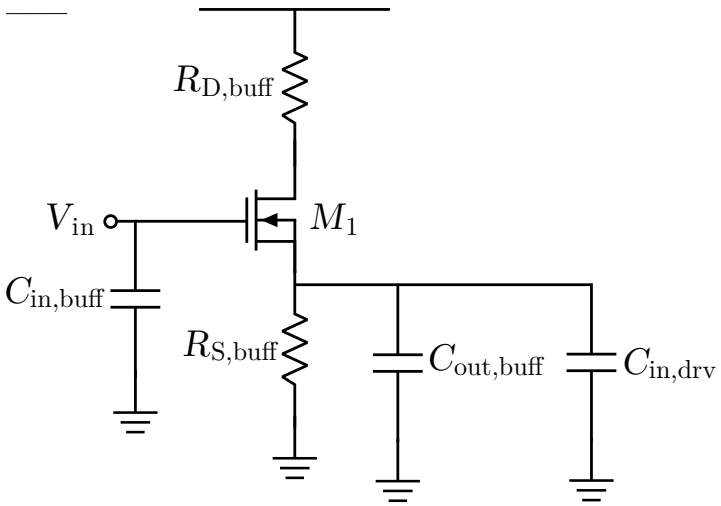

Figure 25: AC model of the interstage buffer circuit

Source: Author

The relevant parameters of the circuit are given by:

$$R_{D,\text{buff}} = \left(\frac{1}{g_{m2}} || r_{o2}\right) \tag{42}$$

$$R_{S,\text{buff}} = R_{sb} + r_{o4} \tag{43}$$

Analogous to the analysis of the input buffer, the frequency response of this circuit can be approximated as:

$$A(s) = \frac{g_{m1} Z(s)}{1 + g_{m1} Z(s)}$$

The source impedance, $Z(s)$, is defined by

$$Z(s) = R_{S,\text{buff}} || \left(\frac{1}{s(C_{\text{out, buff}} + C_{\text{in, drv}})}\right)$$

By substituting and simplifying terms in both the numerator and the denominator, we arrive at:

$$A(s) = \frac{g_{m1} R_{S,\text{buff}}}{1 + g_{m1} R_{S,\text{buff}} + s \cdot R_{S,\text{buff}} \cdot (C_{\text{out, buff}} + C_{\text{in, drv}})} \tag{44}$$

The low-frequency (DC) gain $A(0)$ as

$$A(0) = \frac{g_{m1} R_{S,\text{buff}}}{1 + g_{m1} R_{S,\text{buff}}} \tag{45}$$

and the pole frequency ω_p as

$$\omega_p = \frac{1 + g_{m1} R_{S,\text{buff}}}{R_{S,\text{buff}}(C_{\text{out, buff}} + C_{\text{in, drv}})}. \tag{46}$$

The input capacitance of the buffer, $C_{\text{in, buff}}$, can be calculated as:

$$C_{\text{in, buff}} = \frac{(C_{\text{GS1}} + C_{\text{GB1}})}{1 + g_{m1} R_{S,\text{buff}}} + C_{\text{GD1}} \left(1 + \frac{g_{m1} R_{D,\text{buff}}}{1 + g_{m1} R_{S,\text{buff}}}\right) \tag{47}$$

The input capacitance of the driver, $C_{\text{in, drv}}$, is given by:

$$C_{\text{in, drv}} = \frac{(C_{\text{GS5}} + C_{\text{GB5}})}{1 + g_{m5} R_{sdrv}} + C_{\text{GD5}} \left(1 + \frac{g_{m5}/g_{m7}}{1 + g_{m1} R_{Sdrv}}\right) \tag{48}$$

Since the transistor $M5$ provides the transconductance gain of the driver and the current of this circuit is constrained by the swing specification so it cannot be adjusted to modify the gain. The gain must instead be achieved by increasing the width W of the driver's amplifier transistor, which results in large parasitic capacitances $C_{\text{GS5}}, C_{\text{GB5}}$, and C_{GD5}. Furthermore, the resistance R_{sdrv} is limited by the output impedance, which must approximate 50Ω to match the load receiving the driver. Thus, R_{sdrv} cannot be extensively utilized to reduce the capacitance $C_{\text{in, drv}}$, making this interstage buffer a good choice for lowering

the input capacitance seen by the CTLE.

By analogy, the output capacitance $C_{\text{out,buff}}$ of the interstage buffer can be calculated similarly to the method used for the input buffer, applying the same assumptions. This approach yields the following equation:

$$C_{\text{out, buff}} = C_{\text{DS1}} + C_{\text{DB1}} \tag{49}$$

Table 8: Key design equations for Interstage Buffer design

Parameter	**Equation**
Drain Resistance of Buffer ($R_{D,\text{buff}}$)	$R_{D,\text{buff}} = \left(\frac{1}{g_{m2}} \parallel r_{o2}\right)$
Source Resistance of Buffer ($R_{S,\text{buff}}$)	$R_{S,\text{buff}} = R_{sb} + r_{o4}$
Low-Frequency Gain ($A(0)$)	$A(0) = \frac{g_{m1} R_{S,\text{buff}}}{1 + g_{m1} R_{S,\text{buff}}}$
Pole Frequency (ω_p)	$\omega_p = \frac{1 + g_{m1} R_{S,\text{buff}}}{R_{S,\text{buff}} \left(C_{\text{out,buff}} + C_{\text{in,drv}}\right)}$
Input Capacitance of Buffer ($C_{\text{in,buff}}$)	$\frac{C_{\text{GS1}} + C_{\text{GB1}}}{1 + g_{m1} R_{S,\text{buff}}} + C_{\text{GD1}} \left(1 + \frac{g_{m1} R_{D,\text{buff}}}{1 + g_{m1} R_{S,\text{buff}}}\right)$
Input Capacitance of Driver ($C_{\text{in,drv}}$)	$\frac{C_{\text{GS5}} + C_{\text{GB5}}}{1 + g_{m5} R_{sdrv}} + C_{\text{GD5}} \left(1 + \frac{g_{m5}/g_{m7}}{1 + g_{m5} R_{Sdrv}}\right)$
Output Capacitance of Buffer ($C_{\text{out,buff}}$)	$C_{\text{out,buff}} = C_{\text{DS1}} + C_{\text{DB1}}$

Table 9: Design considerations for the Interstage Buffer

Consideration	**Description**
Safe Operating Area (SOA) Compliance	The 65 nm technology transistors have a maximum voltage tolerance of 1.2 V between their terminals. The design must ensure voltage drops are within this SOA limit.
Bulk Connection	The source is connected to the bulk via the isolated well, eliminating the body effect in V_{TH} and increasing the transistor's g_m.
Gate-Source Voltage V_{GS1}	V_{GS1} must be sufficient to keep transistors $M5$ and $M6$ in saturation.
Common-Mode Voltage Biasing	Although the common-mode voltage is determined by the CTLE, proper biasing is essential for correct operation.

Table 10: Design trade-offs for the Interstage Buffer design

Parameter	**Increasing Value**	**Decreasing Value**
Transconduc. g_{m1}	Improves gain; Reduces input capacitance due to higher $g_{m1}R_{S,\text{buff}}$; May increase power consumption and parasitic effects.	Reduces gain; Increases input capacitance; Lowers power consumption and parasitics.
Source Resistance $R_{S,\text{buff}}$	Increases $g_{m1}R_{S,\text{buff}}$, improving linearity and reducing input capacitance; May lower bandwidth due to increased pole frequency.	Decreases $g_{m1}R_{S,\text{buff}}$; Increases input capacitance; Enhances bandwidth but may degrade linearity.
Transistor Width W	Increases g_m and parasitic capacitances; Improves gain; May decrease bandwidth due to higher $C_{\text{in,buff}}$.	Decreases g_m and parasitics; Reduces gain; Can enhance bandwidth by lowering $C_{\text{in,buff}}$.
Bias Current I_D	Increases g_m; Improves gain and reduces input capacitance; Increases power consumption.	Decreases g_m; Reduces gain and increases input capacitance; Lowers power consumption.
Gate-Source Voltage V_{GS1}	Ensures transistors remain in saturation; May require adjustments in biasing; Affects g_m and linearity.	Risk of transistors entering triode region; Simplifies biasing; May reduce g_m and affect performance.

3.3 Design of the Mach-Zehnder modulator driver

The Mach-Zehnder modulator (MZM) driver will follow the CML architecture discussed in Section 2.3. To ensure the required minimum operational bandwidth, certain modifications will be introduced. In addition to cascode transistors, a degeneration resistance will be added to reduce input capacitance and increase linearity, along with two types of peaking. The first is a capacitive degeneration peaking, achieved through a capacitor placed in parallel with the degeneration resistor. The second is a symmetric inductor in the output resistors, creating shunt-inductive peaking. The symmetric arrangement of both the inductor and capacitor is important for minimizing the circuit's area, as only one device is needed to influence both branches within the frequency response. Additionally, the isolated well in the bulk is used to increase the gain by mitigating the body effect. The circuit schematic can be seen in Figure 26.

The output resistance, R_{out}, must match the load resistance R_L for proper matching with the load. Given that the MZM has a characteristic termination of 50Ω, it follows that $R_{out} = R_L = 50\Omega$.

The bias voltage V_{B2} must be chosen to keep transistors $M1$, $M4$, $M5$, and $M6$ in saturation while maintaining the desired output swing.

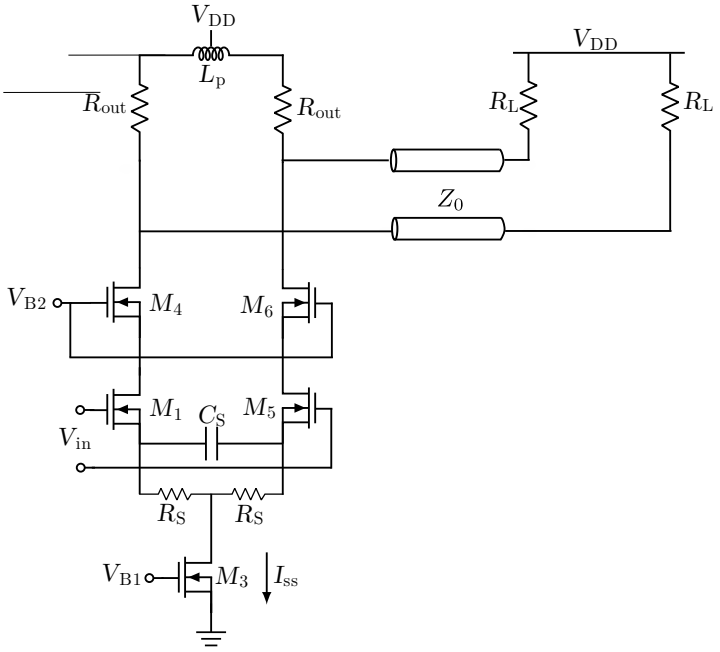

Figure 26: CML circuit design

Source: Author

As characterized in Section 2.3.1, the output swing of this circuit is given by

$$V_{\text{pp,d}} = 2 \cdot I_{SS} \cdot \frac{R_L}{2} = I_{SS} \cdot R_L$$

The power consumption for a given $V_{\text{pp,d}}$ is calculated as

$$\text{Power}_{\text{CML}} = \left(\frac{V_{\text{pp,d}}}{2} + V_{\text{out,min}} \right) \cdot \frac{V_{\text{pp,d}}}{R_L}$$

The frequency response of this circuit can be determined by analyzing the half-circuit of the differential pair, illustrated in Figure 27.

Considering $M4$ as a current buffer, the circuit's transconductance can be defined as

$$G_m = -\frac{g_{m1}}{1 + g_{m1} Z_S(s)}$$

Thus, the frequency response of the circuit can be approximated by

$$A(s) = G_m Z_{out}(s) = -\frac{g_{m1} Z_{out}(s)}{1 + g_{m1} Z_S(s)}$$

The source and output impedances, $Z_S(s)$ and $Z_{out}(s)$, can be expressed as follows:

$$Z_S(s) = \left(R_S || \frac{1}{s \cdot 2C_S} \right)$$

$$Z_{out}(s) = \left(\frac{R_L}{2} + s\frac{L_p}{2} \right) || \frac{1}{sC_L}$$

This leads to the approximate frequency response

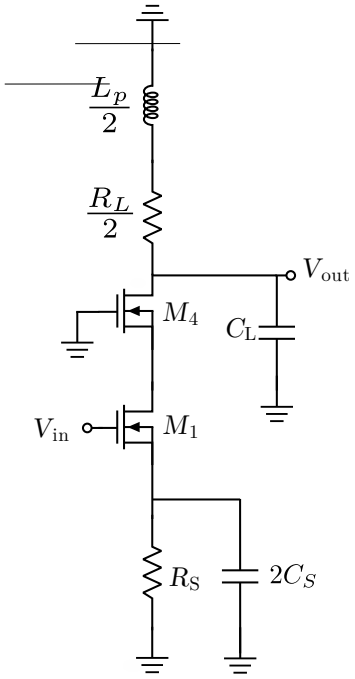

Figure 27: CML circuit AC equivalent

Source: Author

$$A(s) = -\frac{g_{m1}(R_L + sL_p)\left[1 + s \cdot 2C_S R_S\right]}{\left[(R_L + sL_p)sC_L + 2\right]\left[1 + s \cdot 2C_S R_S + g_{m1}R_S\right]} \tag{50}$$

The zeros of this response are given by:

$$\omega_{z1} = \frac{R_L}{L_p} \tag{51}$$

$$\omega_{z2} = \frac{1}{2C_S R_S} \tag{52}$$

The low and high-frequency responses of $A(s)$ are as follows:
For low frequencies ($\omega \to 0$):

$$A(0) \approx -\frac{g_{m1}R_L}{2(1 + g_{m1}R_S)} \tag{53}$$

This represents a constant gain determined by the circuit parameters.
For high frequencies ($\omega \to \infty$):

$$A_{\text{high}}(s) \approx -\frac{g_{m1}}{C_L s} \tag{54}$$

The load capacitance, C_L, can be expressed as a combination of the following capacitances:

$$C_L = C_{GD4} + C_{DB4} + C_{ch} \tag{55}$$

In this calculation, it is assumed that the inverse of the common-gate gain

of transistor $M4$ is significantly less than 1, thus allowing the full effect of these capacitances to be considered at the load. Here, C_{ch} represents the capacitance introduced by the MZM channel.

Some considerations are important in this design. First, the degeneration resistances R_S must be relatively small, ideally much less than $R_L/2$, to ensure that the low-frequency gain is sufficient to meet the overall gain specification. Additionally, excessively large R_S values could introduce a significant voltage drop, potentially driving the current source out of saturation. Furthermore, power consumption must also be allocated within this block to achieve the required output swing.

Table 11: Key design equations for the MZM Driver design

Parameter	**Equation**
Output Swing ($V_{\text{pp,d}}$)	$V_{\text{pp,d}} = 2 \cdot I_{SS} \cdot \dfrac{R_L}{2} = I_{SS} \cdot R_L$
Power Consumption ($\text{Power}_{\text{CML}}$)	$\text{Power}_{\text{CML}} = \left(\dfrac{V_{\text{pp,d}}}{2} + V_{\text{out,min}}\right) \cdot \dfrac{V_{\text{pp,d}}}{R_L}$
Zero Frequencies (ω_{z1}, ω_{z2})	$\omega_{z1} = \dfrac{R_L}{L_p}, \quad \omega_{z2} = \dfrac{1}{2C_S R_S}$
Low-Frequency Gain ($A(0)$)	$-\dfrac{g_{m1} R_L}{2(1 + g_{m1} R_S)}$
High-Frequency Gain ($A_{\text{high}}(s)$)	$-\dfrac{g_{m1}}{C_L s}$
Load Capacitance (C_L)	$C_{GD4} + C_{DB4} + C_{ch}$

Table 12: Design considerations for the MZM Driver

Consideration	**Description**
Output Resistance Matching	The output resistance R_{out} must match the load resistance R_L for proper matching with the MZM load ($R_{out} = R_L = 50\,\Omega$).
Bias Voltage V_{B2}	V_{B2} must be chosen to keep transistors in saturation while maintaining the desired output swing.
Degeneration Resistance R_S	R_S is added to reduce input capacitance, extend the bandwidth and increase linearity; it must be relatively small, ideally $R_S \ll R_L/2$ to maintain good gain parameters and not take the current source out of saturation.
Symmetric Arrangement	Symmetric arrangement of inductor and capacitor minimizes circuit area and ensures balanced influence on both branches.
Bulk Connection	Use of isolated well in the bulk to eliminate body effect in V_{TH}, increasing g_m and overall gain.
Power Consumption Allocation	High power consumption must be allocated to achieve the required output swing.

Table 13: Design trade-offs for the MZM Driver design

Parameter	**Increasing Value**	**Decreasing Value**
Degeneration Resistance R_S	Reduces input capacitance; Increases linearity; Decreases low-frequency gain; May introduce voltage drop affecting current source saturation.	Increases input capacitance; Decreases linearity; Increases low-frequency gain; Less voltage drop, ensuring current source remains in saturation.
Capacitor C_S (in parallel with R_S)	Enhances bandwidth via capacitive degeneration peaking; Takes design area.	Reduces peaking effect; Bandwidth may be limited; Reduces design area.
Inductor L_p	Extends bandwidth through shunt-inductive peaking; Can cause overshoot or peaking in time-domain response; Increases circuit area.	Reduces peaking effect; Bandwidth may be limited; Simplifies circuit design and reduces area.
Transconduc. g_{m1}	Improves low-frequency gain; Increase parasitic capacitances; Lowers bandwidth.	Decreases gain; Reduces parasitic capacitances; Enhances bandwidth.
Bias Current I_{SS}	Increases output swing; Increases power consumption; Increases gain	Decreases output swing; Reduces power consumption; Decreases gain
Output Swing $V_{\mathbf{pp,d}}$	Improves signal ; Requires higher I_{SS}; Increases power consumption.	Worsens signal; Allows lower I_{SS}; Decreases power consumption.

3.4 Design of the programmable continuous-time linear equalizer

The circuits that comprise the programmable CTLE were discussed in Sections 2.4.2 and 2.4.3. Little is changed in comparison to the circuits previously analyzed. As in other stages, the bulk well of the transistors is connected to the source in order to increase gain.

Several considerations should be made for this design. First, the resistance $R_{L,\text{ctle}}$, together with the operating currents, biases the stages cascaded with the CTLE, so a sufficient voltage is needed to maintain saturation of the transistors in the following stages. Additionally, the bias voltage V_{B3} must be high enough to ensure that the switching and transconductance transistors remain in their proper operating region.

The peaking behavior, as covered in the theoretical background sections, depends on $R_{L,\text{ctle}}$ and $R_{S,\text{ctle}}$, as does the gain. However, the biasing requirement for the subsequent stages also relies on the voltage drop across $R_{L,\text{ctle}}$. One approach to address this is to use a lower current, which opens up a wider range

for resistance values and allows for better control of the peaking.

To mitigate DC gain variation, larger widths for the transconductance transistors can be employed. This comes with a trade-off of reduced bandwidth due to increased parasitics because a larger transistor width reduces the variation required in V_S to maintain the transistor's fixed current.

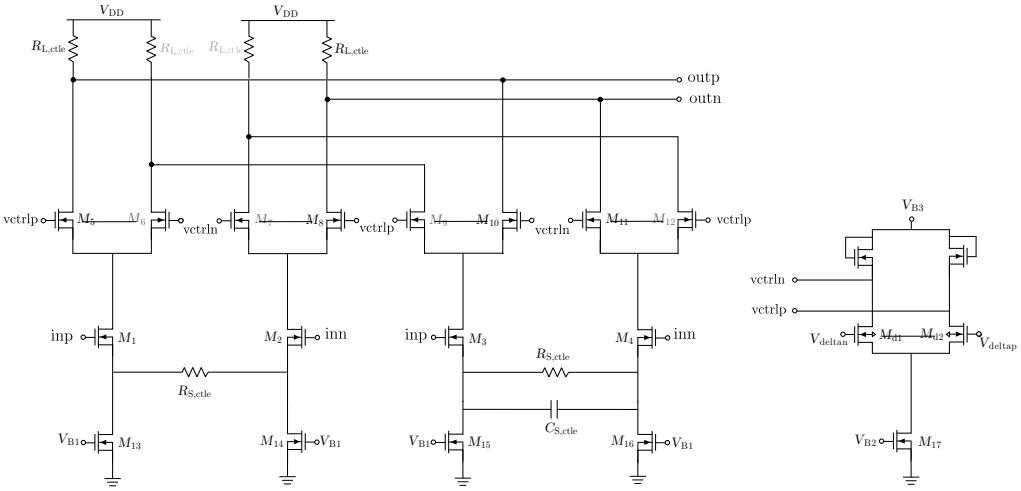

Figure 28: Programmable CTLE circuit design

Source: Author

The equations that parameterize this block are the same as shown previously, namely equations 15, 16, 17, 18, 19, 22 and 21.

Table 14: Key design equations for the Programmable CTLE design

Parameter	**Equation**
Frequency Response without Zero ($H_f(s)$)	$H_f(s) = A_{\text{DC}} \cdot \dfrac{1}{(1 + s/\omega_{pl}) + (1 + s/\omega_{pc})}$
Frequency Response with Zero ($H_p(s)$)	$H_p(s) = A_{\text{DC}} \cdot \dfrac{1 + s/\omega_z}{(1 + s/\omega_{pl}) + (1 + s/\omega_{pc})}$
Low-Frequency Pole (ω_{pl})	$\omega_{pl} = \dfrac{1}{C_L R_L}$
High-Frequency Pole (ω_{pc})	$\omega_{pc} \approx \dfrac{g_{m5}}{C1}$
Zero Frequency (ω_z)	$\omega_z = \dfrac{1}{C_S R_S}$
DC Gain (A_{DC})	$A_{\text{DC}} = \dfrac{g_{m1} R_L}{1 + \dfrac{g_{m1} R_S}{2}}$
Load Capacitance (C_L)	$C_L = C_{DB5} + C_{GD5} + C_{\text{in,buff}}$
Total Capacitance (C_1)	$C_1 = 2C_{GD1} + C_{DB1} + C_{GS5}$

Table 15: Design considerations for the Programmable CTLE

Consideration	**Description**
Bulk Connection	The bulk well of the transistors is connected to eliminate the body effect, increasing g_m and overall gain.
Load Resistance $R_{L,\mathbf{ctle}}$	Must provide sufficient voltage drop to maintain saturation in subsequent stages; impacts gain and peaking behavior.
Bias Voltage V_{B3}	Must be high enough to keep switching and transconductance transistors in their proper operating region (saturation).
Operating Current	Using a lower current widens the range of viable resistance values, aiding in peaking control and biasing requirements.
Transistor Width (Sizing)	Larger widths for transconductance transistors mitigate DC gain variation but increase parasitic capacitances, potentially reducing bandwidth.
Voltage Drop Across $R_{L,\mathbf{ctle}}$	Must be sufficient to bias subsequent stages while avoiding excessive voltage drops that could limit the output swing.
Consistency with other Stages	Design choices should ensure compatibility with other stages to maintain system functionality.

Table 16: Design trade-offs for the Programmable CTLE design

When $\omega_{p1} < \omega_{p2}$		
Parameter	**Increasing Value**	**Decreasing Value**
Load Resistance R_L	Increases DC gain (A_{DC}); Increases peak gain (A_{pk}); Decreases peak frequency (ω_{p1}); May reduce bandwidth.	Decreases A_{DC} and A_{pk}; Increases ω_{p1}; Enhances bandwidth.
Source Resistance R_S	Reduces A_{DC}; No change to A_{pk}; No change to ω_{p1}; Improves linearity.	Increases A_{DC}; Potentially reduces linearity; No change to A_{pk} or ω_{p1}.
Source Capacitance C_S	No change to A_{DC}; Increases A_{pk}; No change to ω_{p1}; May introduce peaking in response.	No change to A_{DC}; Decreases A_{pk}; Simplifies frequency response.
When $\omega_{p2} < \omega_{p1}$		
Load Resistance R_L	Increases A_{DC} and A_{pk}; No change to peak frequency ω_{p2}; May affect biasing of subsequent stages.	Decreases A_{DC} and A_{pk}; No change to ω_{p2}; Easier biasing conditions.
Source Resistance R_S	Reduces A_{DC} and A_{pk}; Reduces ω_{p2}; Enhances linearity; May reduce bandwidth.	Increases A_{DC} and A_{pk}; Increases ω_{p2}; Potentially reduces linearity; Enhances bandwidth.
Source Capacitance C_S	No change to A_{DC}; Increases A_{pk}; Reduces ω_{p2};	No change to A_{DC}; Decreases A_{pk}; Increases ω_{p2};

3.5 Design methodology

The design methodology of this project is based on setting initial values for device parameters and transistor dimensions in each block, guided by the equations and design considerations previously discussed. From these initial values, iterative adjustments are made, considering trade-offs to achieve the target specifications.

The design environment used for this project was Synopsys software, specifically the Custom Compiler Design Environment for schematic design and PrimeSim for performing simulations.

Table 17: Main design parameters affecting each specification - All blocks

Spec.	**Input Buff**	**Interstage Buff**	**Program. CTLE**	**CML Driver**
Bandwidth	g_{m1}, L_p, $R_{S,\text{buff}}$	g_{m1}, $R_{S,\text{buff}}$, W	C_S, R_S, R_L, C_L	R_S, C_S, L_p
Output Swing	-	-	-	I_{SS}, R_L
THD	$R_{S,\text{buff}}$, g_{m1}	$R_{S,\text{buff}}$, g_{m1}	g_{m1}, R_S	R_S, g_{m1}, I_{SS}
Voltage Gain	g_{m1}, $R_{S,\text{buff}}$	g_{m1}, $R_{S,\text{buff}}$	R_L, g_{m1}, R_S	g_{m1}, R_S
CTLE Peaking Gain	L_p	-	C_S, R_L, C_L, R_S	-
CTLE DC Gain Variation	-	-	W, I_{D1}	-

The design process leverages this table along with other tables detailing design considerations and trade-offs specific to each circuit block. Since all blocks are interconnected to form a comprehensive design, it is essential to understand the implications of adjustments in one block on the others and to adapt accordingly, making it hard to achieve a good systematic functionality by only theoretical analysis of each block. By conducting simulations and systematically varying specific parameters within each circuit, the design can be tuned to meet the desired specifications. This iterative process relies on a foundation of intuition and logic, informed by the analyses presented throughout this work.

The dimensions and values achieved for each device, as referenced in Figures 22, 24, 26, and 28, are presented in Table 18 for clarity. All the devices utilized in this project, including capacitors and inductors, are from 65nm technology. Additionally, this table does not list all transistor sizes, as other transistors are matched to the dimensions of those shown.

Table 18: Transistor dimensions and component values for each circuit block.

Component	**Input Buffer**	**Interstage Buffer**	**CML Driver**	**CTLE**
Transistor Dimensions	M1: W = 252u, L = 60n M2: W = 160u, L = 60n M3: W = 216u, L = 60n M4: W = 180u, L = 0.24u	M1: W = 75u, L = 60n M2: W = 152u, L = 60n M4: W = 144u, L = 0.24u	M1: W = 396u, L = 60n M3: W = 480u, L = 0.24u M4: W = 144u, L = 60n	M1: W = 44.8u, L = 60n M5: W = 30u, L = 60n M13: W = 180u, L = 0.24u
Resistances (Ω)	-	Rsb = 18	RL = 50 Rs = 5	RL = 125 Rs = 72
Capacitances (F)	-	-	Cs = 0.45p	Cs = 0.35p
Inductances (H)	Lp = 0.367n	-	Lp = 0.96n	-

3.6 Simulation results

For the simulations, since the design operates at high frequencies, capacitances were added at the circuit nodes to simulate parasitic capacitances. An arbitrary value of 10 fF was used for most nodes, while a larger capacitance of 50 fF was considered for the input and output nodes. This approach is relevant because, for this project, no layout was created to allow for extraction that would account for these parasitic elements.

3.6.1 Frequency response

The frequency response of each circuit block was simulated. Since the overall system operation depends on the performance of each block, the design choices, such as zero placement and gain distribution, were made to minimize power consumption in specific blocks while respecting trade-offs and constraints, including inter-stage biasing.

In Figure 29, the frequency responses of the flat-band CTLE, the input buffer, and their combination are shown. It can be observed that the zero is chosen to maintain a peaking effect in this combined response, compensating for the poles in subsequent circuits. Additionally, part of the overall gain is contributed by this circuit combination.

Figure 30 shows the frequency response of the CML driver and the interstage buffer. As the interstage buffer is situated between the operational stages of the MZM driver, it experiences the greatest impact from parasitic capacitances. The

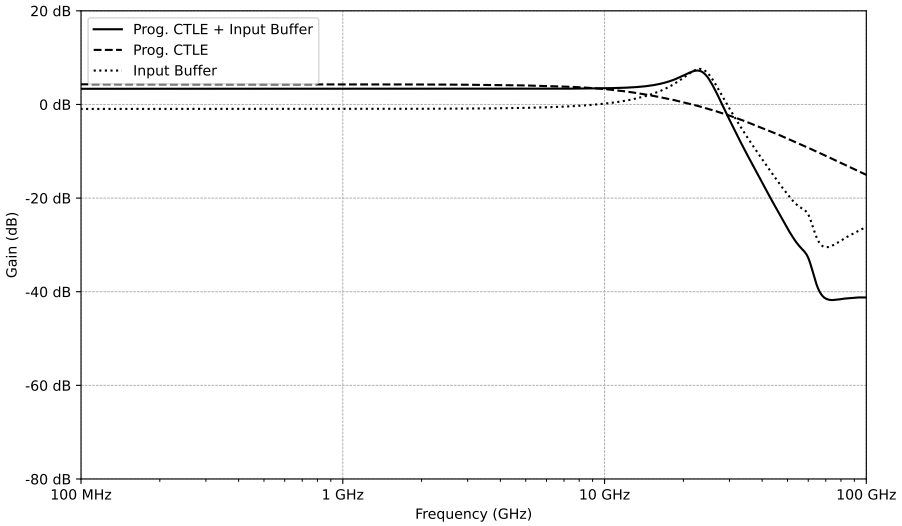

Figure 29: Combination of CTLE and Input Buffer frequency response

Source: Author

zeros created in the CML driver block help to compensate for the high-frequency attenuation caused by these parasitic capacitances.

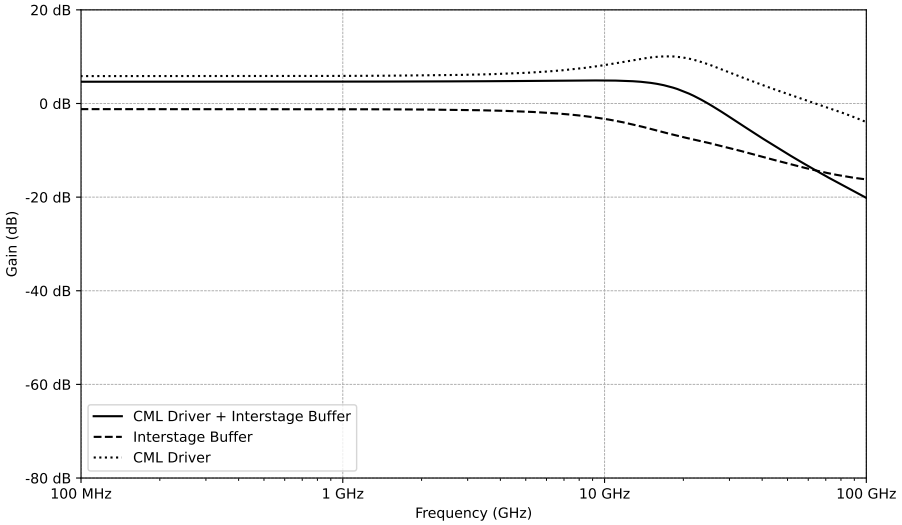

Figure 30: Combination of CML Driver and Interstage Buffer frequency response

Source: Author

Figure 31 shows the final frequency response of the MZM driver, created by combining the responses of all blocks. It can be noted that the peaking effect maintained in the CTLE and input buffer combination contributes to the required bandwidth, compensating for the responses of the remaining stages.

Finally, Figure 32 shows the isolated frequency response of the complete

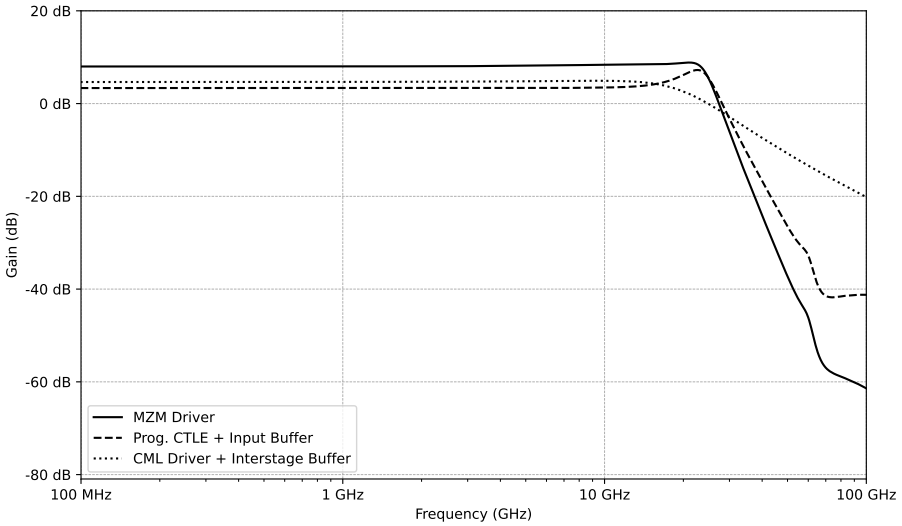

Figure 31: Combination of all blocks frequency responses

Source: Author

MZM driver, highlighting key parameters such as DC gain, -3dB frequency (circuit bandwidth), and peaking observed at high frequencies. In the flat-band configuration, the driver achieves a voltage gain of 8 dB, a bandwidth of 25.2 GHz, and a high-frequency peaking of 8.85 dB, all meeting the specified design requirements.

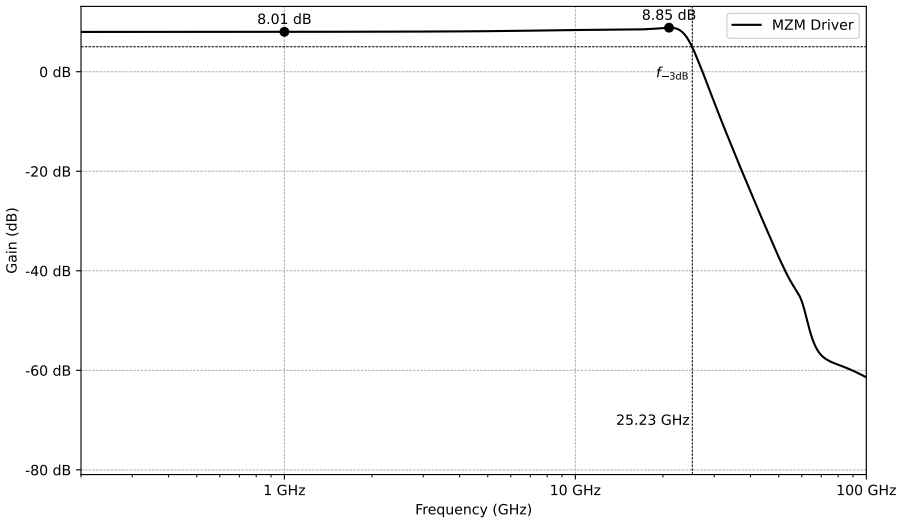

Figure 32: Complete MZM Driver frequency response

Source: Author

Another important metric is the group delay. The group delay (τ_g) represents the rate of change of the signal phase with respect to the angular frequency (ω),

mathematically defined as the derivative of the phase ($\phi(\omega)$) with respect to frequency: $\tau_g = -\frac{d\phi(\omega)}{d\omega}$. A constant group delay implies that all frequency components of a signal travel at the same speed, preserving the signal shape over time. Therefore, examining the variation in group delay across different frequencies is important for assessing this parameter's quality, this metric can be seen in figure 33.

The maximum group delay occurs at 23.1 GHz, near the frequency where peaking is concentrated. Since most of the frequency components of PAM4 signals are at lower frequencies, this maximum variation of 25 ps is not critical, as most signal components are unaffected by this higher delay. The variation of less than 4.81 ps between 1 GHz and 10 GHz is more relevant for evaluating this parameter. However, because there is no direct mapping between group delay, eye diagram, and bit error rate, a more cohesive approach to evaluate the project's performance would be to observe the PAM4 eye diagram at the output.

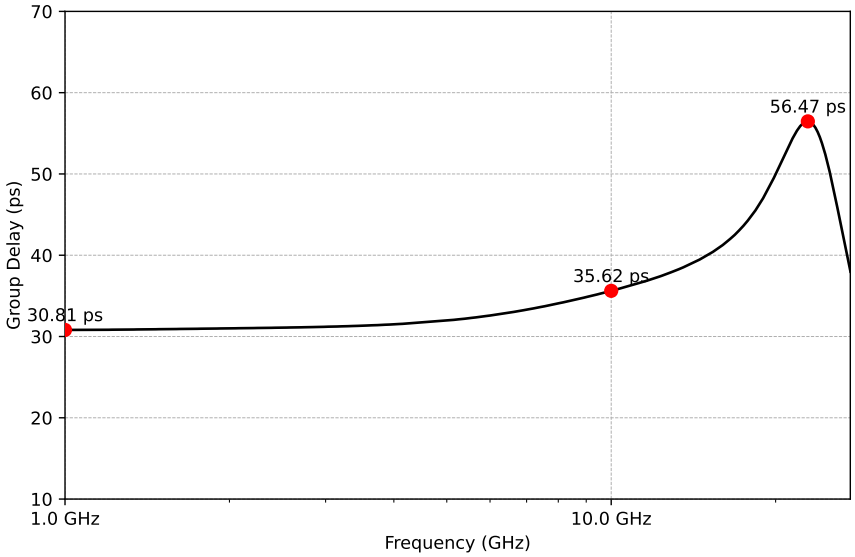

Figure 33: MZM Driver group delay

Source: Author

3.6.2 CTLE results

The results of the CTLE circuit can be observed in the figures below. Figure 34 shows the peaking behavior of the CTLE frequency response. A peaking variation is observed, concentrated around the frequency of 23 GHz, which is the specified operating frequency of the circuit.

Within the complete frequency response of the driver, illustrated in Figure 35, the peaking variation also remains concentrated at the frequency of interest and assumes different values. This allows for the utilization of multiple channels in the circuit load.

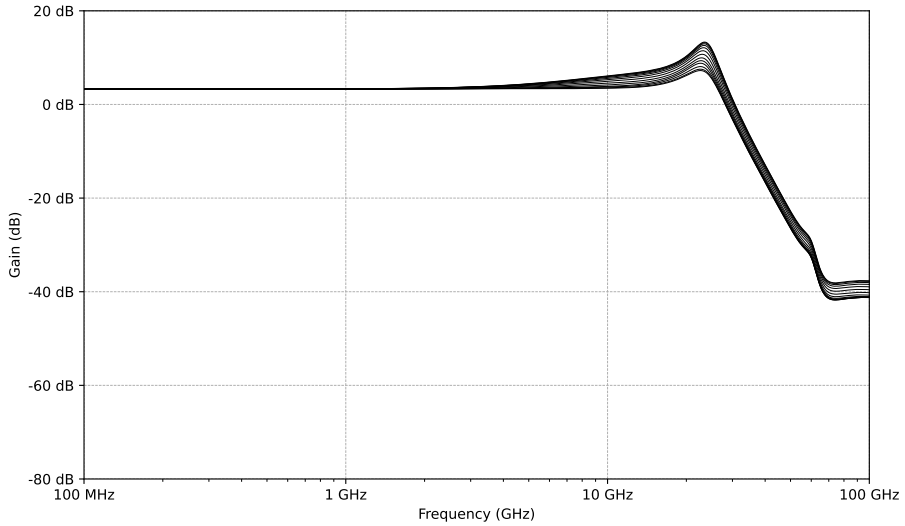

Figure 34: Peaking tuning on CTLE frequency response

Source: Author

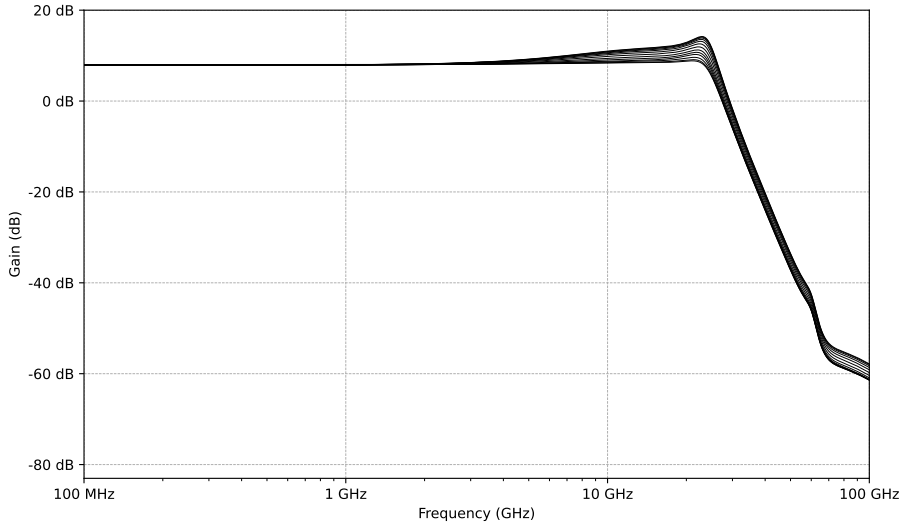

Figure 35: Peaking tuning on MZM Driver frequency response

Source: Author

Figures 36 and 37, represent the graphs of relevant parameter variations during CTLE peaking adjustments as a function of the control signal. In terms of DC gain variation, a maximum variation of 0.15 dB was achieved, which is within the specified limits.

Additionally, a peaking range between 0.86 dB (observed during flat operation of the circuit) and 6.29 dB was achieved, also meeting the specified requirements.

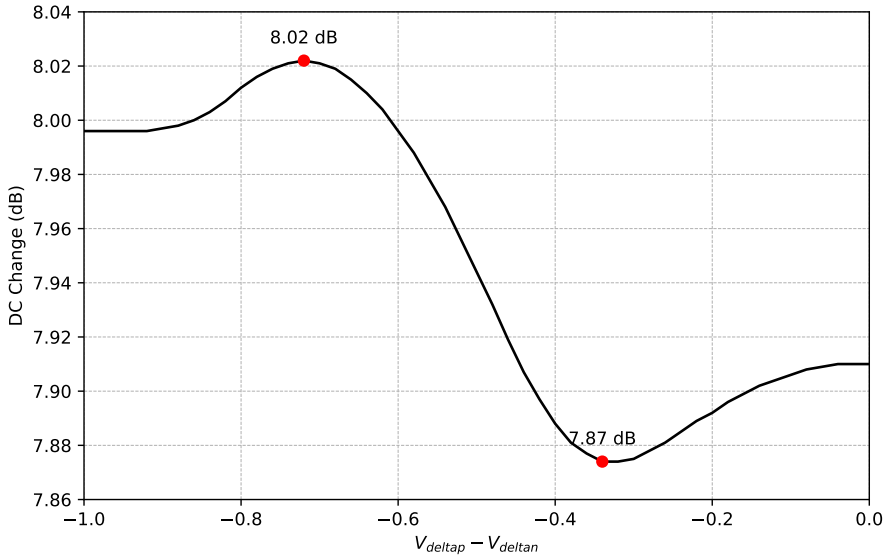

Figure 36: CTLE DC gain change from peaking variation

Source: Author

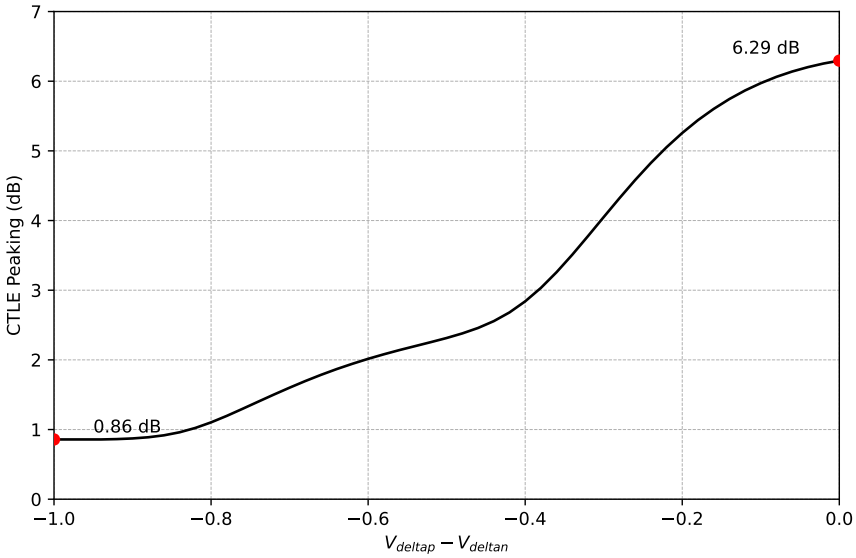

Figure 37: CTLE peaking value change

Source: Author

3.6.3 Distortion

For distortion measurement, the lowest frequency component of the PAM4 signal, approximately 150 MHz, is used. This is because the lower frequency component is more affected by harmonic distortions, as there are more fundamental multiples within the operating bandwidth of the circuit. For the THD measurement, an

input sine wave at 150 MHz was utilized to achieve the circuit's maximum output swing, approximately 2.2 V, pushing the circuit to its maximum stress margin. Figure 38 shows the output sine wave of the circuit overlaid with the input sine wave.

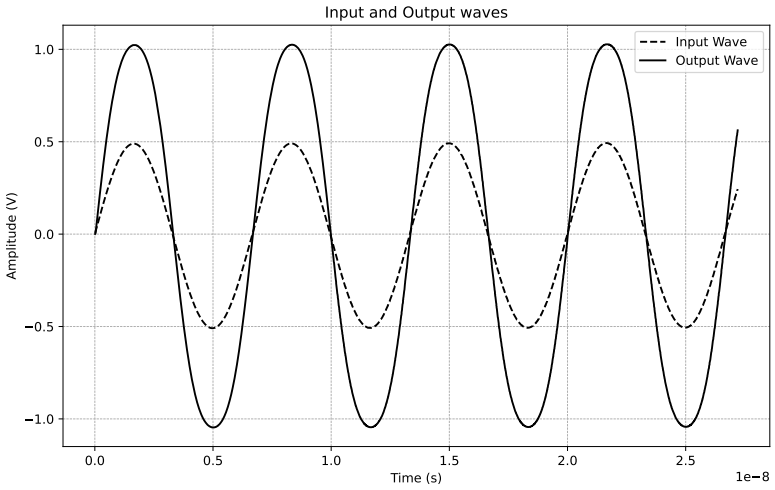

Figure 38: Input vs Output sine wave

Source: Author

Figure 39 shows the harmonics of the circuit's output sine wave, demonstrating distortion through the presence of non-fundamental harmonics. Note that the Y-axis of this figure is in a logarithmic scale for better visualization of the harmonics.

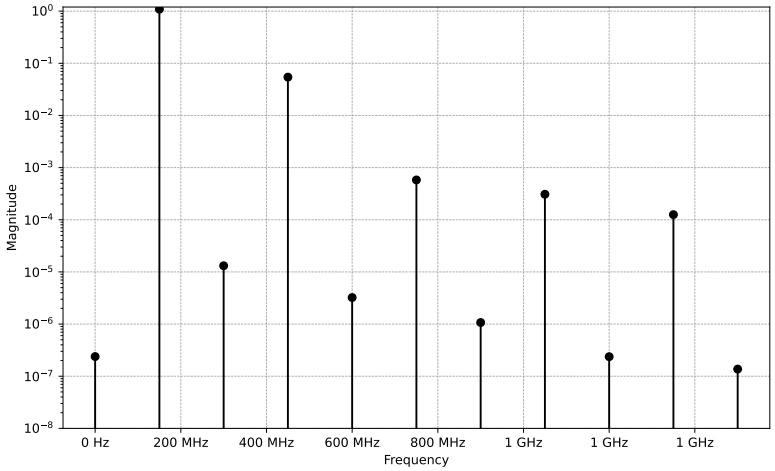

Figure 39: THD: Harmonic values

Source: Author

The total distortion, calculated via software, results in a THD of 5%, which

meets the project specifications. This is particularly noteworthy given that this is the maximum distortion measurement achievable in simulation.

3.6.4 Transient operation

To evaluate the driver's operation, considering the transmission speed requirements of 28 Gbaud or 56 Gb/s, a PAM4 signal with these characteristics was applied to the circuit's input, and the eye diagram of this signal was measured at the output.

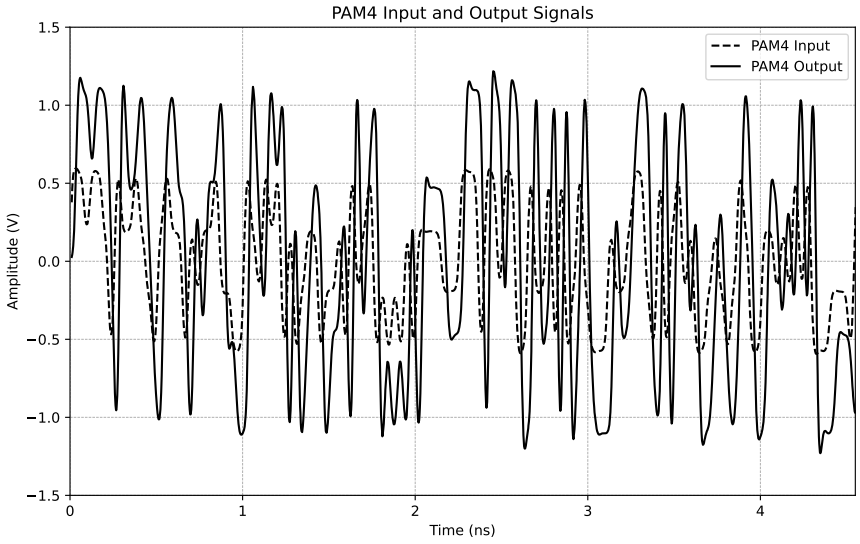

Figure 40: Input and Output PAM4 signals

Source: Author

Figure 40 shows the PAM4 signal at the input and output of the circuit. It is observed that the waveforms maintain a good shape, with the differential output swing reaching 2.2 V.

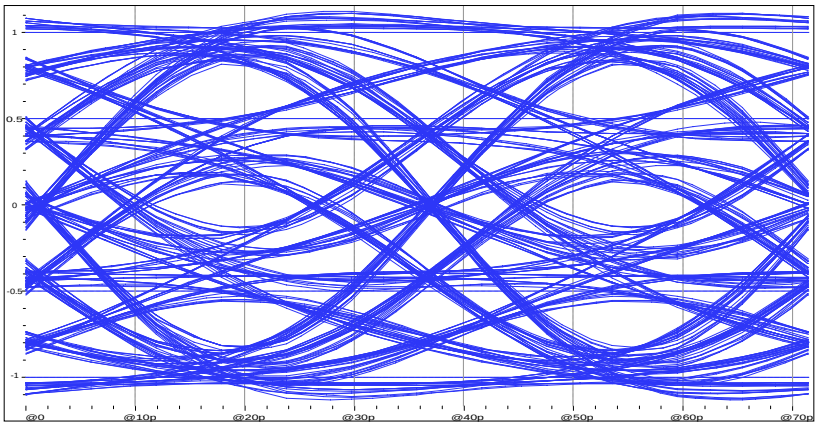

Figure 41: Output signal PAM4 eye diagram

Source: Author

By overlaying all waveform transitions, the eye diagram shown in Figure 41 is obtained. The eye diagram demonstrates a clear eye opening, indicating effective signal transmission.

The eye width is 14.43 ps, and the eye height is 288 mV, which in conjunction with Fig 41 characterize a well defined eye morphology. The measurement of eye width and height are done using the central eye as reference.

3.6.5 S-Parameters

The S-parameters, or scattering parameters, are fundamental in the analysis of high-frequency circuits, as they describe how signals propagate between ports of a circuit, particularly in high-frequency ranges where reflection and loss effects are predominant.

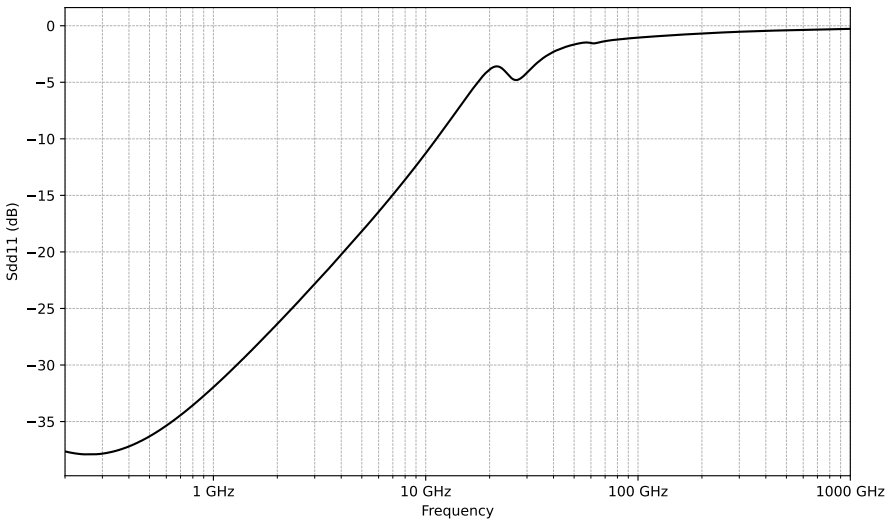

Figure 42: SDD11 scattering parameter

Source: Author

SDD11 represents the input reflection coefficient, indicating how much of the signal is reflected back to the source at the input port, and it is essential for assessing impedance matching and minimizing losses. As shown in Figure 42, the circuit exhibits low reflection, which starts to become more prominent at higher frequencies, reaching up to approximately -5 dB at the maximum operating frequencies of the circuit. This happens because of the parasitic reactances present at the input of the circuit.

SDD12, shown in Figure 43, represents the reverse isolation between the input and output ports, quantifying the degree to which the output signal can influence the input signal. This is an important metric for circuit stability. Low dB values were found for this parameter, indicating excellent isolation between the input and output.

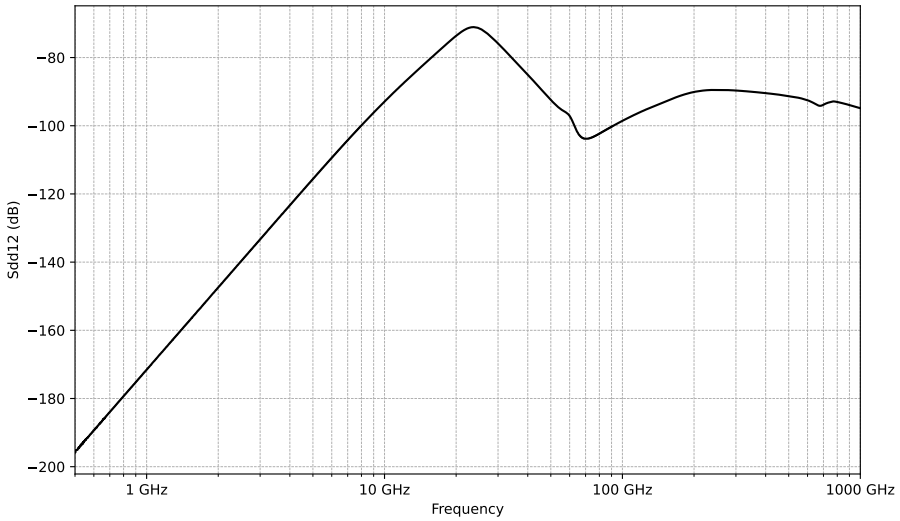

Figure 43: SDD12 scattering parameter

Source: Author

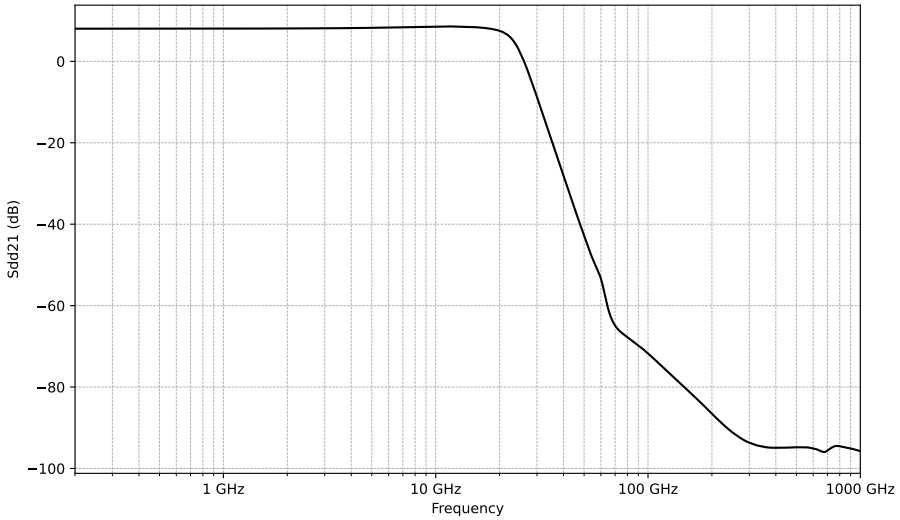

Figure 44: SDD21 scattering parameter

Source: Author

SDD21 is the transmission gain, showing the amount of input signal transmitted to the output port. As seen in Figure 44, this parameter aligns with the AC gain of the circuit, as expected.

Finally, SDD22 is the output reflection coefficient, similar to SDD11 but applied to the output port. This parameter is critical to ensure that the output signal is transmitted adequately without reflections that could impact the overall performance of the circuit. As shown in Figure 45, it provides a low reflection

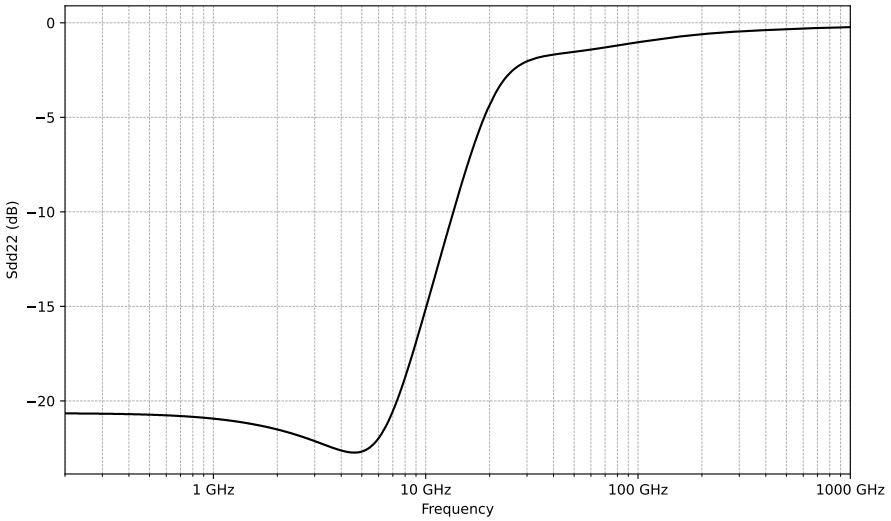

Figure 45: SDD22 scattering parameter

Source: Author

coefficient, which increases as it approaches the maximum operating frequencies, reaching approximately -3 dB. This manly happens because in the output we had to add an inductance to achieve the desired bandwidth, which changes the output impedance in higher frequencies.

3.6.6 CMRR and PSRR

The PSRR (Power Supply Rejection Ratio) and CMRR (Common-Mode Rejection Ratio) are important parameters as they help ensure signal integrity and immunity to external interference. The PSRR measures the circuit's ability to reject voltage variations in the power supply, preventing unwanted interference in the supply from being amplified and impacting the output signal. The CMRR, in turn, measures the circuit's ability to reject common-mode signals, such as noise equally picked up at the inputs of a differential amplifier, preserving the quality of the differential signal. Together, PSRR and CMRR are fundamental to achieving high precision and fidelity in high-frequency circuits, minimizing noise and interference.

Figures 46 and 47 show both high PSRR and CMRR, thus providing good rejection at least within the operating frequency range (up to 25GHz). Note that this was a single measurement taken from the

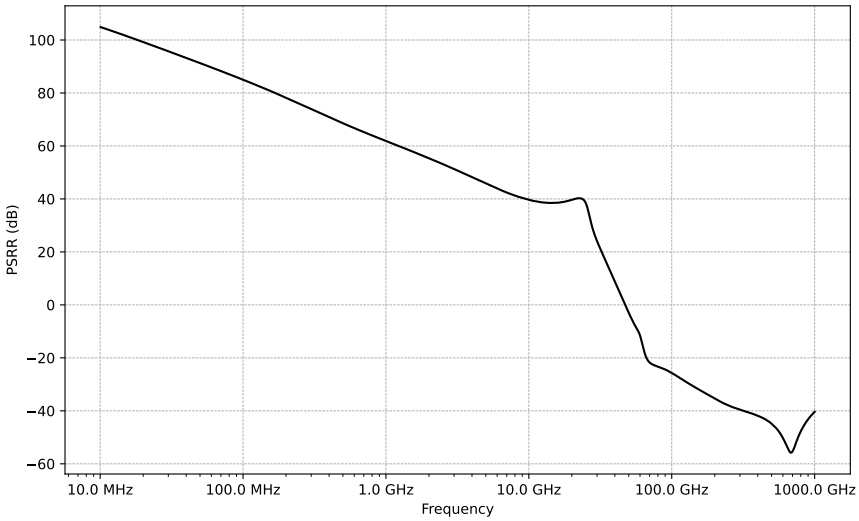

Figure 46: MZM Driver PSRR

Source: Author

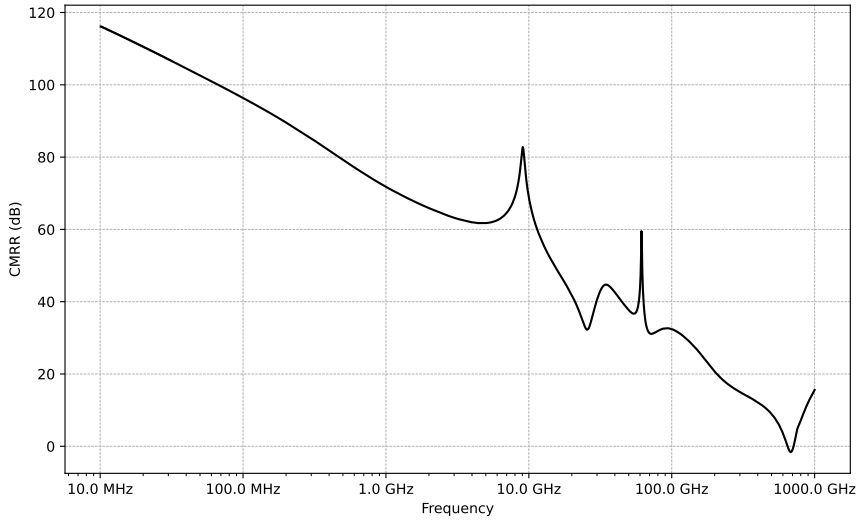

Figure 47: MZM Driver CMRR

Source: Author

3.6.7 Input and output noise

The input and output-referenced noise are critical parameters in high-frequency circuit analysis, as they allow for a detailed understanding of how noise impacts circuit performance. These measurements represent the extent to which internally generated noise by the circuit's components is amplified or transferred to the input or output signals.

From Figure 48, we observe favorable input noise results, showing low noise

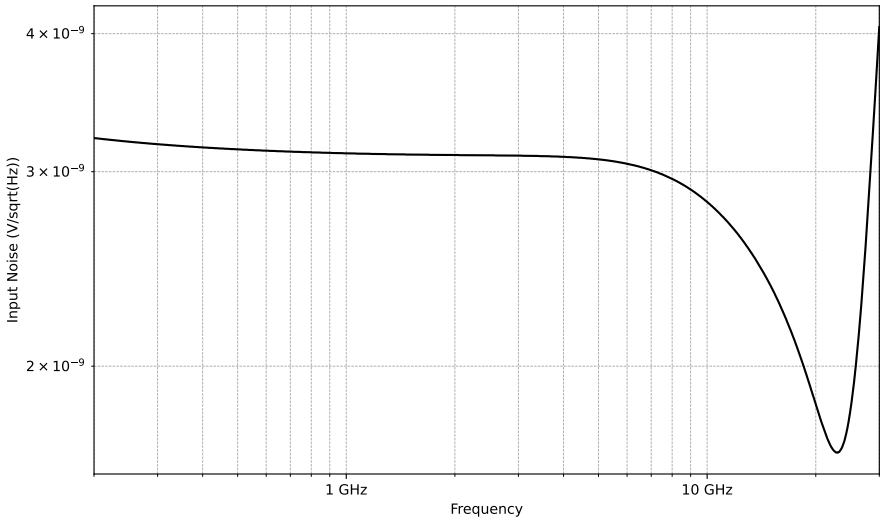

Figure 48: Input noise against frequency

Source: Author

spectral density values, particularly in the higher frequency ranges of interest. The plot demonstrates that, for most frequencies, the noise level remains around $3 \cdot 10^{-9}\,\mathrm{V}/\sqrt{\mathrm{Hz}}$.

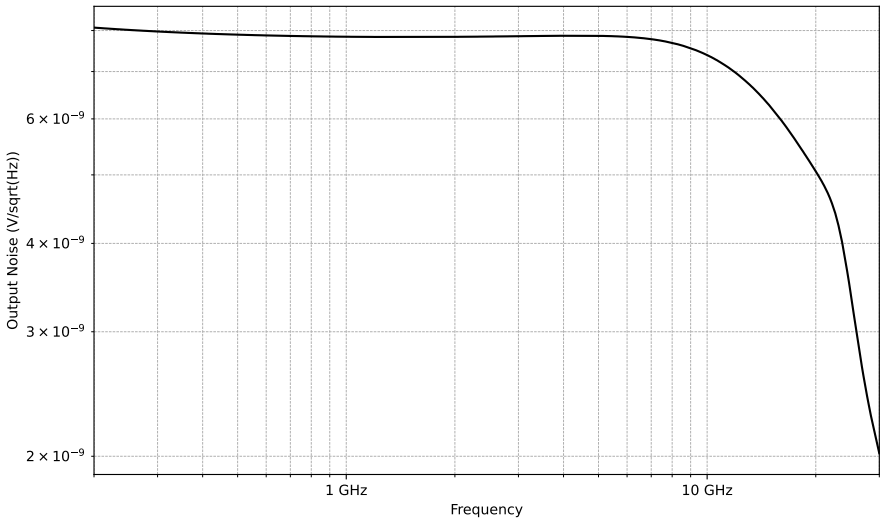

Figure 49: Output noise against frequency

Source: Author

The output noise result is also favorable, displaying low noise spectral density across the analyzed frequency range. The graph shows that, for most frequencies, the noise level is around $8 \cdot 10^{-9}\,\mathrm{V}/\sqrt{\mathrm{Hz}}$, which is reasonable, especially given the output signal's magnitude.

3.6.8 Process variation and mismatch

To evaluate the robustness of the circuit under process variations and component mismatch, a Monte Carlo analysis was conducted with these two conditions imposed within the schematic.

The -3dB bandwidth of the circuit remained within specifications for all simulated variations.

Similarly, the DC gain remained within expected ranges under process and mismatch variations.

The THD value, measured at maximum $V_{\mathrm{pp,d}}$, stayed within an acceptable range, although some values approached the threshold of the specification.

The power consumption of the circuit also remained below the maximum specification across all Monte Carlo simulations.

Finally, the eye diagram quality metrics remained stable across simulation conditions, demonstrating adequate performance.

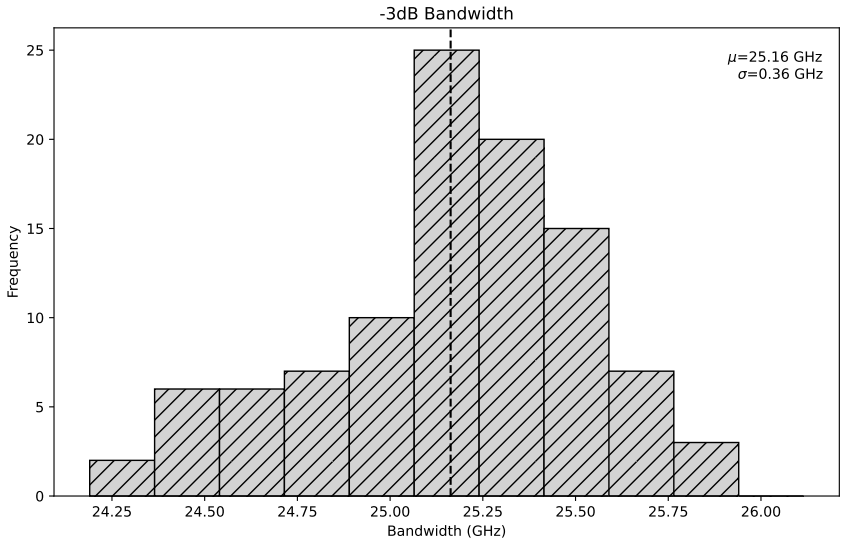

Figure 50: -3dB Bandwidth histogram of process and mismatch variation via Monte Carlo

Source: Author

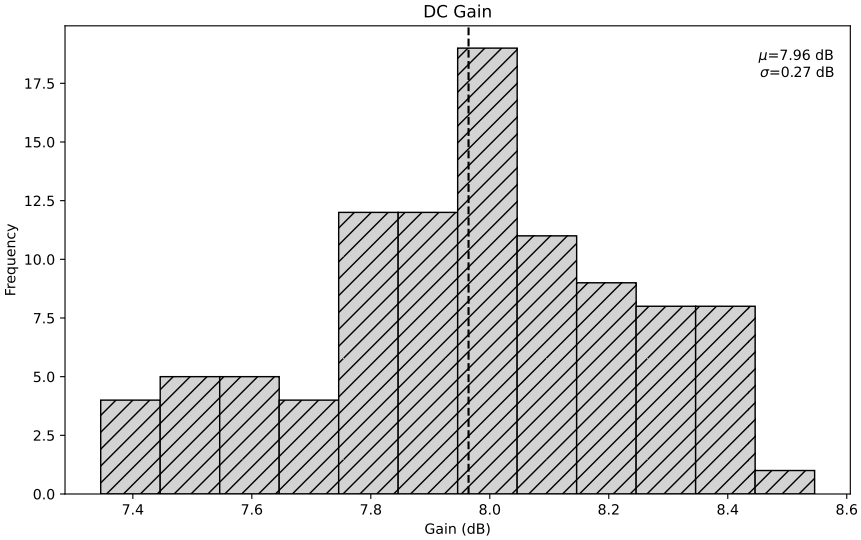

Figure 51: DC gain histogram of process and mismatch variation via Monte Carlo

Source: Author

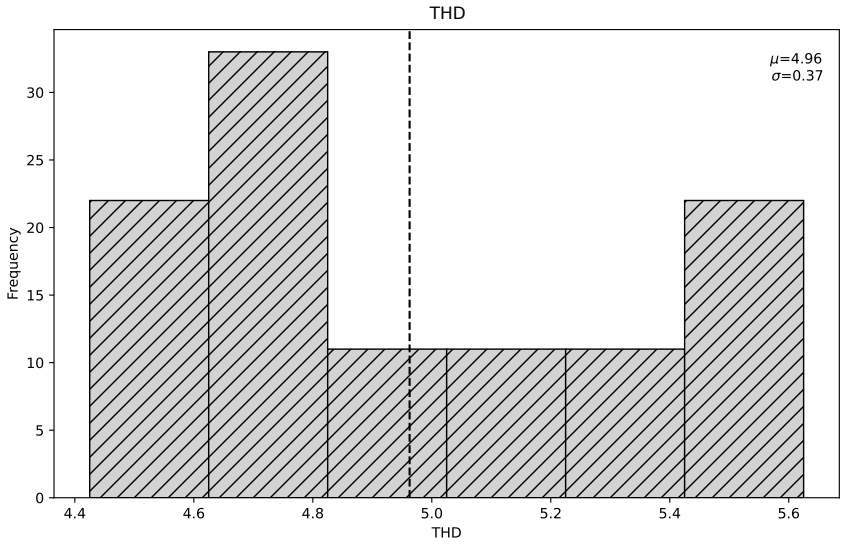

Figure 52: THD histogram of process and mismatch variation via Monte Carlo

Source: Author

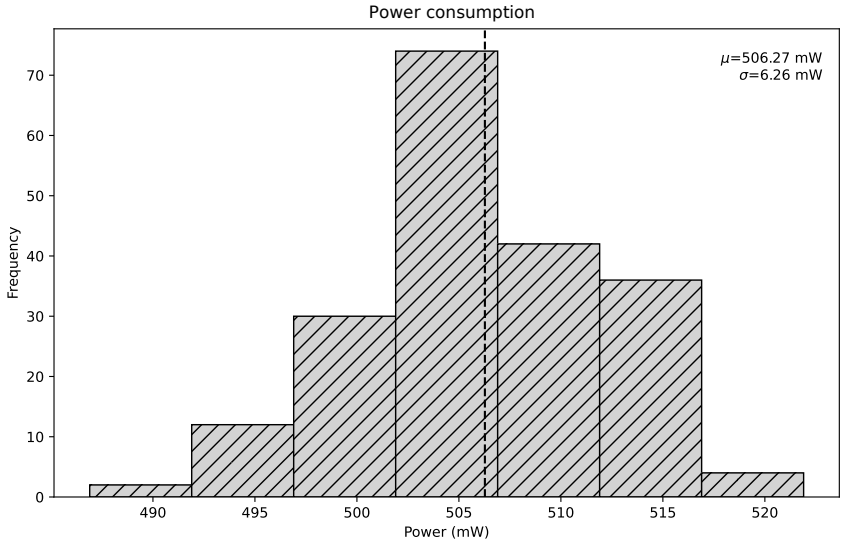

Figure 53: Power consumption histogram of process and mismatch variation via Monte Carlo

Source: Author

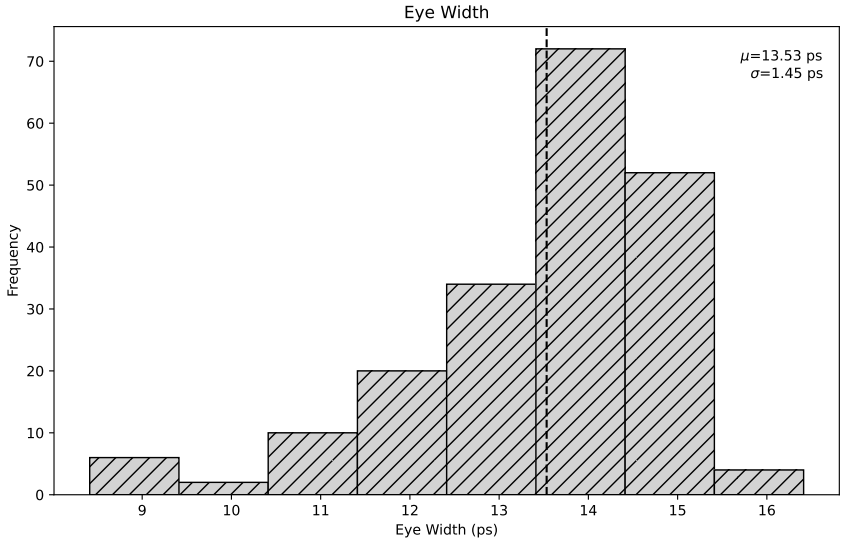

Figure 54: Eye width histogram of process and mismatch variation via Monte Carlo

Source: Author

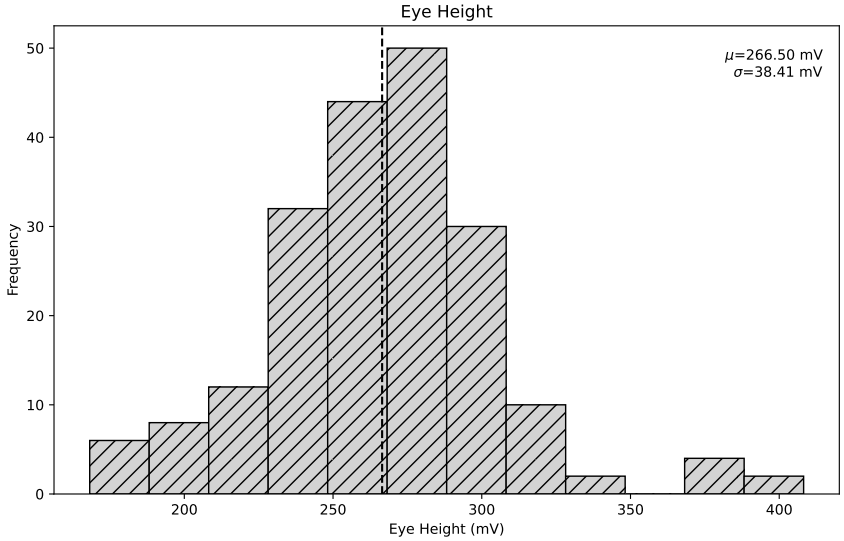

Figure 55: Eye height histogram of process and mismatch variation via Monte Carlo

Source: Author

3.6.9 Temperature variation

For temperature variation analysis, a current source with a Proportional To Absolute Temperature (PTAT) characteristic and a variation rate of 3500 ppm/ºC was used, as illustrated in Figure 56. The purpose of a PTAT source in this circuit is to counteract the unwanted effects inherited by the MOSFETs in higher temperatures by adding more current to the circuit.

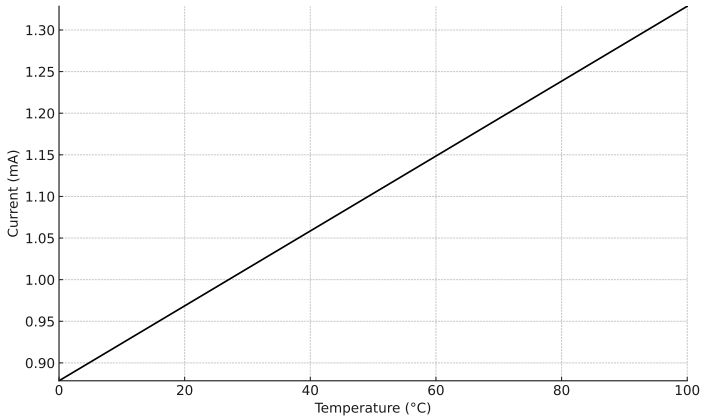

Figure 56: Reference current source (mA) vs Temperature

Source: Author

Some parameters, such as THD and gain, approach the specification limits at temperatures of 0°C and 100°C. However, the circuit remains functional and

Table 19: Parameter Variation as a Function of Temperature

Parameter	**0°C**	**27°C**	**60°C**	**100°C**
Bandwidth (GHz)	25.7	25.2	24.7	24.7
Gain (dB)	8.4	8.0	7.4	6.5
Eye Height (V)	0.285	0.288	0.234	0.200
Eye Width (ps)	14.16	14.43	13.38	13.53
Power Consumption (mW)	462	506	552	589
THD (%)	5.98	5.00	5.43	5.96

within acceptable performance at all tested temperatures, comfortably meeting the 60°C corner.

3.6.10 Compliance table and state of the art comparation

With the simulations completed, a compliance table can be generated to compare the measured results with the project specifications, verifying whether all requirements have been met. Additionally, these values can be contrasted with those presented in state-of-the-art reference articles to assess relative performance and design advancements.

Parameter	**Specification**	**Measured Value**	**Compliance**
Modulation Format	PAM4	PAM4	Yes
Minimum Bandwidth (GHz)	23	25.2	Yes
Minimum Output Swing (Vpp,d)	1.2	2.2	Yes
Maximum THD (%) at Vpp,d	6	5	Yes
Minimum Voltage Gain (dB)	6.5	8	Yes
Maximum DC Power Consumption (mW)	650	506	Yes
Data Rate (Gbaud)	28	28	Yes
Data Rate (Gb/s)	56	56	Yes
Maximum Energy Efficiency (pJ/bit)	11.6	9	Yes
CTLE Min./Max. Peaking Gain (dB)	0 - 6	0.86 - 6.29	Yes
CTLE Maximum Peaking DC Gain Variation (dB)	0.4	0.15	Yes
Temperature Range (ºC)	0 - 60	0 - 100	Yes

Table 20: Compliance table for the MZM driver with programmable equalization.

Table 21: Selected work on high-speed transmitters comparison

Reference	Circuit Topology	Modulation Format	Bandwidth (GHz)	Output Swing ($V_{pp,d}$)	THD (%)	Gain (dB)	Data Rate (Gbaud)	Data Rate (Gb/s)	DC Power (mW)	Energy Efficiency (pJ/b)	Technology	Measurement Scope
[2]	Stacked current-mode, VGA, VEQ	PAM4	32	2	6 (for 2 $V_{pp,d}$)	24	40	80	180	2.25	65nm CMOS	Fabricated
[4]	Stacked current, MZM, GC, EMP, peaking	DP-32QAM	43	1.5	2.2 (for 1.5 $V_{pp,d}$)	13-22.5	64	640	225	1.41	65nm CMOS	Fabricated
[5]	Push-pull CML, MZM, EAM, shunt-peaking	PAM4	17	4	3	3	16	32	201	6.28	65nm CMOS	Fabricated
[3]	Balanced input, single-ended output, tunable pre-emphasis, back-termination	NRZ/PAM4	18	-	-	-	16	32	550	1.075	65nm CMOS	Fabricated
This work	CML driver, MZM load, programmable CTLE	PAM4	25.2	2.2	5	8	28	56	506	9	65nm CMOS	Simulated

4 Conclusion

This work presented the design of a high-speed PAM4 Mach-Zehnder modulator driver for optical communications, implemented using 65nm CMOS technology. Through this design, we explored the trade-offs and interdependencies between essential parameters, such as bandwidth, gain, and linearity, while optimizing for total harmonic distortion (THD), gain, bandwidth and energy efficiency. The design strategy included partitioning the circuit into four core blocks: the input buffer, interstage buffer, CML driver, and programmable CTLE, each contributing uniquely to the overall performance.

A systematic approach to achieving high bandwidth was employed, with the implementation of inductive peaking, capacitive degeneration, cascode topologies and source resistance tuning in each block. The programmable CTLE block was particularly instrumental in controlling the peaking response, allowing fine-tuning of the frequency response to maintain bandwidth across a range of operational conditions. The design also demonstrated the importance of impedance matching, especially between the driver and the Mach-Zehnder modulator (MZM) load, to minimize reflections.

Results showed the circuit achieving a bandwidth of 25 GHz, with a voltage gain of 8 dB with good eye-diagram characteristics. A THD of 5% was measured, meeting the specifications for high-speed optical modulation without excessive distortion. Additionally, the design achieved a power consumption of 506 mW and an energy efficiency of 9 pJ/bit, well within the target specification.

Monte Carlo simulations indicated robust performance across process and mismatch variations, with all key parameters—bandwidth, gain, THD, and power consumption—remaining within acceptable limits. Temperature variations from 0°C to 100°C showed deviations in a few characteristics, notably in gain and THD, yet the driver continued to perform within specification boundaries.

Compared to state-of-the-art designs, this driver offers competitive bandwidth with good output-swing and gain, achieved through a topology which works for different channel loss specifications.

Future work could focus on the complete layout design to capture parasitic effects accurately, further improving the accuracy of simulations and enabling a path to physical implementation. Additionally, exploring an automatic gain control technique for the driver could enhance system sensitivity across varying input levels, potentially improving both linearity and adaptability under dynamic operational conditions.

References

[1] Behzad Razavi. *Design of Integrated Circuits for Optical Communications*. 2nd. Hoboken, NJ, USA: John Wiley & Sons, 2012. ISBN: 978-1-118-33694-6.

[2] Shinsuke Nakano et al. "A 2.25-mW/Gb/s 80-Gb/s-PAM4 Linear Driver with a Single Supply using Stacked Current-Mode Architecture in 65-nm CMOS". In: *IEEE Journal of Solid-State Circuits* (2017).

[3] Bozhi Yin et al. "A 32Gb/s-NRZ, 15GBaud/s-PAM4 DFB Laser Driver with Active Back-Termination in 65nm CMOS". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2017).

[4] Teruo Jyo et al. "A 48GHz BW 225mW/ch Linear Driver IC with Stacked Current-Reuse Architecture in 65nm CMOS for Beyond-400Gb/s Coherent Optical Transmitters". In: *IEEE Journal of Solid-State Circuits* (2020).

[5] Jeongho Hwang et al. "A 32 Gb/s, 201 mW, MZM/EAM Cascode Push-Pull CML Driver in 65 nm CMOS". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2017).

[6] Alireza Zandieh, Peter Schvan, and Sorin P. Voinigescu. "Linear Large-Swing Push–Pull SiGe BiCMOS Drivers for Silicon Photonics Modulators". In: *IEEE Transactions on Microwave Theory and Techniques* (2017).

[7] Behnam Analui et al. "A Fully Integrated 20-Gb/s Optoelectronic Transceiver Implemented in a Standard 0.13-µm CMOS SOI Technology". In: *IEEE Journal of Solid-State Circuits* 41.12 (Dec. 2006), pp. 2945–2955.

[8] Ke Li et al. "A 30 Gb/s CMOS driver integrated with silicon photonics MZM". In: *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. Silicon Photonics Group, Zepler Institute, University of Southampton. 2015.

[9] Siamak Delshadpour and Xu Zhang. "A 20.6 Gb/s Programmable Peaking Gain CTLE". In: *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. NXP Semiconductors. Chandler, AZ, USA: IEEE, 2020.

[10] Sudip Shekhar, Jeffrey S. Walling, and David J. Allstot. "Bandwidth Extension Techniques for CMOS Amplifiers". In: *IEEE Journal of Solid-State Circuits* 41.11 (Nov. 2006), pp. 2424–2439.

[11] Eduard Säckinger. *Broadband Circuits for Optical Fiber Communication*. Hoboken, NJ, USA: John Wiley & Sons, 2005. ISBN: 978-0-471-71233-6.