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An Offline Single-Phase UPS with Voltage Harmonics Suppression

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Dissertação de mestrado apresentada para o Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina, para a obtenção do grau de Mestre em Engenharia Elétrica.

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Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado
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Prof. Lenon Schmitz, Dr
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Resumo

Esta dissertação de mestrado apresenta o projeto, implementação e validação de uma fonte de alimentação ininterrupta (*nobreak* ou Uninterruptible Power Supply (UPS)) monofásica *offline* com qualidade de tensão aprimorada sob cargas não-lineares. A UPS proposta utiliza um conversor *Dual Active Bridge* (DAB) CC-CC bidirecional com uma rede Ressonante CLLC e um inversor CC-CA de ponte completa que é conectado à rede elétrica por meio de um filtro LCL. É implementada uma arquitetura de controle que combina um controlador Proporcional Integral (PI) para a regulação do barramento CC e um controlador Proporcional Multirressonante (PMR) para o controle de tensão ilhada com compensação harmônica. A estratégia de supressão harmônica baseada em PMR é capaz de reduzir harmônicas de baixa ordem da tensão durante a operação ilhada, consequentemente melhorando a qualidade de energia. Tanto os resultados de simulação quanto os experimentais demonstram operação confiável, transição rápida entre os modos conectado e desconectado, e efetiva redução das harmônicas de tensão.

Palavras-chave: *nobreak* (UPS) *offline*, compensação harmônica, conversor DAB ressonante CLLC

Abstract

This master thesis presents the design, implementation, and validation of an offline single-phase UPS with enhanced voltage quality under non-linear loads. The proposed UPS utilizes a bidirectional Dual Active Bridge (DAB) DC-DC converter with a Resonant CLLC network and a full bridge DC-AC inverter which is interfaced to the mains by an LCL filter. A control architecture combining a Proportional Integral (PI) controller for DC bus regulation and a Proportional Multi Resonant (PMR) controller for off-grid voltage control with harmonic compensation is implemented. The PMR-based harmonic suppression strategy is able to reduce low-order voltage harmonics during islanded operation, thereby improving power quality. Both simulation and experimental results demonstrate reliable operation, fast transition between on-grid and off-grid modes, and effective voltage harmonic reduction.

Keywords: offline UPS development, harmonic compensation, resonant DAB CLLC

Resumo expandido

Introdução

Os efeitos crescentes das mudanças climáticas nas linhas de transmissão e distribuição de energia são uma grande preocupação tanto para as concessionárias quanto para os usuários, especialmente em áreas sujeitas a eventos climáticos extremos. Indicadores como SAIFI e SAIDI demonstram que a confiabilidade do fornecimento pode ser comprometida, afetando consumidores residenciais e industriais. Além disso, a popularização de fontes renováveis não despacháveis reduz a inércia da rede, diminuindo a estabilidade da frequência e aumentando o risco de apagões.

Neste cenário, os sistemas de Alimentação Ininterrupta de Energia (UPS) surgem como soluções vitais. Diferentemente de geradores a combustível, que possuem tempos de partida lentos, os UPS podem restaurar a energia em milissegundos. As topologias de UPS são classicamente divididas em *Online* (Dupla Conversão), *Line-Interactive* e *Offline* (Standby). A topologia *Online* oferece a melhor qualidade de energia, mas apresenta maior custo e menor eficiência devido à conversão contínua. A topologia *Offline* é mais eficiente e econômica, mas introduz um tempo de transferência durante falhas.

Este trabalho propõe e analisa uma topologia *Offline* modificada. Ao remover a indutância de desacoplamento típica da topologia *Line-Interactive* e alterar o esquema de operação para se assemelhar ao *Standby*, cria-se um híbrido que mantém a alta eficiência em modo normal, mas utiliza um estágio CC-CC bidirecional isolado. Isso permite o isolamento da bateria tanto da rede quanto da carga, utilizando apenas um transformador de alta frequência, e elimina a necessidade de chaves SPDT complexas, utilizando apenas chaves SPST.

Objetivos

O objetivo principal desta dissertação é fornecer uma visão geral das tecnologias de UPS e apresentar o desenvolvimento completo, da concepção teórica à implementação de protótipo, de um UPS *offline* monofásico.

Os objetivos específicos incluem:

- Desenvolver um sistema com capacidade de conexão e desconexão da rede elétrica.

- Implementar um componente de geração de fase que permita a operação independente fora da rede (*off-grid*), mas capaz de sincronizar suavemente com a rede elétrica.
- Projetar e validar um controlador Proporcional-Multi-Ressonante (PMR) para suportar cargas não lineares e suprimir distorções harmônicas na tensão de saída durante o modo ilhado.
- Analisar e projetar os conversores de potência: um estágio CC-CC do tipo CLLC *Resonant Dual Active Bridge* (RDAB) e um inversor monofásico em ponte completa.

Metodologia

A metodologia do projeto abrangeu a modelagem matemática, o dimensionamento de componentes, o desenvolvimento de *firmware* e a construção de um protótipo de *hardware* denominado “Powerlink”.

Topologia do Conversor de Potência O sistema utiliza uma bateria de baixa tensão (48 V nominais) interfaceada com um barramento CC de alta tensão (400 V) e, subsequentemente, com a rede elétrica (127/220 V).

1. **Estágio CC-CC (CLLC RDAB):** Foi selecionada a topologia *Resonant Dual Active Bridge* com rede CLLC simétrica. Esta escolha deve-se à capacidade de fluxo de potência bidirecional, isolamento galvânico e alta eficiência através de comutação suave (ZVS e ZCS). A modulação utilizada foi a *Triple Phase Shift* (TPS), permitindo três graus de liberdade para controle. O procedimento de projeto proposto define a frequência de ressonância f_r igual à frequência de comutação f_{sw} para desacoplar as dinâmicas de entrada e saída. A indutância magnetizante L_m foi calculada para minimizar a Distorção Harmônica Total (THD) das correntes em um ponto de operação ótimo (P_{opt}), encontrado em um ângulo de defasagem de $\phi_{opt} \approx 131^\circ$.
2. **Estágio CC-CA (Inversor):** Um inversor em ponte completa foi utilizado para interfacear o barramento CC com a rede/carga. A modulação PWM Unipolar foi escolhida por oferecer melhor THD e menores perdas. Para a filtragem de saída, optou-se por

uma topologia LCL+RC, que oferece grande atenuação com baixo volume e perdas de amortecimento reduzidas, complementada por um filtro de modo comum.

Estratégia de Controle O sistema de controle foi implementado em um microcontrolador STM32H7. A arquitetura de controle varia conforme o modo de operação:

- **Modo Ilhado (Off-grid):** O CLLC controla a tensão do barramento CC, enquanto o inversor atua como *grid-forming* (formador de rede), controlando a tensão CA de saída (v_{gin}).
- **Sincronização:** Uma Máquina de Estados Finitos (FSM) gerencia a transição entre operação ilhada e conectada. Um algoritmo de resincronização ajusta a fase do inversor ($\omega_i t$) para convergir com a fase estimada da rede ($\tilde{\omega}_g t$) obtida via SOGI-PLL antes do fechamento do relé de conexão.

Controlador PMR Para mitigar as harmônicas de tensão causadas por cargas não lineares (comuns em eletrônicos modernos), implementou-se um controlador Proporcional-Multi-Ressonante (PMR). Este controlador fornece alto ganho na frequência fundamental e nas frequências harmônicas ímpares ($3^a, 5^a, 7^a, 9^a$), garantindo rastreamento preciso e rejeição de distúrbios.

Resultados e Discussão

O protótipo desenvolvido permitiu a validação experimental das topologias e controles propostos. Os componentes passivos e parâmetros de controle foram selecionados conforme as metodologias de projeto descritas, resultando em um sistema estável.

Desempenho do Conversor CLLC As formas de onda experimentais do conversor CLLC operando a 50 kHz confirmaram o funcionamento da modulação TPS. Observou-se que a defasagem interna θ comportou-se conforme projetado, e a rede ressonante filtrou efetivamente a maioria das harmônicas de comutação da corrente, validando o modelo teórico.

Compensação de Harmônicos com PMR Testes comparativos foram realizados alimentando uma carga não linear (retificador a diodo com filtro capacitivo).

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- **Sem Compensação:** A tensão de saída apresentou distorções visíveis, causadas pela interação entre as correntes pulsadas da carga e a impedância do filtro de saída.
 - **Com Compensação PMR:** Ao ativar o controlador PMR, houve uma atenuação notável das harmônicas de baixa ordem. A análise via Transformada Rápida de Fourier (FFT) demonstrou claramente a redução das amplitudes das 3^a, 5^a, 7^a e 9^a harmônicas na tensão de saída v_{gin} . Embora tenha sido observado um leve aumento em oscilações de alta frequência (próximas à 21^a harmônica) devido à largura de banda dos ressonadores, o resultado global foi uma melhoria significativa na qualidade da energia.

Conexão e Desconexão da Rede Os testes de transição de modo validaram a robustez do software de controle.

- **Desconexão:** Durante um evento de surto/falha simulado, o sistema detectou a anomalia, abriu o relé de interface e iniciou o inversor em dezenas de milissegundos, restaurando a tensão nominal na carga.
- **Reconexão:** O algoritmo de ressincronização ajustou suavemente a fase do inversor à da rede. Após o fechamento do relé, o inversor desligou-se corretamente, deixando a carga ser alimentada pela rede, demonstrando uma transição segura.

Considerações Finais

Esta dissertação apresentou uma análise abrangente e o desenvolvimento prático de um UPS *offline* modificado. A topologia proposta, combinando um estágio CC-CC CLLC isolado e bidirecional com um inversor em ponte completa, provou ser eficaz para aplicações de baixa potência. As metodologias de projeto para os elementos passivos e para o controle digital demonstraram-se adequadas, permitindo a construção de um protótipo funcional.

Os resultados experimentais confirmaram que o controlador PMR é uma ferramenta essencial para a manutenção da qualidade de energia em modo ilhado, suprimindo efetivamente as distorções de tensão causadas por cargas não lineares modernas. Além

disso, a infraestrutura de *hardware* e *software* desenvolvida, incluindo o sistema de monitoramento remoto, forneceu uma base sólida para a operação segura do equipamento.

Conclui-se que o UPS desenvolvido atende aos requisitos de proteção de cargas críticas contra falhas de rede. Trabalhos futuros podem expandir este escopo validando os modos de operação conectados à rede para suporte auxiliar (como *load shifting* e regulação de frequência) e explorando a paralelização de módulos.

Palavras-chave: UPS Offline; Conversor CLLC; Inversor Monofásico; Controle PMR; Compensação Harmônica; Formador de Rede.

Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BESS	Battery Energy Storage System
CMC	Common-Mode Current
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAB	Dual Active Bridge
DC	Direct Current
DMA	Direct Memory Access
DMC	Differential-Mode Current
DPS	Double Phase Shift
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPS	Extended Phase Shift
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
FHA	Fundamental Harmonic Approximation
FM	Frequency Modulation
FSM	Finite-State Machine
GUI	Graphical User Interface
HC	Harmonic Compensation
IIR	Infinite Impulse Response
IO	Input/Output
IP	Internet Protocol
LED	Light Emitting Diode

LP	Low Pass
MCU	Microcontroller Unit
MMF	Magnetomotive Force
PC	Personal Computer
PCB	Printed Circuit Board
PEV	Plug-in Electric Vehicles
PI	Proportional Integral
PLL	Phase Locked Loop
PMR	Proportional Multi Resonant
PN	Part Number
PR	Proportional Resonant
PWM	Pulse Width Modulation
RDAB	Resonant DAB
RMS	Root Mean Square
SAIDI	System Average Interruption Duration Index
SAIFI	System Average Interruption Frequency Index
SMPS	Switched-Mode Power Supply
SOGI	Second-Order Generalized Integrator
SPDT	Single Pole Double Throw
SPS	Single Phase Shift
SPST	Single Pole Single Throw
SRDAB	Series Resonant DAB
SST	Solid State Transformer
THD	Total Harmonic Distortion
TLV	Tag (or Type) Length Value
TPS	Triple Phase Shift
TPSM	Triple Phase Shift Modulation

UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UPS	Uninterruptible Power Supply
VFD	Voltage and Frequency Dependent
VFI	Voltage and Frequency Independent
VI	Voltage Independent
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

$\left\langle \frac{dx}{dt} \right\rangle_k$	Dynamic phasor of the derivative of the state x
A	State dynamics matrix (state space representation)
A_0	DC coefficient of Fourier series
A_e	Magnetic core area (m^2)
A_n	Even coefficient of Fourier series
B	Input matrix (state space representation)
B_n	Odd coefficient of Fourier series
C	Output matrix (state space representation)
C_{bus}	DC bus capacitance (F)
C_d	Damping branch capacitance of the LCL+RC filter (F)
C_f	Main filtering capacitance of the LCL+RC filter (F)
$C_{PMR}(s)$	Proportional Resonant Controller transfer function
C_{r1}	Primary side resonant capacitance (F)
C_{r2}	Secondary side resonant capacitance (F)
C'_{r2}	Secondary side resonant capacitance referenced to the primary side (F)
$C_{R_k}(s)$	Resonant Controller transfer function of the k^{th} harmonic
C_s	Stray common-mode capacitance (F)
C_Y	Class Y capacitor for common-mode filtering (F)
D	Feed-forward matrix (state space representation)
d	Inverter duty cycle
f	Frequency (Hz)

f_{CM}	Cutoff frequency of the common-mode filter (Hz)
f_g	Frequency of the fundamental component of the grid voltage waveform (Hz)
f_{inv}	Inverter switching frequency (Hz)
$f_{maxLCLRC}$	Pole of the LCL+RC filter when $L_{f2} \rightarrow 0$ and $R_d = 0$ (Hz)
$f_{minLCLRC}$	Pole of the LCL+RC filter when $L_{f2} \rightarrow \infty$ and $R_d = 0$ (Hz)
f_r	Resonant frequency (Hz)
f_{sw}	CLLC Switching frequency (Hz)
g	Transconductance variable of the CLLC Resonant DAB (RDAB) equivalent large-signal model (S)
G	Maximum value of g when $\phi = 180^\circ$
i_1	Primary side current (A)
I_1	External DC current on the CLLC converter primary side (A)
i_{1,v_1}	Component of the primary side current excited by v_1 (A)
i_{1,v'_2}	Component of the primary side current excited by v'_2 (A)
I_2	External DC current on the CLLC converter secondary side (A)
i'_2	Current on the secondary side of the CLLC transformer referred to the primary side (A)
i'_{2,v'_2}	Component of the secondary side current referenced to the primary, excited by v'_2 (A)
$\langle I_2 \rangle_0$	Dynamic phasor of the DC component of I_2 (A)
$\langle i'_2 \rangle_1$	Dynamic phasor of the fundamental component of i'_2 (A)
$\langle i'_2 \rangle_1^{\Im}$	Imaginary part of the dynamic phasor of the fundamental component of i'_2 (A)
$\langle i'_2 \rangle_1^{\Re}$	Real part of the dynamic phasor of the fundamental component of i'_2 (A)
$\langle i_2 \rangle_1^{\Im}$	Imaginary part of the dynamic phasor of the fundamental component of i_2 (A)

$\langle i_2 \rangle_1^{\Re}$	Real part of the dynamic phasor of the fundamental component of i_2 (A)
i_{CM}	Common-mode current of the full bridge inverter (A)
i_g	Inverter output grid current (A)
i_{inv}	Inverter current (A)
i_{invHF}	High frequency (switching) component of the inverter output current (A)
$\langle i_{inv} \rangle_0$	Dynamic phasor of the DC component of i_{inv}
$i_{L_{f1}}$	Current through the filtering inductor L_{f1} of the LCL+RC filter (A)
j	Imaginary unit ($\sqrt{-1}$)
k	Harmonic order
k_e	Proportional controller of the SOGI structure
K_p	Proportional gain of the PMR controller
L_{CM}	Common-mode choke inductance (H)
l_e	Magnetic path length
L_{f1}	First inductance of the LCL+RC filter (H)
L_{f2}	Second inductance of the LCL+RC filter (H)
L_g	Grid inductance (H)
L_m	Magnetizing inductance of the CLLC transformer (H)
L_{r1}	Primary side resonant inductance (H)
L_{r2}	Secondary side resonant leakage inductance (H)
L'_{r2}	Secondary side resonant leakage inductance referenced to the primary side (H)
n	Harmonic order
n_1	Number of turns on the primary side of the CLLC transformer
n_2	Number of turns on the secondary side of the CLLC transformer

P_1	Active power flow on the primary side (W)
$p_{1,2}$	First pair of poles of the CLLC input admittance transfer function (rad/s)
$p_{3,4}$	Second pair of poles of the CLLC input admittance transfer function (rad/s)
P_g	Rated power on the output of the inverter, leading to the grid and load (W)
P_{opt}	Optimal power where the THD of the modulated voltage is minimum (W)
R_1	Resistance of the primary side of the CLLC (Ω)
R'_2	Resistance of the secondary side of the CLLC referred to the primary side (Ω)
R_{bus}	Leakage resistance of the DC bus (Ω)
R_d	Damping branch resistance of the LCL+RC filter (Ω)
$R_{d,CM}$	Damping resistance of the common-mode filter (Ω)
R_{out}	Resistive load of the inverter model (Ω)
s	Complex frequency variable of the Laplace Transform (rad/s)
T	Period of the fundamental switching frequency (s)
t	Time (s)
U	Input vector (state space representation)
u	Input of a system (state space)
v_1	Primary side full bridge voltage (V)
V_1	External DC voltage on the CLLC converter primary side (V)
$\langle v_1 \rangle_1$	Dynamic phasor of the fundamental component of v_1
$\langle v_1 \rangle_1^{\Im}$	Imaginary part of the dynamic phasor of the fundamental component of v_1 (V)
$\langle v_1 \rangle_1^{\Re}$	Real part of the dynamic phasor of the fundamental component of v_1 (V)
v'_2	Secondary side full bridge voltage referenced to the primary (V)
V_2	External DC voltage on the CLLC converter secondary side (V)

$\langle V_2 \rangle_0$	Dynamic phasor of the DC component of V_2 (V)
v_{bus}	Voltage of the DC bus (V). It is equal to V_2 when the CLLC converter is connected to the DC bus.
V_{bus}	Nominal value for the DC bus voltage (V)
v_{bus}^*	Reference (setpoint) of v_{bus} (V)
v_{C_d}	Voltage of the damping capacitance C_d of the LCL+RC filter (V)
v_{C_f}	Voltage of the filtering capacitance C_f of the LCL+RC filter (V)
v_{CM}	Common-mode voltage (V)
V_g	Nominal grid RMS voltage (V)
v_{gin}	Filtered voltage (after the LCL+RC) of the inverter applied to the load (V)
v_{inv}	Inverter output voltage (V)
$v_{m,v2}$	Magnetizing voltage component excited by v_2' (V)
$\dot{X}$	State vector derivative
X	State vector (state space representation)
x	Generic variable or a state (state space)
$x(t)$	Arbitrary periodic function in time
x_0	Initial state of a state “ x ”
X_k	Dynamic phasor of the k^{th} harmonic of the state X
Y	Output vector (state space representation)
Y_{eq,v_1}	Equivalent input admittance (S)
$z_{1,2}$	Pair of zeros of the CLLC input admittance transfer function (rad/s)
Z_b	Base impedance (Ω)
Z_{eq,v_1}	Equivalent (input) impedance of the CLLC network excited by the primary side (Ω)

Z_{eq,v'_2}	Equivalent impedance of the CLLC network excited by the secondary side (Ω)
γ_{CM}	Designed transadmittance attenuation at $f = f_{CM}$ for the common-mode filter (A/V)
$\mathcal{F}$	MMF (A) induced by a current in a magnetic core
$\mathcal{F}_1$	MMF (A) from the primary side (CLLC transformer)
$\mathcal{F}_2$	MMF (A) from the secondary side (CLLC transformer)
$\mathcal{F}_m$	MMF (A) at the central E core leg (CLLC transformer)
$\mathcal{R}$	Magnetic reluctance (H^{-1}) on a path
$\mathcal{R}_{eq}$	Equivalent magnetic reluctance (H^{-1}) seen by the primary side (CLLC transformer)
$\mathcal{R}_g$	Magnetic reluctance (H^{-1}) of the lateral E core air gap (CLLC transformer)
$\mathcal{R}_l$	Magnetic reluctance (H^{-1}) of the central E core air gap (CLLC transformer)
μ	Magnetic permeability
μ_0	Magnetic permeability of the air
ω	Fundamental angular frequency (rad/s)
ω_{bw_k}	Bandwidth of $C_{R_k}(s)$ (rad/s)
ω_{CM}	Cutoff frequency of the common-mode filter (rad/s)
ω_g	Angular frequency of the grid voltage fundamental component (rad/s)
$\tilde{\omega}_g$	Estimated value of ω_g from the PLL (rad/s)
ω_g^*	Setpoint or nominal value of ω_g (rad/s)
ω_i	Inverter reference frequency (rad/s)
ω_k	Peak (central) frequency of $C_{R_k}(s)$ (rad/s)
ω_r	Resonant angular frequency (rad/s)
$\frac{\partial y[n]}{\partial x[m]}$	Partial derivative of the n^{th} element of any vector y with respect to the m^{th} element of any vector x

ϕ	Phase shift angle (rad)
Φ	Operating point of ϕ considered for linearization
ϕ_{opt}	Optimal phase shift angle where the THD of the modulated voltage is minimum (rad)
ψ_1	Magnetic Flux (Wb) on the primary side of the CLLC transformer
ψ_2	Magnetic Flux (Wb) on the secondary side of the CLLC transformer
θ	Phase shift angle between primary and secondary voltages (rad)

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1 Introduction

The increasing effects of climate change in grid transmission and distribution lines are a great concern for both power companies and users, especially in areas subject to extreme wind gusts and ice storms [7]. Some indicator of these issues are the high levels of System Average Interruption Frequency Index (SAIFI) and System Average Interruption Duration Index (SAIDI), which combined compromise the reliability of supply to any residential, commercial or industrial customer [8].

Moreover, the popularization of renewable non-dispatchable energy sources creates a scenario where the grid loses inertia, decreasing frequency stability [9] and thus increasing the chances of blackouts.

Some of the solutions to be considered when dealing with the aforementioned issues are standby generators and UPS systems. While the fuel powered generators can provide power for long durations, their startup time may take many seconds and their dependency on periodic maintenance and frequent tests might make them unsuitable for many applications [10, 11, 12]. An UPS, on the other hand, may take anywhere from zero to dozens of milliseconds to restore power — depending on its working principle — making them attractive to time sensitive and critical operations.

UPS systems are broadly classified into three major topologies: Offline (or Standby), Line-Interactive, and Online (or Double-Conversion). The Online topology offers the highest level of power quality, as the load is constantly fed by the inverter, providing zero transfer time and effective isolation from grid disturbances, but this comes at the cost of higher complexity, greater heat dissipation, and reduced operating efficiency [13, 14]. Conversely, the Offline topology is the simplest and most cost-effective, achieving high efficiencies in grid-connected mode by feeding the load directly from the mains and activating the inverter only when a power failure occurs [15, 16]. The Line-Interactive has mixed characteristics between the Online and Offline, and further details will soon be elaborated.

However, the primary drawback of Offline and Line-Interactive topologies becomes evident when supplying modern electronic equipments. Loads such as computers, servers, and LED lighting utilize switch-mode power supplies (SMPS), which draw highly distorted, non-sinusoidal currents from the UPS output. The current harmonics degrades the quality of the voltage supplied by the UPS inverter, especially during off-grid operation. The resulting distorted output voltage, characterized by high Total Harmonic Distor-

tion (THD), can compromise the performance or lifetime of sensitive devices. Therefore, the challenge in designing the Offline topology is to develop a control strategy that can effectively suppress these voltage harmonics during battery operation.

This master thesis aims to provide an overview on UPS technologies before presenting the development of an offline single phase UPS. The prototype development encompasses the conceptual analysis of the power converter systems, as well as their control schemes, design procedures, and an overview on the underlying hardware and software development.

Unlike inverters used in motor drive and photovoltaic applications, UPS inverters must operate as either grid-following when connected or as grid-forming when disconnected from the mains. Moreover, while the former applications have well defined loads, UPS may need to supply energy to many kinds of devices, be it a simple resistor-based load, inductive or capacitive reactive loads, nonlinear power converter loads, or a combination of them.

These requirements increase the overall system complexity both in terms of hardware and software, and demand a careful development. Thus, some key features of this work include:

- Grid connection and disconnection capability;
- Phase generation component to allow an independent off-grid reference generation despite being capable of smoothly synchronizing to the grid;
- Proportional Multi Resonant (PMR) controller to support loads which cause voltage harmonic distortions.

1.1 Uninterruptible Power Supplies

UPS systems have been around for many decades, establishing them as a fairly mature technology whose applications guarantee the reliance of many devices such as industry controllers, computer and communication systems,

The review done by [13] provides an overview of UPS topologies with power ratings up to 1 kVA, their classification criteria, advantages and disadvantages. The three main divisions of topologies are classified based on the main power flow path and power transfer method upon grid failure:

- Double conversion (online);
- Line-interactive;
- Standby (Offline).

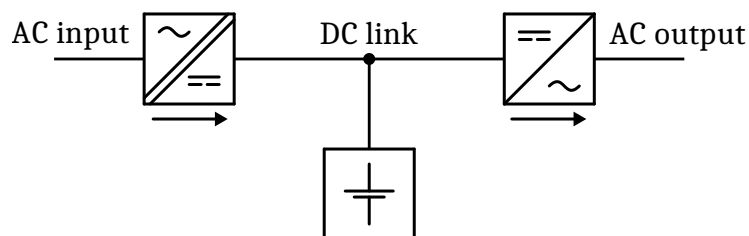
These categories still hold to the present day, and have been formalized by IEC 62040 [17]. The following sections 1.1.1, 1.1.2 and 1.1.3 will respectively discuss them and provide an overview of each according to the current understanding of IEC 62040 [17].

1.1.1 Double conversion (online) topology

The double conversion topology is understood as a continuously operating conversion device, in which the grid Alternating Current (AC) input is rectified into a Direct Current (DC) link where a battery is positioned. This DC is then converted back to AC by an inverter connected to the load. Figure 1 shows a block diagram representing both AC/DC and DC/AC conversion steps.

Because the DC link is always powered by the battery — assuming it has enough charge — in the event of a grid outage, the inverter will be able to continue its operation as if nothing has happened, except for possibly a small disturbance transient. Thus, in terms of down time, this topology provides the best solution for guaranteeing the supply of critical loads. As a down side, because two power converter stages are continuously operating, even in normal grid conditions, its efficiency tends to be lower than topologies with direct connection to the grid. Moreover, the two conversion stages need to be robust for continuous operation, possibly making the semiconductors more expensive.

Figure 1: Double conversion UPS topology.



Source: adapted from [17], annex B.2.

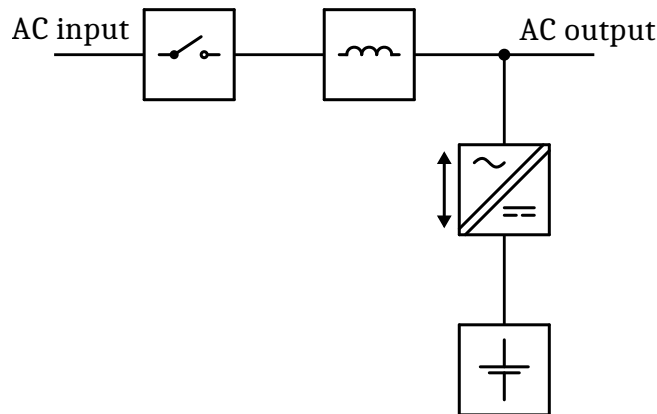
This type of UPS is classified by [17] as Voltage and Frequency Independent (VFI), meaning the output waveform is (mostly) unaffected by the mains in terms of both voltage and frequency.

Although the double conversion topology may be isolated, a non-isolated solution is also possible, as demonstrated by Choi et al. [18], whose work proposes a three-leg non-isolated online (double-conversion) UPS. The proposed structure offers low losses and low cost due to the reduced number of components.

1.1.2 Line-interactive topology

The line-interactive topology consists of a bidirectional converter to couple the battery with the AC output and a grid interface between the AC input and the output, as shown in Figure 2. Due to the bidirectional capability, the converter is able to both charge and discharge the battery by the same path. The grid interface consists essentially of a switch in series with an inductive impedance in order to separate the circuit from the grid during an outage and to decouple the input and output voltages, respectively. This inductance may also come in the form of a tapped transformer to allow adjustments to the voltage amplitude on the load side.

Figure 2: Line-interactive topology.



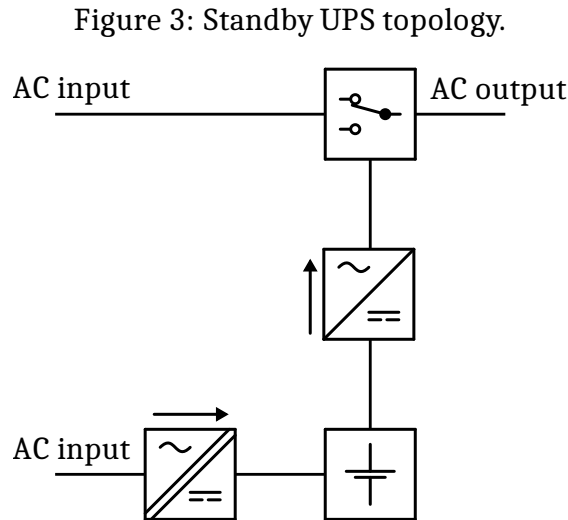
Source: adapted from [17], annex B.3.

According to [17], the line-interactive UPS is considered as Voltage Independent (VI) because the voltage decoupling on the input interface allows the converter to shape the voltage amplitude on the output, although still in phase with the grid (frequency dependent). One example application of line-interactive UPSs is presented by [19], where active line conditioning is used to reduce grid current distortion. Kamran et al. [20] proposed an online UPS with line interaction capability by inserting a series and a parallel converter between load and grid.

1.1.3 Standby (offline) topology

Depicted in Figure 3, the last standard UPS type is characterized by its standby topology, in which the load is directly connected to the grid in normal operation, while the battery is kept charged by the grid via another path. As soon as the AC input leaves the normal operating region, the device starts the inverter and starts supplying the load to maintain normal operation.

Because the inverter stays off when the grid is within the accepted tolerance region, this type of UPS usually displays less power losses in normal conditions. However, the time delay needed to start the inverter makes it the slowest option to restore power to the load.



Source: adapted from [17], annex B.4.

IEC 62040 [17] classifies this UPS type as Voltage and Frequency Dependent (VFD) because, in normal operation, the voltage waveform seen by the load is exactly that of the grid, making it fully dependent on the voltage and frequency imposed by the mains.

A transformerless offline UPS is proposed by [15], which although has a transfer time of 10 ms (from grid to battery mode), has low cost and size.

1.1.4 Proposed modified topology and operation scheme

The double conversion topology provides the best solution to protect sensitive critical loads from grid disturbances and outages, such as data centers. However, this comes at a higher cost of components due to its complexity and need for increased reli-

ability because of its continuous power conversion, which also penalizes energy efficiency.

Alternatively, a line-interactive UPS is constantly connected to the grid and is able to continuously shape the output voltage in parallel to the grid. However, this requires an inductance at the input to decouple the mains voltage from the inverter's, slightly increasing cost, size, and drawing more reactive power compared to the standby topology even when the grid is online.

If greater efficiency, lower cost and lower complexity is desired, a standby topology might be preferred, even when facing larger power restoration delays.

By removing the decoupling inductance from the line-interactive topology and by changing the operation scheme to resemble that of the standby topology, a modified offline UPS type can be created, as shown in Figure 4. These modifications attempt to mix characteristics usually present in either the line-interactive or the standby types.

Because the the load is now directly connected to the grid on normal conditions, the efficiency and power factor match that of the standby topology. However, this modified type does not need a Single Pole Double Throw (SPDT) switch, thus a Single Pole Single Throw (SPST) switch is sufficient.

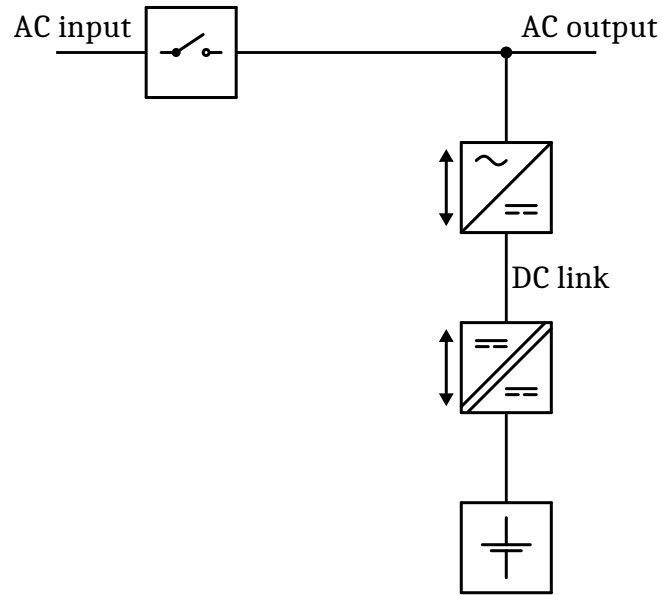
Also, due to the now inherent bidirectionality of the DC/AC conversion stage, the battery is essentially isolated¹ from both the input mains and the output load, even by using a single² high frequency transformer. This transformer also facilitates the step-up and step-down between the battery voltage and the DC bus voltage by adjusting its windings ratio. Besides, since the inverter has direct connection to the mains, it is possible to provide grid support functionalities such as load shifting [22], reactive power compensation [23] and frequency inertia support [24] (although these features are not in the scope of this work).

Table 1 summarizes a general comparison of the four discussed UPS topologies. Another advantage of this modified UPS type as compared to the standby topology is the fact that the single bidirectional path used for charging and discharging the battery makes it possible to reuse the same sensors for both operation modes.

¹The isolation is recommended for safety reasons [21], especially from the grid. Output isolation adds another safety layer against unwanted accidental battery discharge.

²As demonstrated by [13], double conversion UPS devices might also isolate the battery both at the input and at the output, although that would require at least two transformers.

Figure 4: Proposed UPS topology.



Source: own work.

Table 1: Comparison of UPS topologies.

	Double conversion	Line- interactive	Standby	Proposed modified
Grid decoupling inductance	No	Yes	No	No
Cost & complexity	High	Medium	Low	Low
Efficiency with active grid	Low	Medium	High	High
Switch type needed	None	SPST	SPDT	SPST
Power restoration delay	None	Medium	High	High
Battery isolation	Input and/or output	Input and output ³	Input	Input and output ³

Source: own work.

Having researched different types of UPS systems, the question is now how these

³Bidirectional battery charging and discharging isolates the battery from both input and output.

are implemented in practice. Section 2 will define the requirements for the battery and for the topology, followed by a detailed modeling of the adopted topology for the DC-DC and DC-AC power conversion stages. Next, section 3 will present a detailed overview of Powerlink, the developed prototype, both in terms of hardware and software. Finally, the experimental results from the performed tests will be brought up in section 4.

2 Power conversion systems

With an overall architecture topology selected (Figure 4), there are still many possibilities to implement each individual conversion stage, that is, DC/DC and DC/AC.

This current Section will first discuss the possible choices for both stages based on the requirements (subsection 2.1). Then, a topology for each of the DC/DC and DC/AC stages will be chosen and detailed in the following subsections 2.2 and 2.3, respectively.

2.1 General topology definitions

Before deciding on the power conversion topologies, some constraints must be set to guarantee that the requirements are met. First and foremost, because the battery needs to be charged and discharged via the same path, both stages must allow bidirectional power flow. Furthermore, the battery bank specifications themselves must be defined prior to the final decision.

2.1.1 Battery requirements

Batteries come in many shapes and forms of technologies with very different characteristics and are able to suit many applications such as UPS, Plug-in Electric Vehicles (PEV) and Battery Energy Storage System (BESS) [25], as well as other consumer appliances. With the aim to choose the power conversion topologies, some home energy storage products available on the market were briefly analyzed with respect to their main electrical specifications, as shown on Table 2.

Some batteries such as those manufactured by Generac [26], Panasonic [27] and BYD [28] have a modular design approach, allowing some or many batteries in parallel to increase energy storage and power output, while others such as from Enphase [29] and Tesla [30] are monolithic integrated with the inverter.

One thing all analyzed commercial batteries have in common is the usage of low voltage rating in the range from 46 V to 68 V, and since 48 V is an optimal balance between safety and power transfer efficiency typically used in residential applications [31, 32], this voltage level was selected as the nominal input for the conversion system.

2.1 General topology definitions

Table 2: List of analyzed home energy backups based on batteries.

Model	Grid voltage (V)	Energy storage (kWh)	Output Power (kVA)	Battery voltage (V)
Enphase IQ Battery 10T [29]	240	10	3.84	67.2
Panasonic EverVolt Standard [27]	120; 240	11.4	4.6	46.2
Generac PWRcell [26, 33]	120; 240	3	7.2	46.8
Tesla Powerwall [30]	120; 240	14	5	50
BYD BatteryBox LV Flex Lite [28]	—	5	3.5	51.2

Source: own research.

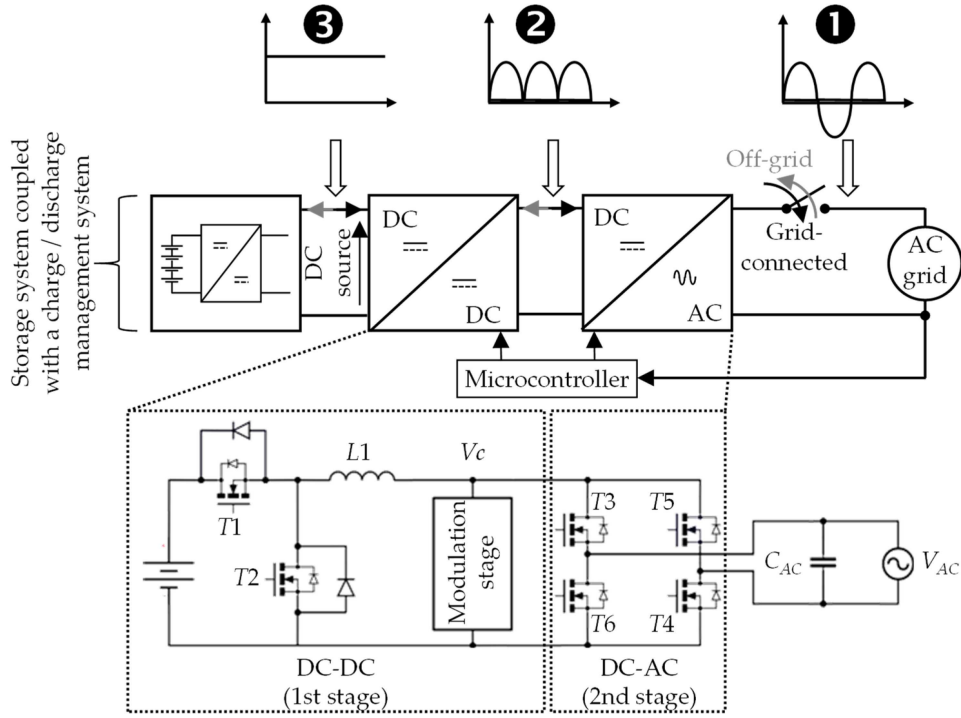
2.1.2 Topology requirements

The topology architecture choice for a power conversion system to interface a 48 V battery with the mains⁴ can be accomplished in many ways.

A bidirectional architecture is proposed by [34] and shown in Figure 5. This topology consists of a bidirectional buck and boost converter as the first DC/DC stage with sinusoidal modulation, followed by the DC/AC low frequency unfolding inverter. Because of the lower switching losses on the inverter and the direct galvanic connection between input and output, this topology can provide very high conversion efficiency while still being bidirectional. However, due to the lack of isolation, this topology doesn't meet the safety requirement. Furthermore, the limited voltage gain on the DC/DC stage makes it unsuitable to step 48 V up to above the mains peak voltages of 180 V or 311 V (127 V or 220 V RMS, respectively).

⁴Brazilian domestic AC low voltage grid is either 127 V or 220 V single phase RMS at 60 Hz, depending on the region.

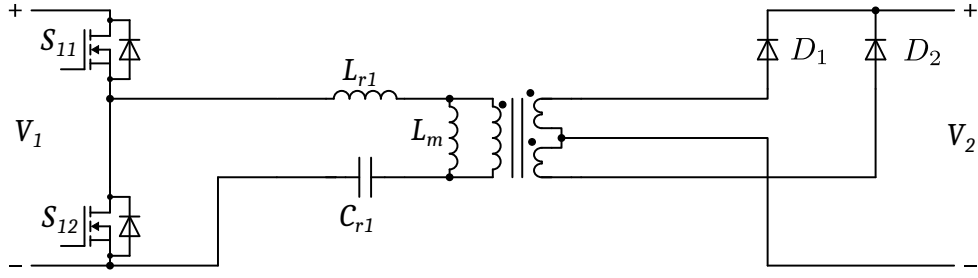
Figure 5: Bidirectional DC/AC converter.



Source: copyright © [34] and licensed as CC BY [35].

Since galvanic isolation and a greater DC/DC gain are required, the LLC resonant converter as reviewed by [36] and depicted in Figure 6 may be considered along with its other advantages such as lower switching losses — because of Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) soft switching — which enables the usage of higher frequency, thus allowing for a reduced size resonant network and a higher power density. As can be seen in Figure 6, however, the output rectifier of this DC/DC converter makes it unidirectional. Moreover, its input consists of a single half-bridge, which although may reverse the current flow, it cannot reverse the voltage, making it only two quadrants, thus limiting the possible voltage waveforms that can be modulated on the resonant network (only positive square pulses are hereby feasible).

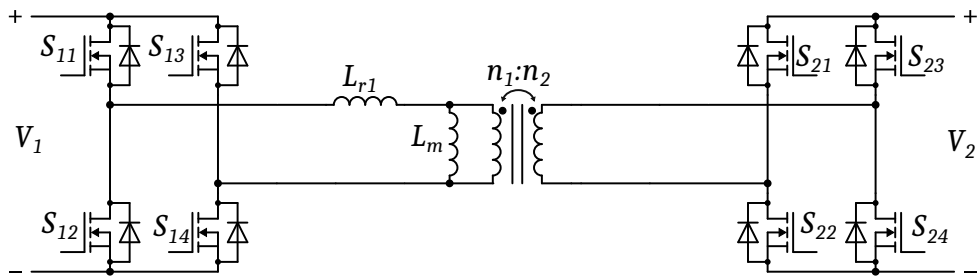
Figure 6: LLC resonant converter.



Source: adapted from [36].

Since a bidirectional four-quadrant isolated DC/DC converter is desired, the DAB topology, as shown in Figure 7, might be chosen to build this conversion stage, as it is commonly adopted in high power applications such as in Solid State Transformers (SSTs), UPS and BESS [37]. The usage of two full bridges on both sides of the high frequency transformer allows the modulation of unipolar voltages, making it possible to perform not only Single Phase Shift (SPS), but also Extended Phase Shift (EPS), Double Phase Shift (DPS) or Triple Phase Shift (TPS) modulations [38]. If the voltage amplitude of the primary and secondary sides do not match, however, the currents through the transformer acquire greater amplitudes [38], and so do their harmonics when considering the inductances only provide first order filtering capabilities. Because the transformer acts as a low-pass filter, a zero-frequency current harmonic (i.e. DC component) may arise, possibly offsetting the transformer operating point and increasing the likelihood of core saturation.

Figure 7: DAB converter.



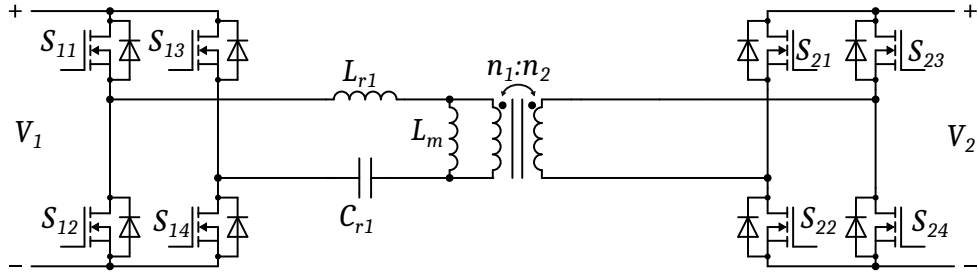
Source: adapted from [35].

To improve the soft switching performance [38] and decrease the harmonic distortion [37] — including the elimination of the DC component — a resonant network may be assembled with the transformer.

By joining some features of the unidirectional LLC with the DAB converter, the

Series Resonant DAB (SRDAB) converter is created, as depicted in Figure 8. This topology can transfer power in both directions just like the DAB converter with voltage and current reversibility, while still maintaining some of the advantages of the LLC converter, such as higher efficiency [39].

Figure 8: SRDAB converter.

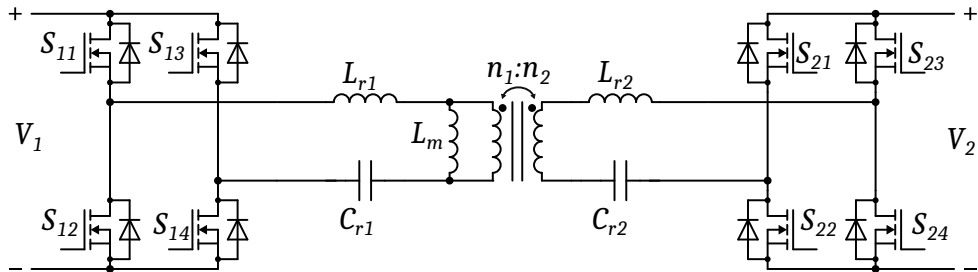


Source: adapted from [40].

To allow the cancellation of the DC component on the secondary side, a secondary capacitor may be added to the RDAB, turning it into a CLLC RDAB converter, which consists of a DAB with a symmetric CLLC network, and is represented in Figure 9. According to [38, 41], the symmetric CLLC can have high efficiency by undergoing ZVS.

This topology may be controlled by either using phase shifting modulations (SPS, DPS and TPS) as is common practice with the DAB converter, or by varying its switching frequency as often done with the LLC. This last method uses the so called Frequency Modulation (FM) and takes advantage of variable magnitude gain due to the frequency response of the CLLC network. However, this work will solely focus on the phase shift modulation.

Figure 9: CLLC RDAB converter.

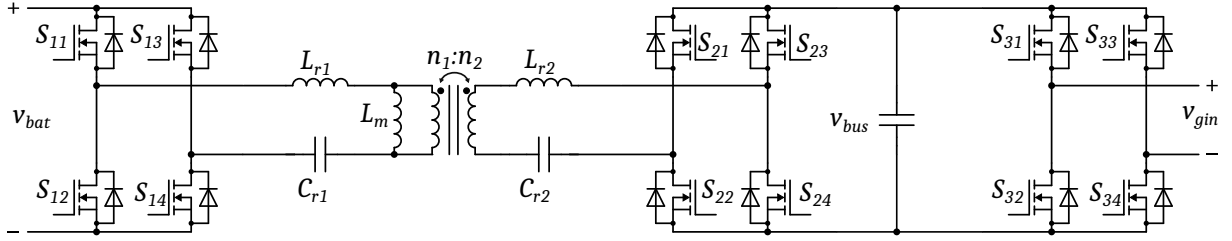


Source: own work.

With the DC/DC topology selected, the output DC/AC stage must be chosen as well. Considering this UPS will work on a single phase system and must be able to form an islanded grid, a simple Voltage Source Converter (VSC) topology such as the full bridge

might be selected and coupled on the secondary side of the CLLC converter. Then, the final power conversion topology is assembled and is shown in Figure 10.

Figure 10: Complete topology — CLLC RDAB + full bridge inveter.



Source: own work.

This two-stage bidirectional converter is very versatile for interfacing a low voltage battery to the mains and it allows the operation of three different power flow modes regarding this UPS system:

- On-grid charge, which allows the battery to be charged when the grid is functional;
- On-grid discharge to allow grid support interactions or simple energy trade;
- Off-grid discharge, which is triggered on grid fault to maintain supply to the load.

2.2 CLLC RDAB converter

The CLLC RDAB highlighted in Figure 9 consists of two full bridges with one DC and one AC side. The DC side is connected externally to capacitor banks to stabilize the voltage and to provide low impedance for high frequency switching currents, while the AC side is connected to the CLLC network.

In order to model the complete UPS system, section 2.2 will discuss the basic working principle of this DC/DC converter, and later propose a design methodology to guide the choice of the reactive components.

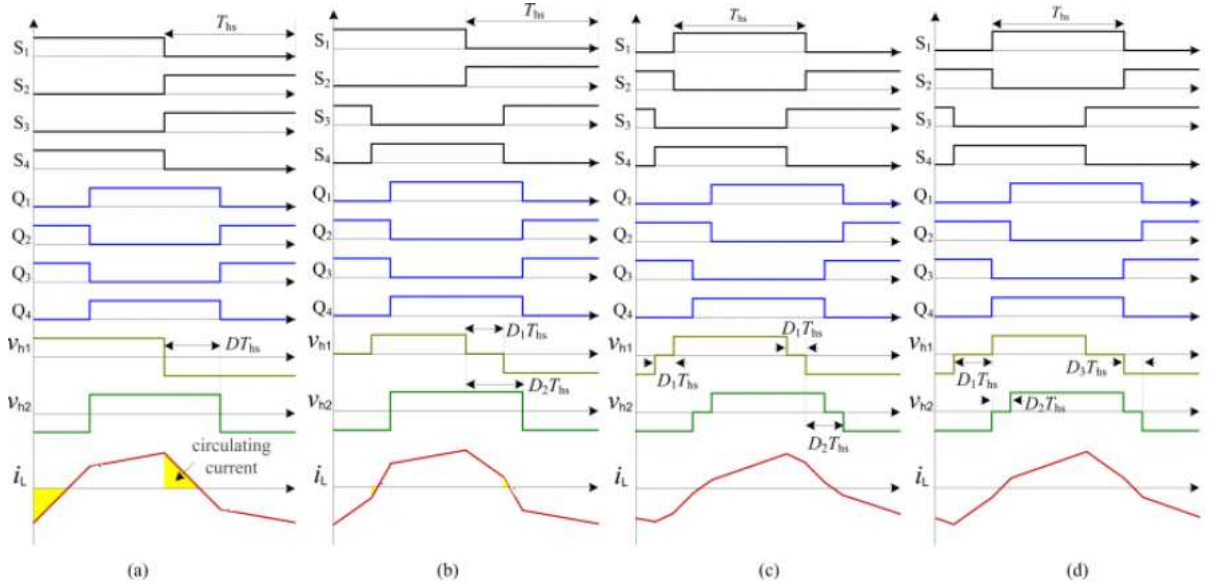
2.2.1 Working principle

To work with the CLLC converter, it is essential to understand its control requirements and its mathematical working principle. In order to gain a deep insight of the CLLC RDAB converter, first the modulation will be discussed, followed by a steady-state model derivation, and finally a dynamic model will be presented.

2.2.1.1 Modulation

The most commonly used phase shift modulations, as described by [38], include the SPS, EPS, DPS and TPS modulations, which are graphically explained in Figure 11. SPS is implemented by generating two bipolar square voltage waveforms with both full bridges, in which the phase shift angle between them is the control input. EPS introduces another degree of freedom by allowing the control of phase shift angle between two switching branches on the same full bridge, which creates a unipolar voltage waveform, thereby improving efficiency [38]. DPS extends the controllability by letting both full bridges vary their pulse angles in equal amount, as well as the phase offset between them. Finally, the TPS allows the phase offset and both pulse angles to be independent from one another, effectively providing three degrees of freedom for controlling both unipolar voltage waveforms. In practice, TPS is a generalization of all the others, and for this reason, this work implements the CLLC converter control with the flexible TPS modulation.

Figure 11: Comparison of phase shift modulations: (a) SPS; (b) EPS; (c) DPS; (d) TPS.



Source: copyright © 2011 IEEE [38].

The TPS modulation defines three angles:

- ϕ_1 , the phase shift of the first full bridge;
- ϕ_2 , the phase shift of the second full bridge;
- θ , the phase offset between the first and second full bridges waveforms.

As will be seen later, all these angles affect the rate of power flow between the primary and secondary sides of the CLLC.

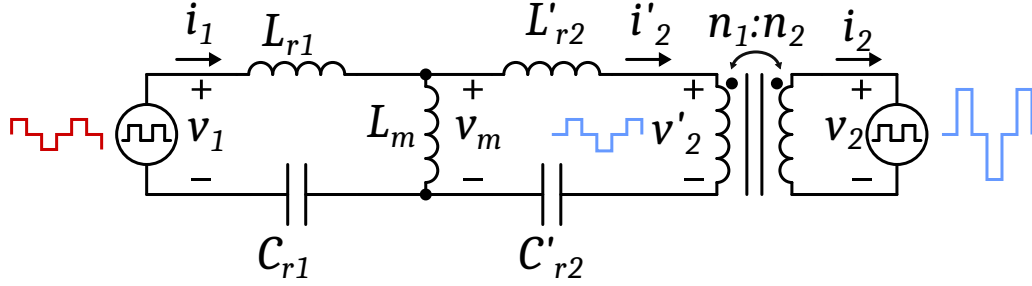
2.2.1.2 Steady state model

The derivation of the steady-state model which describes the CLLC RDAB converter behavior is important not only to understand the post-transient state, but also to define a power flow equation to help with the design procedure, which will be discussed in section 2.2.2.

Figure 12 shows the equivalent circuit of the CLLC network under the excitation of the primary and secondary full bridges (v_1 and v_2). Note that the real transformer is represented by the T model followed by an ideal transformer, and all secondary side electrical parameters are also referenced to the primary side, as denoted by the prime symbols (v_2 is

the higher voltage modulation of the secondary side, while v'_2 is stepped down to approximately match the level of v_1).

Figure 12: CLLC network impedance model.



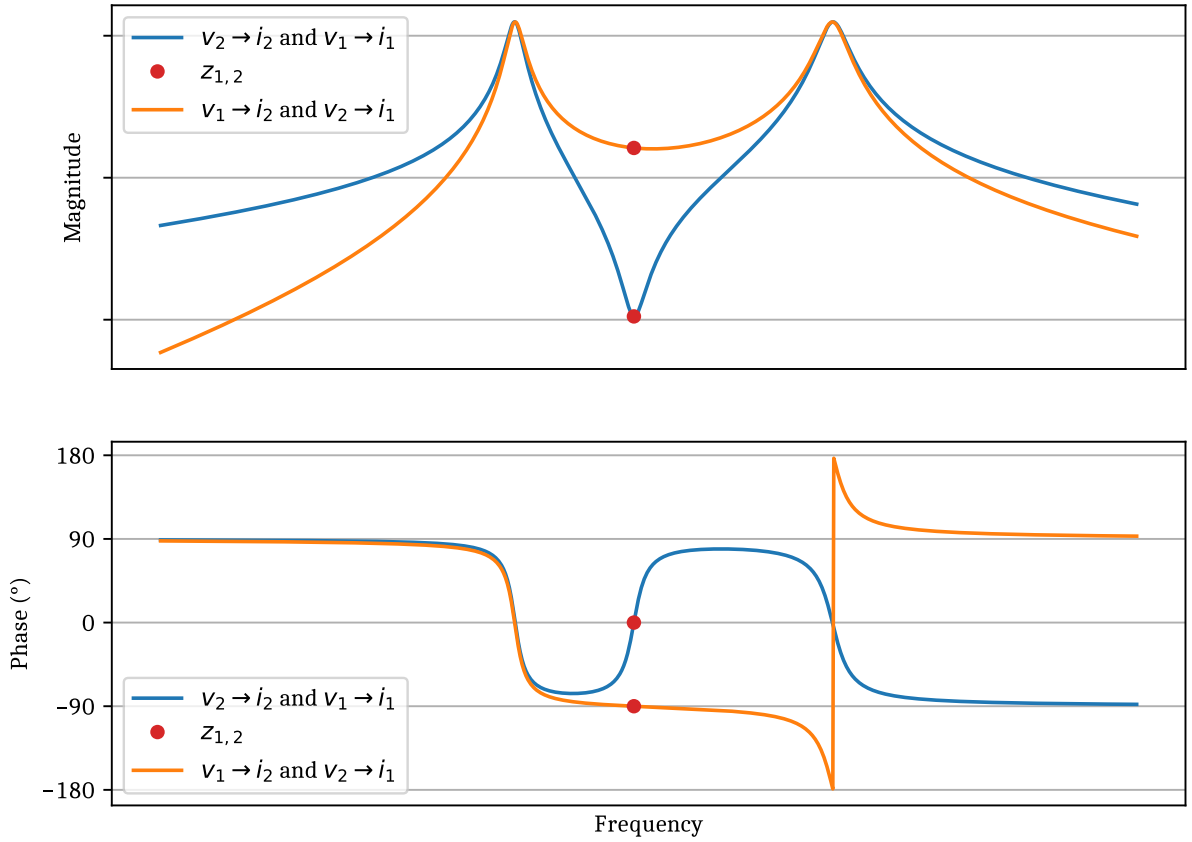
Source: own work.

In summary, the steady-state model is developed using the Fundamental Harmonic Approximation (FHA) method [42] by analyzing the superposed effects of both TPS modulated full bridge voltages v_1 and v_2 applied to the CLLC network, and how they affect the primary side current i_1 . This analysis is done in the frequency-domain using static phasors on the switching frequency, and all harmonics but the fundamental are disregarded. Therefore, the average power may be computed using a simple product of v_1 and i_1 . Inside the CLLC network, variables are all AC (v_1 , i_1 , v'_2 , etc.), but since it consists of a DC/DC converter, we are also interested in the external DC behavior, and the energy conservation principle can fill this gap.

Firstly, the analysis is greatly simplified if the passive elements are designed to be symmetric, so that $C'_{r2} = C_{r1}$, $L'_{r2} = L_{r1}$ and $R'_2 = R_1$. Although resistances are intrinsic to every circuit, they were not represented on the diagrams because they are not actual components on the assembled circuit (i.e., there are no discrete resistors).

To provide an overview of the general CLLC admittance characteristics, Figure 13 illustrates the frequency responses from the voltages v_1 and v_2 to the currents i_1 and i_2 . The input and output admittance frequency responses (in blue) show a magnitude dip (in red) at the frequency $z_{1,2}$, which will be later clarified.

Figure 13: Generic transfer functions frequency responses from v_1 and v_2 to i_1 and i_2 .

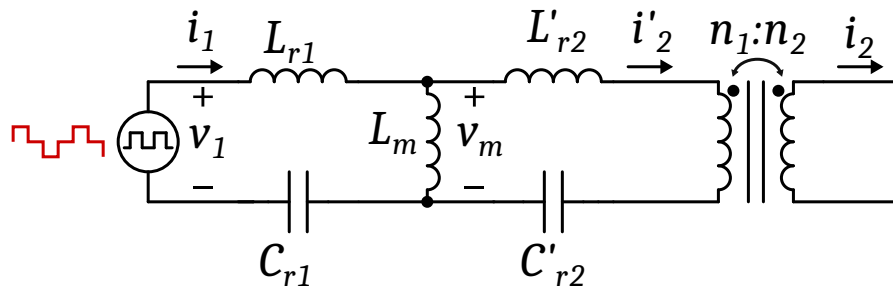


Source: own work.

2.2.1.2.1 Primary side excitation

The first step is to analyze the interactions of the primary voltage v_1 and the primary current i_1 . Because the only circuit excitation comes from v_1 , the secondary side voltage is shorted, as shown in Figure 14.

Figure 14: CLLC network impedance model excited by the primary side (secondary side shorted).



Source: own work.

Now, the relationship between v_1 and i_1 is as simple as the equivalent impedance Z_{eq,v_1} , as shown in

$$Z_{eq,v_1} = L_{r1}s + R_1 + \frac{1}{\frac{1}{L_{r1}s + R_1 + \frac{1}{C_{r1}s}} + \frac{1}{L_m s}} + \frac{1}{C_{r1}s}. \quad (1)$$

If C_{r1} is tuned to resonate with the inductance of the primary coil L_1 (that is, the sum $L_m + L_{r1}$) at the fundamental component of the switching frequency, as shown in

$$C_{r1} = \frac{1}{-s^2 (L_m + L_{r1})}, \text{ where } s = j\omega_r, \quad (2)$$

then (1) is simplified to

$$Z_{eq,v_1} = -\frac{L_m^2 s^2}{R_1} + R_1. \quad (3)$$

Notice how if the system is lossless, that is, if $R_1 = R'_2 = 0 \Omega$ in (3), the input impedance becomes infinite at the resonant frequency. That means if the primary self-resonates in this condition, v_1 will not influence i_1 . This phenomena corresponds to the magnitude dip at $\omega_{1,2}$ shown in Figure 13.

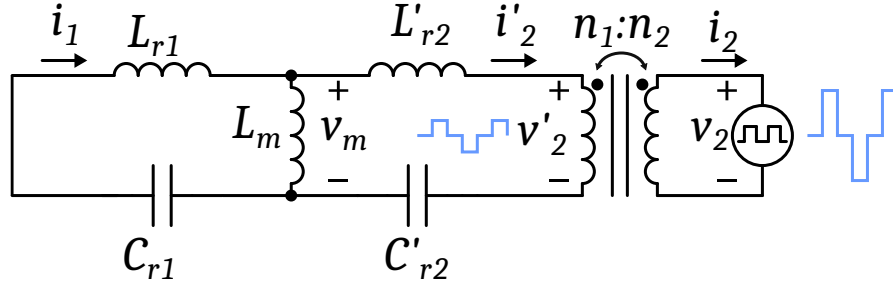
The component of the primary side current excited by v_1 is then given by

$$i_{1,v_1} = -\frac{R_1 v_1}{L_m^2 s^2 - R_1^2}. \quad (4)$$

2.2.1.2.2 Secondary side excitation

After computing the i_1 component excited by v_1 , the same must be done for v'_2 . This case is the opposite of the former, and as is depicted in Figure 15, the primary side is shorted so that only the excitation of the secondary is considered.

Figure 15: CLLC network impedance model excited by the secondary side (primary side shorted).



Source: own work.

Similarly, the output impedance Z_{eq,v'_2} may be computed by (5) in order to derive the secondary side current i'_2 . Notice how the secondary side parameters in (5) are replaced with their primary side equivalents as given by the symmetry condition.

$$Z_{eq,v'_2} = L_{r1}s + R_1 + \frac{1}{\frac{1}{L_{r1}s + R_1 + \frac{1}{C_{r1}s}} + \frac{1}{L_ms}} + \frac{1}{C_{r1}s} \quad (5)$$

If again C_{r1} is tuned to resonate with L_1 ($L_m + L_{r1}$), then (5) is simplified into

$$Z_{eq,v'_2} = -\frac{L_m^2 s^2}{R_1} + R_1. \quad (6)$$

In the same manner as before, (6) shows that in a lossless condition, the secondary side voltage v_2 and v'_2 will not generate current on the secondary side (i_2 and i'_2) at the resonant frequency, because the output impedance becomes infinite.

The current component on the secondary side i'_2 excited by v'_2 is given by (7), and its main purpose here is to help computing the magnetizing voltage v_m .

$$i'_{2,v'_2} = \frac{v'_2}{-\frac{L_m^2 s^2}{R_1} + R_1} \quad (7)$$

The magnetizing voltage component excited by v'_2 is given by (8). This voltage is used to compute the primary side current i_1 as excited by v'_2 .

$$v_{m,v2} = v'_2 - \frac{v'_2 (L_{r1}s + R_1 - s(L_m + L_{r1}))}{-\frac{L_m^2 s^2}{R_1} + R_1} \quad (8)$$

Finally, the component of the primary current i_1 excited by v'_2 is given by

$$i_{1,v'_2} = \frac{R_1 v'_2 [L_{r1}s + R_1 - s(L_m + L_{r1})] - v'_2 (-L_m^2 s^2 + R_1^2)}{(-L_m^2 s^2 + R_1^2) [L_{r1}s + R_1 - s(L_m + L_{r1})]}. \quad (9)$$

2.2.1.2.3 Superposition

From (4) and (9), since the CLLC is modeled as a linear system network, the superposition of both excitations is the sum of both components, as represented in

$$i_1 = i_{1,v_1} + i_{1,v'_2}. \quad (10)$$

After proper substitution, (10) expands into

$$i_1 = \frac{L_m s v'_2 - R_1 v_1}{L_m^2 s^2 - R_1^2}. \quad (11)$$

If the CLLC network is definitely assumed to be lossless, that is, $R_1 = R'_2 = 0 \Omega$, then i_1 is completely decoupled from v_1 and becomes solely dependent on v'_2 , as shown in

$$i_1 = \frac{v'_2}{L_m s}. \quad (12)$$

The result in (12) can also be observed in Figure 13 because at the resonance point $z_{1,2}$, v_1 has a large impedance (or a low admittance) against i_1 , whereas i_1 lags v_2 by 90° as a typical inductance.

Since steady-state behavior is being sought, the substitution $j2\pi f_r = s$ is applied to (12), resulting in

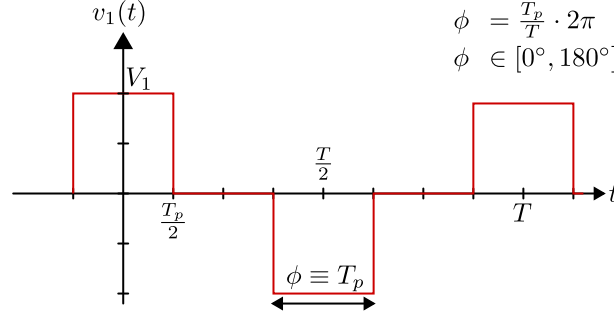
$$i_1 = -\frac{jv'_2}{2\pi f_r L_m}. \quad (13)$$

2.2.1.2.4 Fourier series decomposition of voltage waveforms

A mathematical representation of the primary and secondary voltages applied to the CLLC circuit is needed to allow for an analytical calculation of the power flow. Consider the voltage $v_1(t)$ in time-domain with peak amplitude V_1 modulated with TPS and a phase shift angle $\phi_1 = \phi$, as shown in Figure 16. This piecewise periodic function can be approximated by an infinite Fourier series as written in

$$v_1(t) = A_0 + \sum_{n=1}^{\infty} \left[A_n \cos\left(\frac{2\pi n t}{T}\right) + B_n \sin\left(\frac{2\pi n t}{T}\right) \right]. \quad (14)$$

Figure 16: Computation domain of Fourier decomposition.



The coefficients A_0 , A_n and B_n are associated with the average, even and odd components of $v_1(t)$, respectively, and their values can be calculated with the set of equations (15). Note that v_1 , as shown in Figure 16, has no DC component, since its average is zero. Moreover, the waveform has been purposely placed to be in symmetry around the ordinate axis where $t = 0$, making it a pure even function.

$$\begin{cases} A_0 = \frac{1}{T} \int_0^T x(t) \cdot dt \\ A_n = \frac{1}{T} \int_0^T x(t) \cdot \cos\left(\frac{2\pi n t}{T}\right) \cdot dt, \quad n \geq 1 \\ B_n = \frac{1}{T} \int_0^T x(t) \cdot \sin\left(\frac{2\pi n t}{T}\right) \cdot dt, \quad n \geq 1 \end{cases} \quad (15)$$

Because the average of v_1 is null and it only consists of even (cosine) components, that is, no odd (sine) components, $A_0 = 0$ and $B_n = 0$. Therefore, only A_n needs to be computed, and when all the coefficients are substituted in (14), then the closed-form continuous-time representation of v_1 is given by

$$v_1(t) = \sum_{n=1, 3, 5, \dots}^{\infty} \frac{4}{\pi} V_1 \frac{\sin\left(n \frac{\phi}{2}\right)}{n} \cos\left(\frac{2\pi n t}{T}\right). \quad (16)$$

As also discussed by [43], because this CLLC network is tuned on the switching

frequency, and as will be discussed later on the design procedures (section 2.2.2), because this CLLC circuit shows a high impedance to the harmonics of the switching frequency, the power transferred by the harmonics will be considered negligible as a means of simplification. If the power is assumed to be only transferred at the fundamental frequency, the phasor model of v_1 shall only consider the case for $n = 1$. Therefore, the phasor of v_1 is given by

$$v_1 = \frac{4}{\pi} \cdot V_1 \cdot \sin\left(\frac{\phi}{2}\right). \quad (17)$$

Similarly to v_1 , v'_2 is shown in (18), though its amplitude is from the secondary side referenced to the primary, and its phase is offset by θ , meaning v'_2 acquires an imaginary part for $\theta \neq 0$.

$$v'_2 = \frac{4}{\pi} \cdot \frac{n_1}{n_2} \cdot V_2 \cdot \sin\left(\frac{\phi}{2}\right) \cdot [\cos(\theta) + j \cdot \sin(\theta)] \quad (18)$$

Note that both v_1 and v'_2 have implicitly been assigned the pulse angle ϕ , and although each could have its own (ϕ_1 and ϕ_2) when using TPS, it would increase the degrees of freedom for the control and consequently its complexity. Since the phase shift angles ϕ and θ are the actuation control variables, there are still two degrees of freedom. According to [41], the system can be optimized for soft switching if θ is taken to be half of ϕ , such that $\theta = \frac{\phi}{2}$. Then, after substituting this relationship in (18), v'_2 is now given by

$$v'_2 = \frac{4}{\pi} \cdot \frac{n_1}{n_2} \cdot V_2 \cdot \sin\left(\frac{\phi}{2}\right) \cdot \left[\cos\left(\frac{\phi}{2}\right) + j \cdot \sin\left(\frac{\phi}{2}\right) \right]. \quad (19)$$

2.2.1.2.5 Power flow

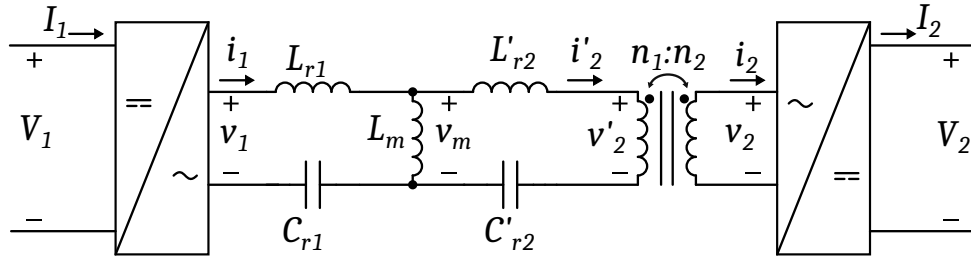
The active power flow P_1 on the primary side can be computed by the real part of the product between v_1 and i_1 , such that $P_1 = \frac{1}{2} \Re\{v_1 \cdot i_1\}$. After plugging v'_2 into i_1 and extracting the real part of it, the final power equation is found to be (20), matching the result also found by [41].

$$\therefore P_1 = \frac{8}{\pi^2} \cdot \frac{n_1}{n_2} V_2 \cdot \frac{V_1}{2\pi f_r \cdot L_m} \cdot \sin^3\left(\frac{\phi}{2}\right) \quad (20)$$

So far, a phasor model of the fundamental frequency component has been de-

veloped in order to derive a macro behavior of the CLLC RDAB converter. Because of the nonlinearities concerning the full bridges composed of switching semiconductor devices, it might at first be difficult to relate the internal AC variables (v_1, i_1 , etc.) to the external DC ones (V_1, I_1 , etc.), as depicted in Figure 17. However, assuming the energy and power are conserved, this nonlinearity may be bypassed entirely by relating the input and output of the full bridges, such that $P_1 = \frac{1}{2} \Re \{v_1 \cdot i_1\} = V_1 \cdot I_1$.

Figure 17: CLLC RDAB circuit with parameters and variable assignments.



Source: own work.

Because of the relationship $I_1 = \frac{P_1}{V_1}$, the external DC current I_1 can be given by

$$I_1 = V_2 \cdot \frac{8}{\pi^2} \cdot \frac{n_1}{n_2} \cdot \frac{1}{2\pi f_r \cdot L_m} \cdot \sin^3 \left(\frac{\phi}{2} \right). \quad (21)$$

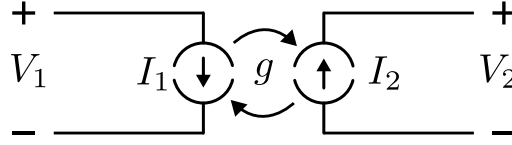
Considering the CLLC symmetry, equation (21) shows that the external current of each side depends only on the voltage of the opposite side. These mutual interactions can be represented by a two-port system defined by the set of equations

$$\begin{cases} I_1 = g \cdot V_2 \\ I_2 = g \cdot V_1 \end{cases} \Rightarrow \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & g \\ g & 0 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \quad (22)$$

The transconductance variable g , according to (23), is set by the control system via the phase shift angle ϕ , and it is a measure of how much current on one side is being demanded with a given voltage on the opposite side. These interactions are easily understandable with the equivalent circuit depicted in Figure 18, which consists of a Gyrator [44], similar to that of the conventional DAB converter.

$$g = \frac{8}{\pi^2} \cdot \frac{n_1}{n_2} \cdot \frac{1}{2\pi f_r \cdot L_m} \cdot \sin^3 \left(\frac{\phi}{2} \right) \quad (23)$$

Figure 18: Equivalent circuit model for the CLLC RDAB converter in steady-state.



Source: own work.

2.2.1.3 Dynamic Model

The CLLC network consists of two leakage inductances, one magnetizing inductance and two capacitances. Since the currents of any inductance in a T topology are a linear combination of the other inductive currents, there are only two linearly independent inductive currents, therefore, only two current states. With the other two capacitive voltages, there is a total of four states.

When deriving the CLLC linear system model, due to the AC nature of the voltage and current signals, the commonly used state-space averaging method is not suitable to represent the oscillating signals in steady-state. Instead, the dynamic phasors method [45] (also generalized state-space averaging method [46]) may be employed to decompose a sinusoidal signal into real and imaginary components, which in turn can model the sinusoidal steady-state, similarly to the DQ modelling approach [47].

One problem with the dynamic phasors method is that each AC state is decomposed into two other states (real and imaginary). This means a system of order 4 is converted into a massive system with 8 state variables, which makes the analysis much harder to be properly developed.

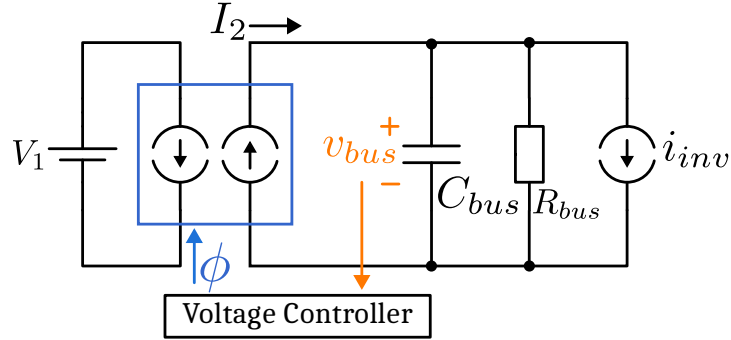
As a simpler alternative, the dynamic model developed herein will assume all the CLLC dynamics are much faster than the voltage control loop of the RC network formed by the DC bus capacitance C_{bus} and leakage resistor R_{bus} . With the CLLC response much faster than the DC bus charging dynamics, the current I_2 is expected to respond almost instantaneously given a variation in ϕ (recall equations (23) and (22)).

Figure 19 illustrates the system consisting of the battery imposing a constant voltage V_1 , an RC network and an output load current i_{inv} . R_{bus} is a large resistance whose main purpose is to safely discharge the DC bus when the converter is off.

Because of the simplifications considered above, the system presents a single energy storing element, and its state equation may be directly derived as

$$C_{bus} \frac{dv_{bus}}{dt} = I_2 - \frac{v_{bus}}{R_{bus}} - i_{inv}. \quad (24)$$

Figure 19: Equivalent circuit for the CLLC voltage control plant.



Source: own work.

The transconductance g defined in (23) can be thought of as having a maximum value G when $\phi = 180^\circ$, so (23) is rewritten for convenience as

$$g = G \sin^3 \left(\frac{\phi}{2} \right), \quad (25)$$

with

$$G = \frac{8}{\pi^2} \frac{n_1}{n_2} \frac{1}{2\pi L_m f_r}. \quad (26)$$

Now according to (22), (24) can be rewritten as

$$C_{bus} \frac{dv_{bus}}{dt} = G V_1 \sin^3 \left(\frac{\phi}{2} \right) - \frac{v_{bus}}{R_{bus}} - i_{inv}. \quad (27)$$

Considering the state variable v_{bus} and the input signal ϕ , the system is non-linear due to the $\sin^3 \left(\frac{\phi}{2} \right)$ term. A linearization is possible by taking the multivariate Taylor Series expansion around the operating point where $\phi = \Phi$ and $v_{bus} = V_{bus}$ and by analyzing the first order term, as is described by

$$\frac{dv_{bus}}{dt} \approx \phi \frac{\partial}{\partial \phi} \left(\frac{GV_1 \sin^3 \left(\frac{\phi}{2} \right) - \frac{v_{bus}}{R_{bus}} - i_{inv}}{C_{bus}} \right) \Big|_{\phi=\Phi} + v_{bus} \frac{\partial}{\partial v_{bus}} \left(\frac{GV_1 \sin^3 \left(\frac{\phi}{2} \right) - \frac{v_{bus}}{R_{bus}} - i_{inv}}{C_{bus}} \right) \Big|_{v_{bus}=V_{bus}}. \quad (28)$$

Then, the resulting linearized state equation results in

$$\frac{dv_{bus}}{dt} \approx \phi \frac{3GV_1 \sin^2 \left(\frac{\Phi}{2} \right) \cos \left(\frac{\Phi}{2} \right)}{2C_{bus}} - v_{bus} \frac{1}{C_{bus}R_{bus}}. \quad (29)$$

Recalling the value of G in (26), the Laplace transform is applied to (29), and the resulting transfer function from the phase shift angle ϕ° (ϕ in degrees) to the DC bus voltage v_{bus} is given by

$$\frac{v_{bus}(s)}{\phi^\circ(s)} = \frac{\pi}{180} \cdot \frac{3R_{bus}V_1 \sin^2 \left(\frac{\Phi}{2} \right) \cos \left(\frac{\Phi}{2} \right) G}{2(C_{bus}R_{bus}s + 1)}. \quad (30)$$

As seen in (30), the system behaves as a low-pass filter, but since the RC constant is large enough to prevent excessive discharge during normal operation, the system is likely to appear as though it were an integrator with respect to the controller.

An impulse response simulation has been performed to validate the model frequency response. This method applies an impulse perturbation on a system and its frequency response spectrum is measured.

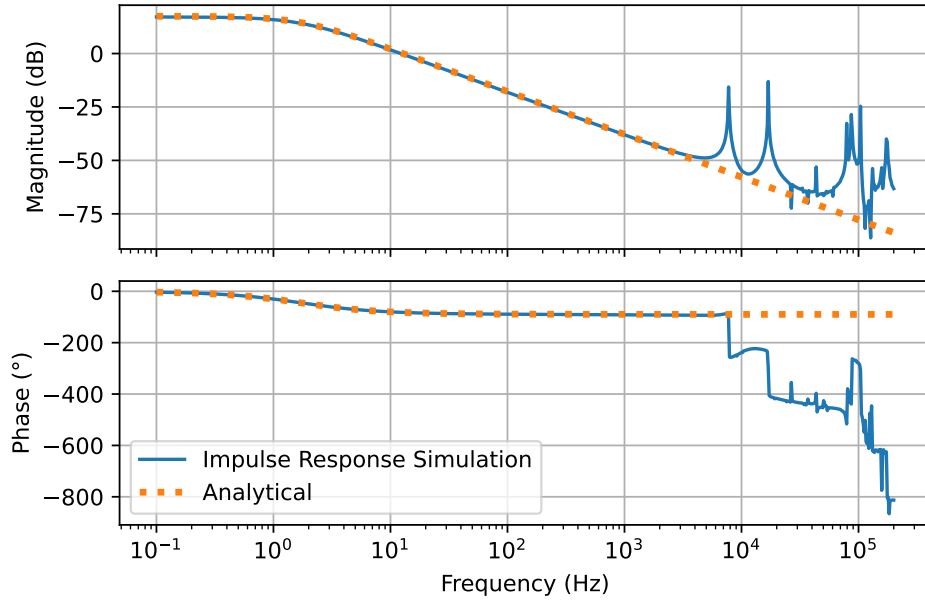
Figure 20 shows the DC bus voltage response caused by a phase shift impulse while using an ideal CLLC RDAB switched model. The simplified transfer function model is superposed as a dotted line, showing that below the kilohertz bands where the voltage control loop operates, both models neatly share the same frequency response in terms of magnitude and phase.

2.2.2 Proposed Design Procedure of the CLLC Network

When designing the CLLC RDAB converter, it is important to carefully select the values for each of the reactive elements to prevent malfunctioning or general undesired behaviors.

The aim of this Section is to propose a simple and direct reasoning pattern for quickly choosing the values of capacitances, inductances and windings ratio of the CLLC

Figure 20: CLLC RDAB voltage control plant validation.



Source: own work.

network.

Although this work focuses on TPS modulation, this methodology may apply to other fixed-frequency phase shift modulations.

Before choosing the parameters, the design procedures need some specifications as input, which will depend on the desired application. These inputs are:

- Input voltage V_1 ;
- Output voltage V_2 ;
- Optimum power P_{opt} (this will be explained later);
- Switching frequency.

A symmetry condition is applied to both the primary and secondary sides of the CLLC, such that when the secondary side parameters are referenced to the primary, they will match the parameters values on the primary side. In other words:

- $L'_{r2} = \left(\frac{n_2}{n_1}\right)^2 L_{r2} = L_{r1}$
- $C'_{r2} = \left(\frac{n_1}{n_2}\right)^2 C_{r2} = C_{r1}$

Also, the switching frequency f_{sw} must be defined beforehand, as it will serve as the basis for the dynamic behavior of the converter. The CLLC input admittance transfer function has three resonating modes: one zero and two singularities with infinite admittance. With this procedure, the zero admittance frequency should be selected to exactly match the switching frequency, as set by (31), so that the input and output admittances are cancelled at the fundamental component (high impedance). This helps reducing circulating currents at low load.

$$\boxed{f_r = f_{sw}} \quad (31)$$

The choice of switching frequency is also subject to criteria such as smaller passive components, control loop bandwidth and switching losses according to the selected semiconductor technology.

2.2.2.1 Parameters Definition

The first parameter that can be quickly selected is the windings ratio, which, as with most transformers, is used to provide voltage and current gain across a magnetic coupling. The ratio is selected according to the input-to-output voltage requirements, as defined in

$$\boxed{\frac{n_1}{n_2} = \frac{V_1}{V_2}}. \quad (32)$$

Equation (20) describes the power flow equation based on circuit parameters and operating conditions. Notice how apart from the transformer turns ratio — which is used match the input and output voltages of the converter — the only circuit parameter which affects the power flow is the magnetizing inductance L_m .

The proposed selection for L_m value is to choose an inductance value which, at a specific power P_{opt} , incurs resonant currents with the least THD, thereby minimizing reactive (conduction) power losses at this power level. This optimal harmonic distortion occurs at an angle ϕ_{opt} . The choice for P_{opt} can be based on expected average power demand (say, 80 % of nominal), or simply the rated power.

In order to find ϕ_{opt} , recall the Fourier series expansion of v_1 at (14) and (15) — which also applies to v_2' , although phase shifted — and note that the CLLC network is linear,

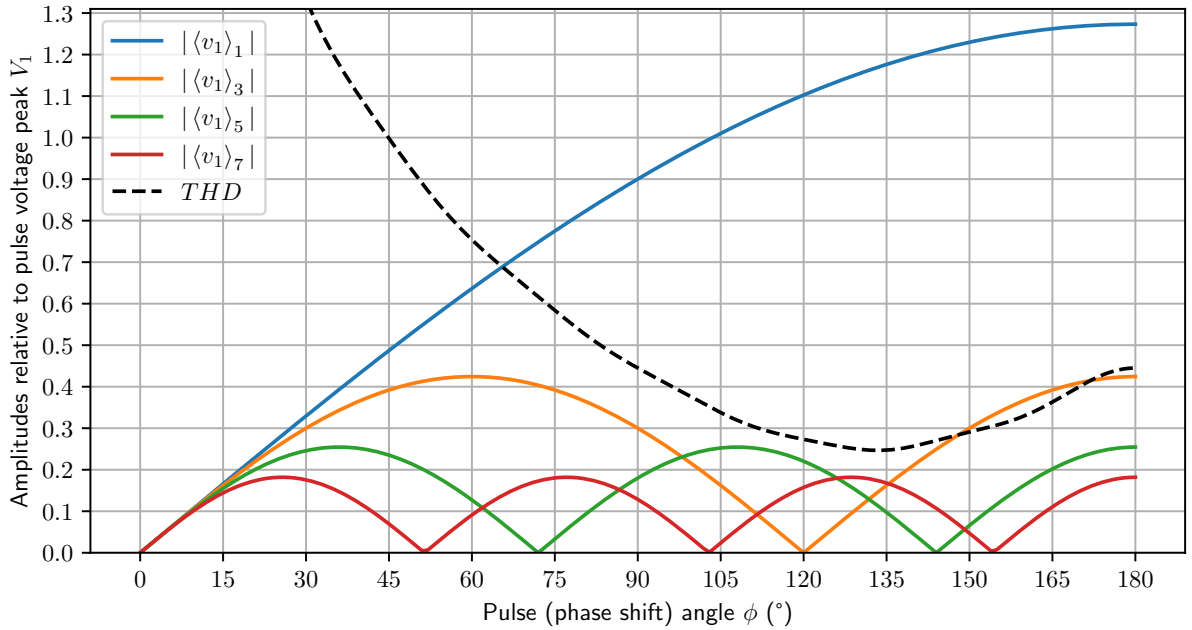
thereby making any current harmonic proportional to its respective excitation voltage.

The optimal phase shift angle ϕ_{opt} can be found by first expanding the Fourier series (14) up to a certain harmonic, such as the 13th. Then, the THD is computed with the Euclidean norm of the harmonics (that is, the square root of the sum of squares) for each value of ϕ using the equation (33), where $|\langle v_1 \rangle_n|$ is the amplitude of the n^{th} harmonic component of v_1 .

$$THD(v_1) \approx \frac{\sqrt{|\langle v_1 \rangle_3|^2 + |\langle v_1 \rangle_5|^2 + |\langle v_1 \rangle_7|^2 + |\langle v_1 \rangle_9|^2 + |\langle v_1 \rangle_{11}|^2 + |\langle v_1 \rangle_{13}|^2}}{|\langle v_1 \rangle_1|} \quad (33)$$

The calculated values of the THD and the amplitude of the harmonics are plotted in Figure 21, where the optimal angle ϕ_{opt} is found to be 131° , which minimizes the harmonic distortion on v_1 and v_2 down to 24.66 %, and consequently on the currents as well. In other words, this is the operating point where the voltage waveform, and consequently the current ones, are the most similar to a pure sine wave.

Figure 21: Family of traces for the amplitude of various harmonics of the TPS modulated voltage v_1 (some harmonics were omitted to prevent clogging). The dashed line is the THD for each angle ϕ , up to the 13th harmonic.



Source: own work.

After solving for L_m in (20) and substituting the optimum phase shift and power

defined, L_m is found by

$$L_m = \frac{8}{\pi^2} \cdot \frac{n_1}{n_2} V_2 \cdot \frac{V_1}{2\pi f \cdot P_{opt}} \cdot \sin^3 \left(\frac{\phi_{opt}}{2} \right), \text{ where } \phi_{opt} = 131^\circ. \quad (34)$$

The input lossless transfer function of the CLLC network is given by (35) and it consists of three zeros and four poles. The four poles consist of two pairs of imaginary conjugates, $p_{1,2}$ and $p_{3,4}$ which are guaranteed to be in different locations if $L_m \neq 0$. The slower poles pair is given by (36), while the faster poles pair is provided by (37).

$$Y_{eq,v_1} = Z_{eq,v_1}^{-1} = \frac{i_1}{v_1} = \frac{C_{r1}s + s^3 (C_{r1}^2 L_m + C_{r1}^2 L_{r1})}{s^4 (2C_{r1}^2 L_m L_{r1} + C_{r1}^2 L_{r1}^2) + s^2 (2C_{r1} L_m + 2C_{r1} L_{r1}) + 1} \quad (35)$$

$$p_{1,2} = \pm j \sqrt{\frac{1}{C_{r1} (2L_m + L_{r1})}} \quad (36)$$

$$p_{3,4} = \pm j \sqrt{\frac{1}{C_{r1} L_{r1}}} \quad (37)$$

One of the zeros is located at the origin of the complex plane, while the other two are a pair of imaginary conjugates whose values are given by

$$z_{1,2} = \pm j\omega_r = \pm j \sqrt{\frac{1}{C_{r1} (L_m + L_{r1})}}. \quad (38)$$

Since all inductances and capacitances are positive real numbers, the poles and zeros may be ordered on the imaginary axis according to

$$|p_{1,2}| < |z_{1,2}| < |p_{3,4}|. \quad (39)$$

As noted by [41], the leakage inductances L_{r1} and L_{r2} are required to prevent high frequency shoot-through between the capacitors, essentially adding a low-pass behavior to the CLLC circuit. This is evident by observing that L_{r1} defines the position of the poles $p_{3,4}$, which would excure towards infinity if no leakage was present.

For this reason, the value of L_{r1} can be determined by constraining the range of values accepted for $p_{3,4}$. Because $L_m > 0$, then indeed $|z_{1,2}| < |p_{3,4}|$. As already discussed, the switching frequency is set to resonate at $2\pi \cdot f_r = |z_{1,2}|$ exactly because at this frequency,

the transfer function given by (35) is zero, providing full decoupling of v_1 and i_1 , and v_2 and i_2 . However, since v_1 and v_2 have large odd harmonics, it would be unwise to select a value of L_{r1} small enough to increase $|p_{3,4}|$, thus amplifying the current harmonics (i.e., the high frequency shoot-through). With these considerations, $|p_{3,4}|$ is allowed to be set in the open interval from $|z_{1,2}|$ to $3|z_{1,2}|$.

Equation (38) is solved for C_{r1} , yielding

$$C_{r1} = \frac{1}{-z_{1,2}^2 (L_m + L_{r1})}. \quad (40)$$

When (40) is substituted into (37), then it can be solved for L_{r1} as shown in

$$L_{r1} = L_m \cdot \frac{z_{1,2}^2}{p_{3,4}^2 - z_{1,2}^2}. \quad (41)$$

If the faster poles are set in the middle between $z_{1,2}$ and $3 \cdot z_{1,2}$, such as $p_{3,4} = 2 \cdot z_{1,2}$, then (41) simplifies to

$$\boxed{L_{r1} = \frac{L_m}{3}}. \quad (42)$$

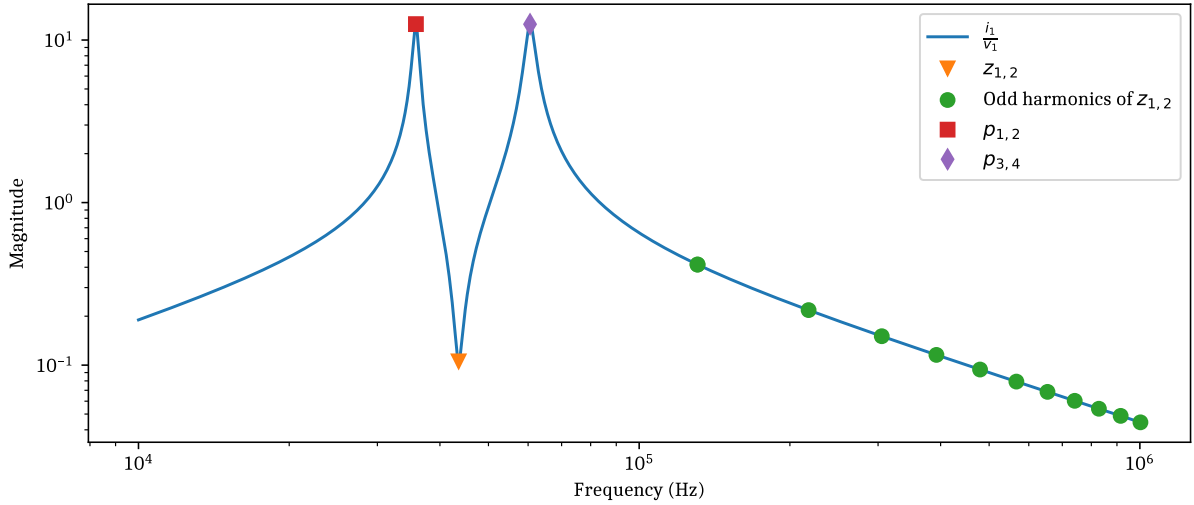
If the value of L_{r1} is set according to (42), then from the equality of the primary side inductance $L_1 = L_m + L_{r1}$, it can be observed that 1/4 of L_1 is leakage, while 3/4 is magnetically coupled with $L'_2 = L_m + L'_{r2}$, meaning the target coupling factor for the CLLC transformer is $k = 3/4$.

With the values for ω_r , L_m and L_{r1} already selected, C_{r1} may be calculated by

$$\boxed{C_{r1} = \frac{1}{\omega_r^2 (L_m + L_{r1})}}, \text{ with } \omega_r = 2\pi f_r. \quad (43)$$

Although $p_{1,2}$ is not directly used on the design, it should ideally not overlap the inverter switching frequency f_{inv} to prevent the amplification of switching noise.

Figure 22 illustrates the magnitude frequency response of (35). This plot is consistent with the constraints in (39) and with the inequality $p_{3,4} < 3 \cdot z_{1,2}$.

Figure 22: Transfer function from v_1 to i_1 .

Source: own work.

2.3 Inverter

The inverter stage is responsible for interfacing the DC bus with the grid with a combination of power semiconductors and a passive filter, which may come in many forms. The filters are usually assembled with inductors and capacitors, and sometimes damping resistors. Along with the filter topology, the modulation is also a key feature to determine the behavior of the inverter in the system. Although this conversion stage is being referred to as “inverter” because of its main operating mode, due to the required bidirectionality nature, this output stage must also be able to rectify the mains power to charge the battery bank. However, this thesis will only briefly mention the rectifying mode, and focus on the inverter operation.

This section 2.3 will discuss the working principle of the inverter, including the choice for modulation, filter and the resulting mathematical model. At the end, the design procedures are proposed for the Electromagnetic Interference (EMI) filters.

2.3.1 Working principle

The output inverter is implemented as a VSC, that is, given constant DC voltage on one side, it modulates it into a voltage waveform on the other side. This modulation, along with the output filters and the dynamic model will be discussed in details in 2.3.1.

2.3.1.1 Modulation

This type of VSC when operating with voltage control is often modulated with Pulse Width Modulation (PWM) by keeping a fixed switching frequency in some (or all) controllable semiconductors in order to shape the output waveform.

To analyze the usual types of PWM applicable to single-phase full bridge converters, [48] has performed a qualitative comparison between the Bipolar, Unipolar and a “Hybrid (totem-pole)” modulation scheme, as shown in Table 3.

Table 3: Comparison of some PWM modulation schemes for the single-phase full bridge converter.

	THD	Common-mode age current	leak-	Loss distribu- tion	Zero crossing distortion
Bipolar	Bad	Good		Good	No
Unipolar	Good	Bad (high frequency common-mode voltage)		Good	No
Hybrid	Good	Good		Bad	Yes

Source: ©2017 IEEE [48].

According to Table 3, if a good THD and no zero crossing distortion are desired, the Unipolar modulation is proved to be a fitting candidate for a choice. The Unipolar PWM provides better THD because of the three discrete voltage levels on the output which — when compared to the bipolar PWM with only two levels — better resembles a sine wave, as detailed by [49]. Therefore, this modulation has been chosen for the present work.

2.3.1.2 EMI Filters

The switching nature of modern power converter stages might exert strong electromagnetic transient stresses of both voltages and currents in terms of high dv/dt and di/dt . If left untreated, the output signals can conduct and irradiate noise to other devices, or even make the device itself susceptible to outside interference. This may cause a num-

ber of possible issues, ranging from telecommunications malfunction to semiconductors misfiring and destructive consequences due to supply surges.

To mitigate the negative side-effects of switching power converter stages, EMI filters are employed to increase the output impedance in both common and differential-modes, which causes a reduction in the conducted noise currents. Thus, this Section will discuss the adopted topology and how it influences the noise immunity for the two modes.

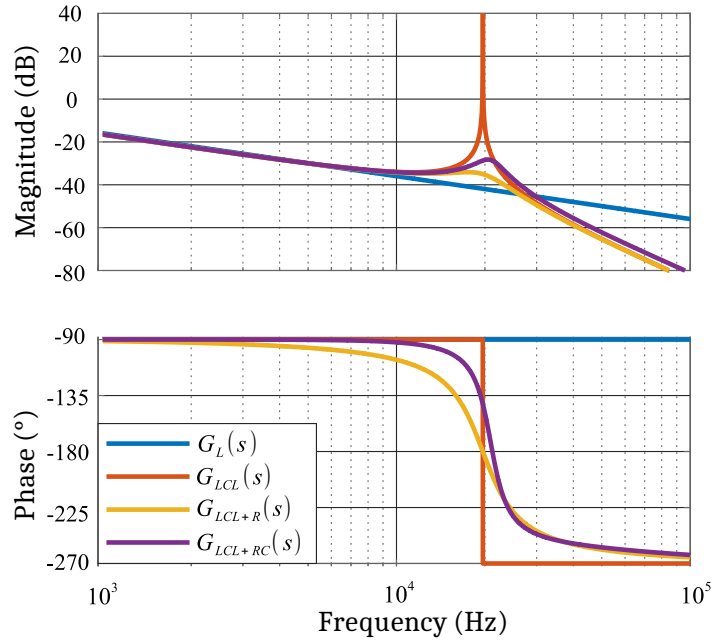
2.3.1.2.1 Differential-Mode Filter

The modulated output voltage with Unipolar PWM alternates among three different levels: $-v_{bus}$, 0 and $+v_{bus}$. Because these levels do not exactly match the grid voltage due to the presence of high-frequency components, a filter must be integrated between the inverter and the load or grid.

Ideally, this filter should have no differential impedance mode attenuation and no phase offset at the grid frequency f_g (50 Hz or 60 Hz) and infinite differential-mode impedance at the inverter switching frequency f_{inv} . Moreover, common-mode impedance should be ideally high for all the frequency spectrum.

In practice, many possible arrangements of passive elements may be used to implement these low-pass characteristics. [50] presents a comparison of four filter types, namely L, LCL, LCL+R and LCL+RC. The frequency responses of the mentioned filter topologies in terms of transadmittance (from input voltage to output current) are depicted in Figure 23.

Figure 23: Comparison of transadmittance frequency response of four possible choices for differential-mode grid filter.

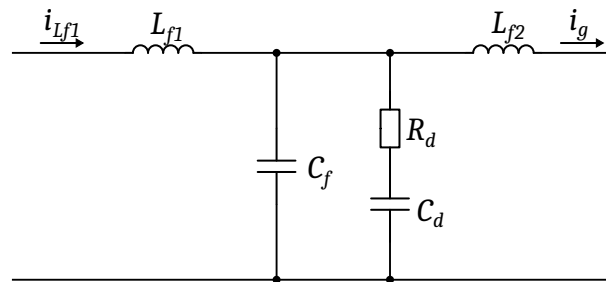


Source: own work as per [50].

At lower frequencies, they present similar output currents with the same input voltage. However, the resistive damping branch of LCL+R suffers from high power loss at f_g . At the cut-off (resonance) frequency, the third and fourth order filters increase their magnitude attenuation, while the L filter continues with the same attenuation rate, providing poorer filtering capabilities at higher frequencies. The issue with the bare LCL filter is its undamped low impedance mode, which may cause current instability.

From the presented options, LCL+RC depicted in Figure 24 has been deemed the optimal choice due to its great attenuation rate, low volume, and low damping losses [50].

Figure 24: Schematic of the LCL+RC filter topology.



Source: own work.

2.3.1.2.2 Common-Mode Filter

The LCL+RC topology as depicted in Figure 24 has been designed so far for attenuating Differential-Mode Currents (DMCs) only. However, a simple modification such as splitting L_{f1} into the two lines not only does not affect the differential-mode filtering, but also distributes the losses and provides a common-mode filtering capability.

Common-Mode Current (CMC) noise arises when two or more lines conduct current in the same direction and whose return path is not part of the intended circuit, usually through the environment, including the ground.

In the case of the full bridge inverter with unipolar modulation, a common voltage is applied at the output when either both high side or low side switches turn on at the same time, causing both the line and neutral wires to receive a common potential (from either the DC bus positive or negative electrode). This happens because the circuit nodes are coupled with the environment, such as with stray (parasitic) capacitances, which will be referred to as C_s in this text.

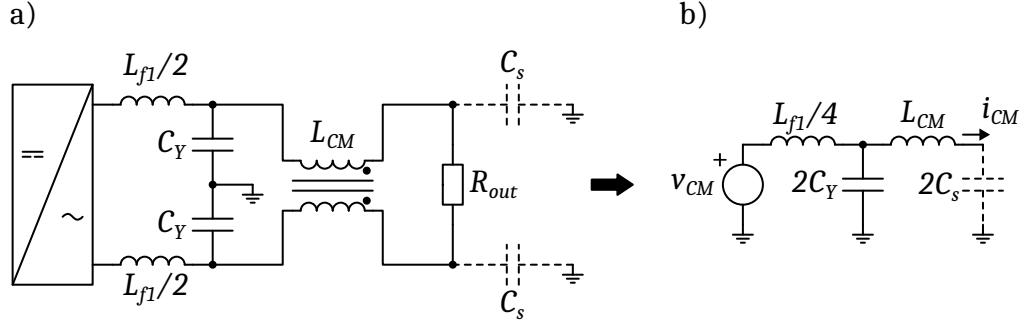
In order to mitigate the undesired effects of the common-mode noise and meet the Electromagnetic Compatibility (EMC) standards, common-mode filters are usually employed to interface power converter stages with the grid. These filters provide high common-mode impedance (balanced among all lines), and are especially important when using converters or modulation techniques which exhibit large common-mode voltages.

The full bridge inverter with unipolar modulation is susceptible to common-mode noise with amplitude $V_{bus}/2$ because when either the MOSFETs S_{31} and S_{33} or S_{32} and S_{34} (as in Figure 10) are simultaneously active, both the outputs wires (i.e., line and neutral) are connected to either the positive or negative poles of the DC bus, respectively.

Figure 25a shows the adopted common-mode filter topology with the L_{f1} inductance split into two, thus providing high common and differential impedances. A class Y capacitor C_Y — designed to fail open instead of as a short circuit — is added between each line and the ground to provide a low shunt impedance. Furthermore, a coupled common-mode (choke) inductance L_{CM} is added to the output to provide greater series impedance. The stray capacitances C_s are dashed because they do not represent actual capacitors, but rather capacitive coupling to the environment. For simplification, an equivalent common-mode circuit is derived according to [51] in Figure 25b, yielding the features of an LCL

filter.

Figure 25: Common-mode filter: a) actual topology with line and neutral; b) equivalent single-phase common-mode circuit model.



Source: own work.

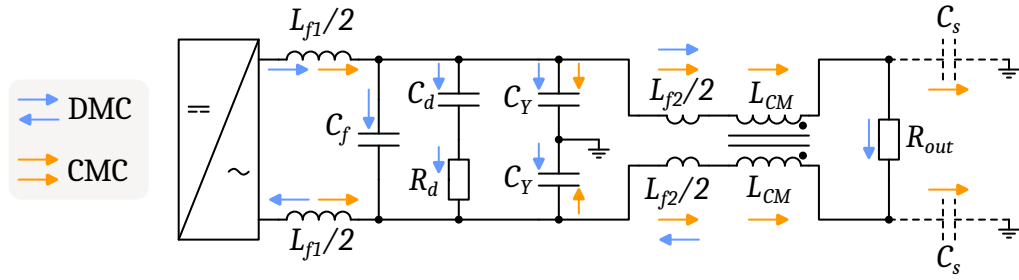
The worst case scenario for the C_s coupling would be if it were infinite ($C_s \rightarrow \infty$), which is equivalent to a short circuit to ground. In this case, the only common-mode impedance between the source and the ground would be due to the filter itself. Therefore, just as for the differential-mode filter, the common-mode filter will be analyzed in terms of its transadmittance transfer function from the input common-mode voltage v_{CM} to its output common-mode current i_{CM} , as in

$$\frac{i_{CM}(s)}{v_{CM}(s)} = \frac{1}{s^3(2C_Y \cdot L_{CM} \cdot L_{f1}/4) + s(L_{CM} + L_{f1}/4)}. \quad (44)$$

Because the coupled choke inductors match in polarity, their magnetizing inductance in differential-mode is zero. However, the ever-present leakage inductances due to uncoupled magnetic flux produce a differential-mode inductance, meaning that the output inductance of the differential filter L_{f2} has contributions from the output common-mode choke. If these contributions are deemed enough for the differential filtering, the additional L_{f2} inductor may be omitted as shown in Figure 26.

Figure 26 shows the complete filtering topology for attenuating both DMCs (represented by blue arrows) and CMCs (orange arrows). The arrows represent the elements which interact with each current mode.

Figure 26: Complete output filter with differential and common-mode elements. Each arrow color indicates whether the element interacts with DMC (blue) or CMC (orange).

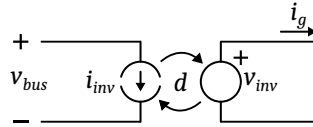


Source: own work.

2.3.1.3 Dynamic Model

By using the PWM Averaging technique, or the generalized State Space Averaging [52], a continuous-time circuit model can be found for the unipolar modulated full bridge inverter. This resulting circuit consists of two mutually dependent sources, as shown in Figure 27. Its defining equations are given by (45), which behaves as a DC transformer whose duty cycle gain d is controlled.

Figure 27: Equivalent circuit model of the PWM full bridge converter.

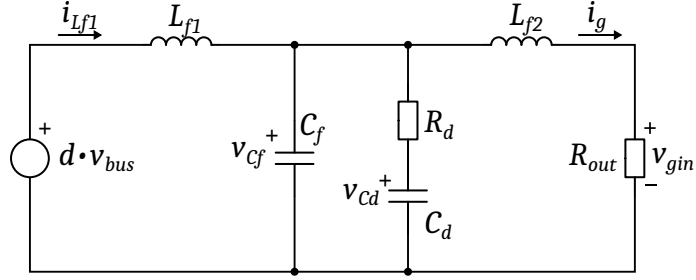


Source: own work.

$$\begin{cases} v_{inv} = d \cdot v_{bus} \\ i_{inv} = d \cdot i_g \end{cases} \Rightarrow \begin{bmatrix} v_{inv} \\ i_{inv} \end{bmatrix} = \begin{bmatrix} 0 & d \\ d & 0 \end{bmatrix} \cdot \begin{bmatrix} i_g \\ v_{bus} \end{bmatrix} \quad (45)$$

The dynamics of the output differential-mode filter is tightly related to the behavior of the inverter, so they must be considered in the overall inverter model. The common-mode filter effects will be disregarded from the dynamic model because only the differential behavior is of interest. Considering the inverter in the voltage control mode (islanded), the load connected to its output must also be considered. Figure 28 shows the equivalent linear circuit of the output when considering the filter and the load.

Figure 28: Equivalent circuit model of the inverter output with LCL+RC filter and load.



Source: own work.

From Figure 28, the state equations can be easily extracted to represent the dynamics as a set of differential equations with the duty cycle d as the input, and the voltage on the load v_{gin} as the output. Since the state equations in this case are already linear, the system can be directly described by state space matrices according to (46).

$$\begin{aligned}
 \begin{bmatrix} \frac{di_{L_{f1}}}{dt} \\ \frac{dv_{C_f}}{dt} \\ \frac{dv_{C_d}}{dt} \\ \frac{di_g}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & -\frac{1}{L_{f1}} & 0 & 0 \\ \frac{1}{C_f} & -\frac{1}{C_f R_d} & \frac{1}{C_f R_d} & -\frac{1}{C_f} \\ 0 & \frac{1}{C_d R_d} & -\frac{1}{C_d R_d} & 0 \\ 0 & \frac{1}{L_{f2}} & 0 & -\frac{R_{out}}{L_{f2}} \end{bmatrix} \cdot \begin{bmatrix} i_{L_{f1}} \\ v_{C_f} \\ v_{C_d} \\ i_g \end{bmatrix} + \begin{bmatrix} \frac{V_{bus}}{L_{f1}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot [d] \\
 [v_{gin}] &= \begin{bmatrix} 0 & 0 & 0 & R_{out} \end{bmatrix} \cdot \begin{bmatrix} i_{L_{f1}} \\ v_{C_f} \\ v_{C_d} \\ i_g \end{bmatrix} + [0] \cdot [d]
 \end{aligned} \tag{46}$$

2.3.2 Proposed Design Procedures of the EMI Filters

Although there is no single universal rule for selecting the filter parameters, it is helpful to define an objective reasoning for choosing their values because it ensures the desired requirements are met and the resulting filters are consistent. This Section will discuss the rules adopted to find the value of each inductance, resistance and capacitance.

2.3.2.1 Parameters of the Differential-Mode Filter

The selection of parameter values for the differential-mode grid-interface filter is done according to [50] and briefly summarized as follows.

The inverter side inductance L_{f1} must be select with a minimum value so that the amplitude of the high-frequency switching current is limited to the value i_{invHF} . This relationship is shown in

$$L_{f1} \geq \frac{V_{bus}}{8f_{inv} \cdot i_{invHF}}. \quad (47)$$

The capacitance values are found to work best if they are equal to each other [50]. In addition, they should be selected so that $f_{minLCLRC}$ is greater than the control bandwidth. However, the total capacitance should not generate a reactive power greater than 5 % of the nominal power P_g , according to (48).

$$C_f = C_d = \frac{1}{2} \cdot \frac{1}{L_{f1} \cdot (2\pi f_{minLCLRC})^2} \leq \frac{1}{2} \cdot \frac{5\%P_g}{2\pi f_g V_g^2} \quad (48)$$

For the grid side inductance L_{f2} , its value should be selected in a way which $f_{maxLCLRC}$ is less than the inverter's switching frequency f_{inv} , according to (49).

$$L_{f2} \geq \frac{L_{f1}}{(2\pi f_{maxLCLRC})^2 L_{f1} (C_f + C_d) - 1} \quad (49)$$

Both $f_{minLCLRC}$ and $f_{maxLCLRC}$ are respectively the minimum and maximum values for the range of possible resonance frequencies of the LCL+RC filter when the grid inductance L_g — which is in series with L_{f2} — varies from ∞ to 0, respectively.

Finally, the damping resistance R_d is selected with an optimal value which has the lowest resonance peak amplitude for all possible values of R_d . This value, as done by [53], is selected by placing the resonant pole in the geometric mean between the poles found by setting R_d to both 0 Ω and ∞ . This procedure is summarized in

$$R_d = \frac{3}{2} \sqrt{\frac{L_{f1}}{C_f}}. \quad (50)$$

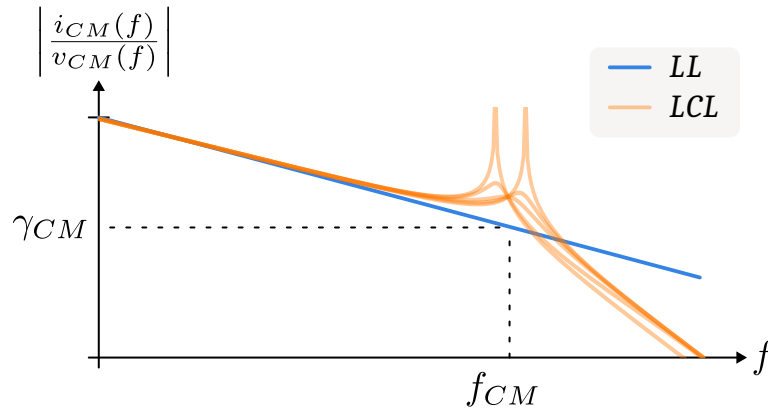
2.3.2.2 Parameters of the Common-Mode Filter

According to [54]—unlike the differential-mode filter—there are no fixed goals for the common-mode filter (as long as the standards requirements are met), except for practical requirements such as filter size, weight and prices, meaning it is impractical to design a filter with a cutoff frequency too low. Thus, in an industrial scenario, this filter could be designed by measuring the CMCs and selecting a combination of reactive components to attenuate this current.

The reasoning behind the design of the LCL common-mode filter for this work lies on the selection of a cutoff frequency f_{CM} and a target transadmittance attenuation γ_{CM} at this frequency. The transfer function of the LCL filter represented in Figure 25b is described by (44). The value for f_{CM} , as often considered by [54], might be arbitrarily set at 100 kHz . This value is small enough to mitigate EMI issues in the MHz bands, though large enough to yield a compact filter.

Suppose the class Y capacitor C_Y fails as an open circuit. In this case, only the inductive reactances would be able to filter the common-mode voltage. Therefore, this method ensures at least an attenuation γ_{CM} at the chosen cutoff frequency f_{CM} . This method is better explained visually with the help of Figure 29.

Figure 29: Graphical representation of the design procedure for the common-mode filter.



Source: own work.

From (44), if $C_Y = 0$ and $\omega_{CM} = 2\pi f_{CM}$, then the attenuation can be computed by

$$\gamma_{CM} := \left. \frac{i_{CM}(\omega_{CM})}{v_{CM}(\omega_{CM})} \right|_{C_Y=0} = \frac{1}{\omega_{CM} (L_{CM} + L_{f1}/4)}. \quad (51)$$

A value for the transadmittance attenuation γ_{CM} (in A/V) must be set to limit the common-mode current in case of failure of the capacitor (and assuming the worst case scenario where C_s is a short circuit). For instance, if a full bridge with a 400 V DC bus must limit the common-mode current components to 1 A (in the spectral interval $[f_{CM}, \infty]$), then $\gamma_{CM} = 1/400$. With these considerations, the inductance for the common-mode choke is found by

$$L_{CM} = \frac{1}{\omega_{CM} \cdot \gamma_{CM}} - \frac{L_{f1}}{4}. \quad (52)$$

For the resulting LCL topology, the cutoff frequency found by the complex poles pair is given by (53). Then, the needed capacitance C_Y is calculated by solving for it, as shown by (54). After adding C_Y , the attenuation rate increases from -20 dB/dec to -60 dB/dec, ensuring little high frequency common-mode noise will pass through.

$$\omega_{CM} = \pm \sqrt{-\frac{L_{f1}/4 + L_{CM}}{2C_Y \cdot L_{f1}/4 \cdot L_{CM}}} \quad (53)$$

$$C_Y = \frac{L_{f1}/4 + L_{CM}}{2 \cdot \omega_{CM}^2 \cdot L_{f1}/4 \cdot L_{CM}} \quad (54)$$

If necessary, a damping resistance may also be added to a damping branch (recall the LCL+RC topology) to suppress the amplitude gains near the resonant frequency f_{CM} . [53] suggests choosing an intermediary resistance value which lowers the resonant peak amplitude relative to the extreme values of 0 Ω and ∞ . This quick calculation can be done by solving

$$R_{d,CM} = \frac{3}{2} \sqrt{\frac{L_{f1}/4}{2C_Y}}. \quad (55)$$

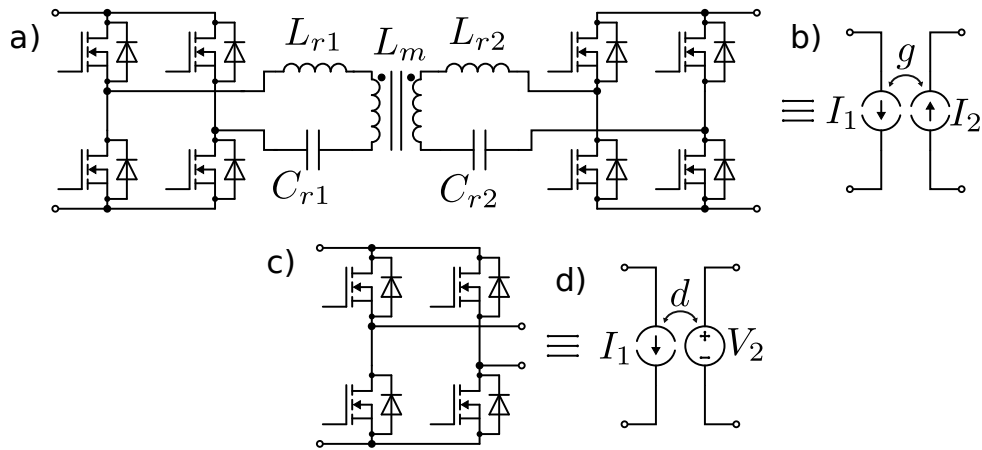
2.4 Control architecture

After designing the power electronics topology for the converter, it is essential to develop the control strategies to maintain the required operating conditions of the whole system. For this reason, chapter 2.4 will discuss the general control structure in low and high level of abstraction.

For the development of the control systems, the power electronics circuits can be

simplified into a set of simple mutually dependent sources according to Figure 30. This simplification removes the high frequency switched components and only considers the slower averaged dynamics.

Figure 30: Equivalence between the switched and the large-signal equivalent circuit models.

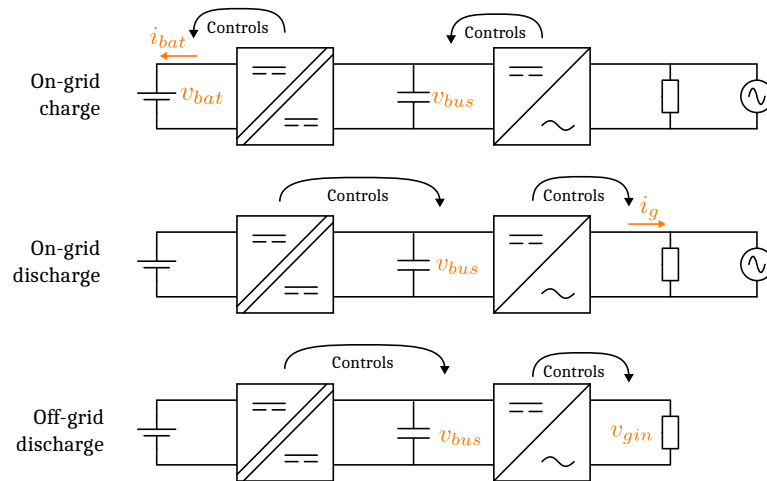


Source: own work.

2.4.1 Overview

This UPS device was conceived to operate in three possible modes: on-grid charge, on-grid discharge and off-grid discharge. Each of these modes has their own set of controlled variables and objectives, as depicted in Figure 31. The following subsections will explore and detail the characteristics of each.

Figure 31: High level control strategy depending on operating mode.



Source: own work.

In this thesis, only the off-grid discharge mode has been validated with the built prototype. However, the remaining modes could be implemented by future works.

2.4.2 On-grid charge mode

The on-grid charge mode, as the name suggests, is responsible to charge the battery while connected to the distribution grid. It is characterized by the control of the battery current i_{bat} and voltage v_{bat} —as seen in Figure 31—according to the charge profile.

Because the CLLC RDAB converter is the one controlling the battery variables as its output, it needs a stable input voltage from the DC bus. The inverter (which in this case operates as a rectifier) is assigned to control the DC bus voltage v_{bus} and allow the operation of the CLLC.

In order to properly test and validate this operation mode in hardware, ideally either a battery bank or a battery-emulating bidirectional DC supply should be used on the input of the CLLC. Because of the added complexity to validate this scenario in actual hardware, this mode has been left for future works.

2.4.3 On-grid discharge mode

If the UPS is connected to the grid and the power flow direction reverses to dispatch stored energy from the battery, it operates in the on-grid discharge mode. As shown in Figure 31, the battery is assumed to have a fixed voltage serving as input for the CLLC converter, which then controls v_{bus} . With v_{bus} stable, the inverter is able to control i_g to inject power in the fixed-voltage grid.

This mode can be useful to promote energy trade by storing energy when the prices are low and dispatching when high, effectively contributing to load shifting. Moreover, if the output control is implemented as grid-forming and is adopted in large scale, it may greatly benefit the distribution grid by providing grid support functionalities, such as voltage and frequency regulation, which could in turn improve overall system stability.

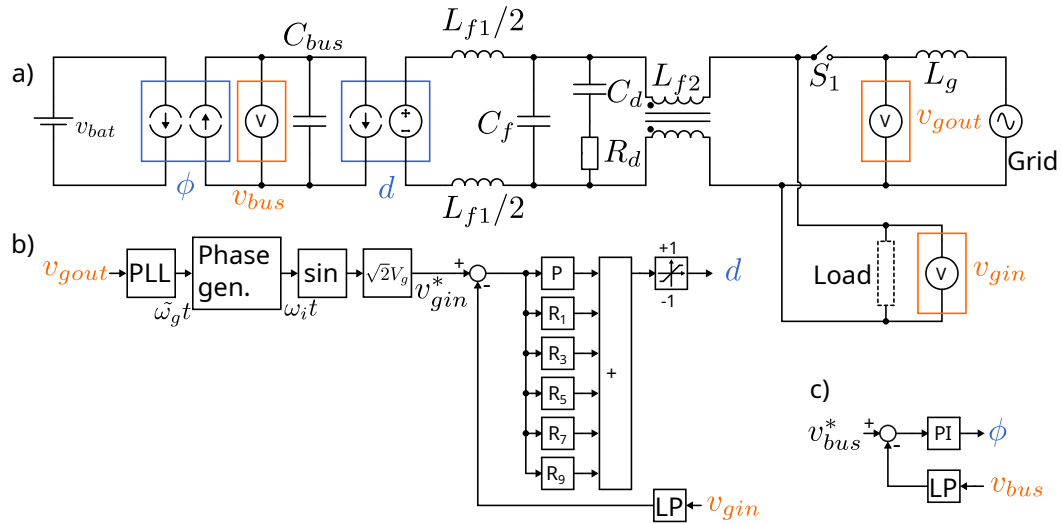
However, this mode is not an essential nor priority feature of an UPS, since the main objective is to guarantee the operation of local critical loads. Because of this and the complexity to test in the hardware prototype, the implementation and validation of this mode has been disregarded on this work. When the grid is available, the converter will idle until there is a need to restore and maintain the load, either due to an outage or other

issues regarding power quality.

2.4.4 Off-grid island mode

The most important operation mode for an UPS is the off-grid discharge, which offers a mean to protect and resume the energy delivery to essential critical loads. As was seen in Figure 31, the CLLC in this mode is responsible to maintain the DC bus voltage stable, while the inverter forms an isolated (islanded) grid by controlling the output internal voltage v_{gin} , and by opening the switch S_1 to isolate the load from the grid, as better detailed in Figure 32a.

Figure 32: Control architecture: a) Equivalent average circuit model; b) Island voltage control loop with harmonics suppression and synchronization algorithm; c) DC bus voltage control loop.



Source: own work.

The off-grid control mode utilizes two control systems:

- DC bus voltage control;
- Output AC voltage control.

This mode usually stands by when the grid is present and its operating conditions are nominal (in terms of voltage and frequency). Only when there is an issue, such as overvoltage, overfrequency, undervoltage, underfrequency or an outage, does the off-grid discharge mode control begins.

2.4.4.1 DC Bus Voltage Control

Figure 32c shows the control structure of the DC bus voltage control. It consists of a simple PI controller which tracks the constant reference voltage v_{bus}^* . In addition, a low pass filter is added to the feedback path to prevent measurement noise in v_{bus} from disturbing the control action.

The control action signal is the phase shift angle ϕ which, according to equation (23), is related to the CLLC RDAB transconductance g , which in turn is proportional to the current I_2 .

2.4.4.2 Inverter Control

In the inverter stage, the control structure is a combination of both a grid-following current controller with Phase Locked Loop (PLL) to track the grid reference voltage, and a grid-forming voltage controller. However, as already mentioned, the on-grid current control modes have been omitted on the present work.

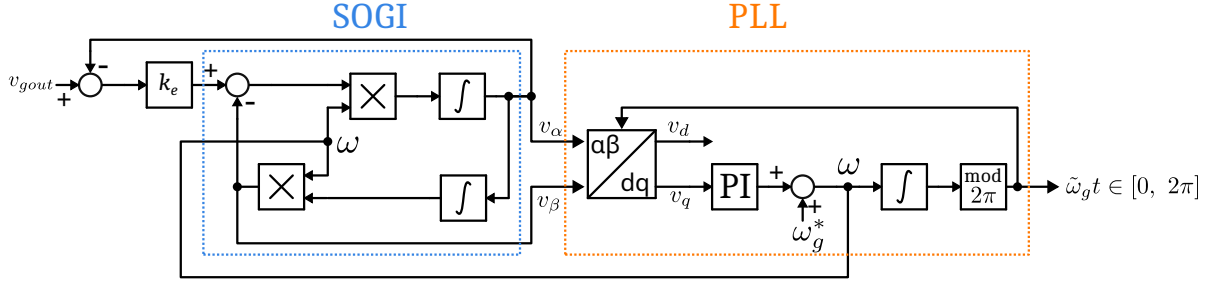
When the PLL is synchronized to the grid and the operating conditions are within the correct ratings, switch S_1 is closed in Figure 32a. When the grid requirements are not met, S_1 opens and the voltage control maintains the islanded grid.

2.4.4.2.1 PLL

The PLL is the component responsible for extracting the grid frequency and phase given its measured signal. It was implemented with a Second-Order Generalized Integrator (SOGI) structure, which generates two orthogonal signals in the $\alpha\beta$ (stationary) reference frame to be fed into the PLL itself [55].

A PLL in the dq (rotating) reference frame was used to synchronize the input phase of $v_{gin}(\omega_g t)$ with its estimated value $\tilde{\omega}_g t$. This is accomplished by applying a PI controller to bring the quadrature component v_q to zero, which results in the input signal phase being synchronized with the $\alpha\beta$ -dq transform angle in steady-state.

Figure 33: Diagram representing the SOGI-PLL structure, which is used to synchronize the inverter reference with the grid.



Source: own work.

2.4.4.2.2 Phase Synchronization

The phase synchronization module receives from the PLL the estimated grid phase reference $\tilde{\omega}_g t$ corresponding to the fundamental frequency component and is responsible for generating the reference phase for the inverter $\omega_i t$. Unlike a conventional grid-tie inverter, which follows the grid phase at all times, an UPS needs to be able to have its own phase reference. In this case, since the output voltage v_{gin} might be either on or off-grid, its phase must be generated according to the presence or absence of the grid.

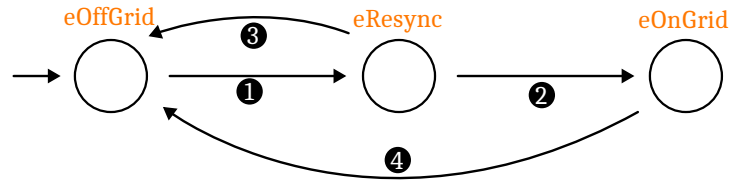
This module is controlled at a higher level by the Finite-State Machine (FSM) shown in Figure 34, which dictates the operating strategy at any given moment. The states are eOffGrid, eResync and eOnGrid.

The default state on initialization is eOffGrid. This state generates an independent phase reference used by the inverter to form a voltage on the output bus when the grid is not in an acceptable operating condition or when this condition has not been yet measured (as is the case during initialization).

The second state is eResync, which also occurs when the inverter is operating off-grid. When entering this state, the generated reference phase (which was independent) starts to gradually resynchronize with the estimated grid phase $\tilde{\omega}_g t$.

When resynchronization has been achieved, the system arrives in the eOnGrid state. In this state, the inverter simply follows the estimated grid phase $\tilde{\omega}_g t$ with no further processing. The state transitions are described in Table 4.

Figure 34: FSM of the phase synchronization module.



Source: own work.

Table 4: State transitions of the phase synchronization FSM.

State transition	Description
1	The transition from eOffGrid to eResync is triggered once the measured grid conditions are deemed safe to restore the supply from the grid (i.e., voltage and frequency in the permissible interval).
2	When in eResync state and the difference between the grid's and the inverter's phases is small enough (below a certain threshold), plus the grid is zero-crossing, the resynchronization is triggered and the FSM transitions to eOnGrid, causing the physical reconnection to the grid.
3	If the grid conditions are insufficient to meet the requirements while in the eResync state, the FSM automatically transitions back to eOffGrid.
4	During normal grid-tie operation, if an event such as overvoltage, under-voltage, overfrequency or underfrequency occurs, the FSM transitions back to eOffGrid and the loads are isolated from the grid.

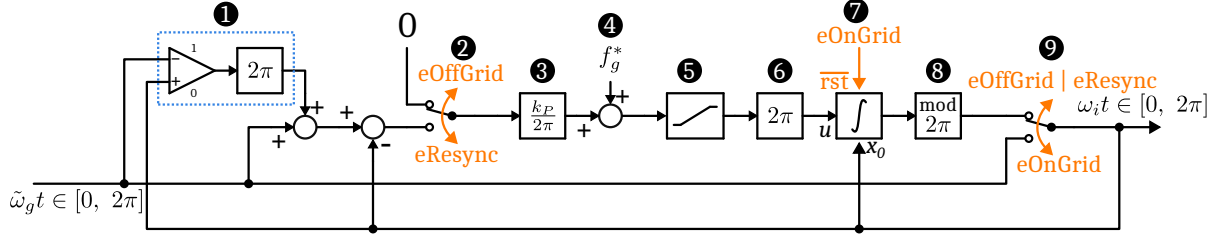
Source: own work.

Based on the states and transitions seen in Figure 34 and on Table 4, the signal processing structure is represented in Figure 35, which shows the block diagram of the resynchronization algorithm depending on the connection state.

Figure 35 depicts the input signal $\tilde{\omega}_g t$ from the PLL branching off into three different paths, two of which are used when the UPS is physically disconnected from the grid (eOffGrid or eResync), and one when it is connected (eOnGrid). Table 5 provides in-depth

explanations on the marked components.

Figure 35: Block diagram of the phase synchronization module.



Source: own work.

Table 5: Components of the phase synchronization block diagram.

Component	Description
1	Because both the input $\tilde{\omega}_g t$ and the output $\omega_i t$ are limited to the interval $[0, 2\pi]$, when for instance $\tilde{\omega}_g t$ is leading $\omega_i t$ and it wraps from 2π back to 0, suddenly $\tilde{\omega}_g t$ lags $\omega_i t$. This phenomena would cause the system to misbehave due to oscillations because the input would not be able to be tracked, as the input would constantly appear to be oscillating around the output value. This would not be an issue if the phases were allowed to increase in ramp.
2	This switch selects the control error (phase difference), given by $\tilde{\omega}_g t - \omega_i t$ during resynchronization, and considered zero in off-grid operation to prevent unintended controller action when the grid is out.
3	The controller issues an action signal based on the control error. In this case, a proportional control with conversion from Hz to rad/s suffices for the purpose, although an integral action would also be possible.
4	A feed forward with the grid nominal frequency f_g^* (i.e., 50 or 60 Hz) is summed after the control action to make it the default frequency during initialization and off-grid operation, when no control action is performed.

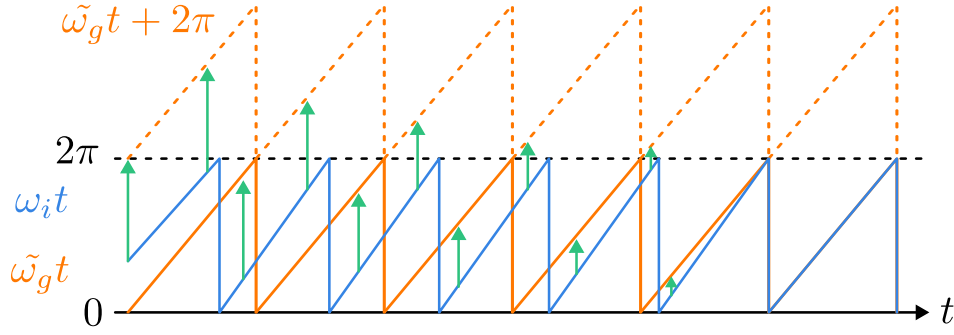
Continuation of Table 5

Component	Description
5	The resulting variable frequency is limited around f^* to avoid causing issues to the load.
6	The frequency in Hz is converted to radians per second.
7	An integrator is used to transform the computed frequency (from the input “u”) into a phase for the inverter. However, when the state is eOnGrid, the integrator is reset by the $\overline{\text{rst}}$ input with the value of current output phase ω_{it} , which is fed through the “x ₀ ” port as reset value (initial value).
8	To wrap the potentially infinite phase into the interval $[0, 2\pi]$, the modulo operator is symbolically represented in the diagram. In practice, using the modulo is inefficient in actual code, thus a programmatically solution with branching instructions might be preferred.
9	The final step consists in choosing the inverter phase based on the current state. If connected to the grid, its phase is simply the same as the grid’s. Otherwise, the inverter phase results from the presented control system.

Source: own work.

The resulting phase synchronization is represented in Figure 36, where $\tilde{\omega}_g t$ develops at constant rate along the time axis t , and ω_{it} slowly converges to it. In the time instants where $\omega_{it} > \tilde{\omega}_g t$, the controller setpoint is incremented by 2π to maintain the convergence on the same ascending direction. This prevents output oscillations when the phases are limited to the interval $[0, 2\pi]$ in practical finite precision digital systems.

Figure 36: Qualitative representation of the phase synchronization control.



Source: own work.

2.4.4.2.3 Proportional Multi Resonant Controller

In the event of a power outage, the UPS shall resume the power supply to the attached loads as quickly as possible, and the steady-state operation of this load without the grid strength might be challenging depending on the load type.

If the load is linear and highly reactive, a larger out-of-phase current must be supplied to exchange energy with the capacitances and/or inductances. However, if the load is non-linear, not only might the fundamental current component be larger, but other current harmonics might be requested by the load, such as when a filtered full bridge rectifier draws a pulsed current only at small time intervals of the grid cycle.

Because these current harmonics request pulsed current from the inverter, a voltage drop of v_{gin} can be observed during the pulses intervals, which creates voltage harmonics as well. If the voltage harmonics are left untreated, they may interfere with adjacent loads and degrade their performance if they are sensitive to grid distortions.

Therefore, this work also implements a Proportional Multi Resonant (PMR) voltage controller, whose task is not only to generate the off-grid voltage in the fundamental frequency f_g , but also to suppress low order odd voltage harmonics, such as $3f_g$, $5f_g$, $7f_g$ and $9f_g$.

Both of these objectives may be achieved by designing a controller with high gain for each of these harmonic frequencies, including the fundamental. The PMR controller has been selected because it performs the best in comparison with other common linear controllers in the stationary reference frame, as shown in Figure 37. Each of these controllers has been tuned to operate near the edge of stability with the inverter, LCL+RC filter and a

resistive load, as defined by the system in (46).

The Proportional controller yields the worst result, since it provides very little gain at the desired frequencies when operating at the edge of stability. Although the PI controller provides higher gains at lower frequencies than the Proportional, its phase offset in the closed loop system is relatively poor because it narrows the phase margin. The Band Pass filter controller is able to provide even more gain at the harmonic frequencies, but just as the previous ones, it has little tuning capability of each harmonic individually. Notice that a control implementation is also possible in the rotational reference frame, but each harmonic would need its own reference frame transformation [56], which would require much more signal processing power from an MCU.

The PMR controller is formed by the sum of a proportional term K_p with the resonant transfer functions $C_{R_k}(s)$, as represented by (56). Each of the $C_{R_k}(s)$ terms correspond to the resonant frequency with harmonic index k , according to (57), where ω_{bw_k} is the bandwidth around each resonance peak centered at ω_k , and K_{r_k} is the gain at each peak such that $C_{R_k}(j\omega_k) = K_{r_k}$.

In the open loop frequency response of Figure 37, it is noteworthy that the PMR controller achieves the highest gains at the desired harmonic frequencies, including the fundamental, while also providing low amplitude gain to other non-harmonic frequencies. This happens due to its high rate of frequency-dependent gain variation (dB/dec).

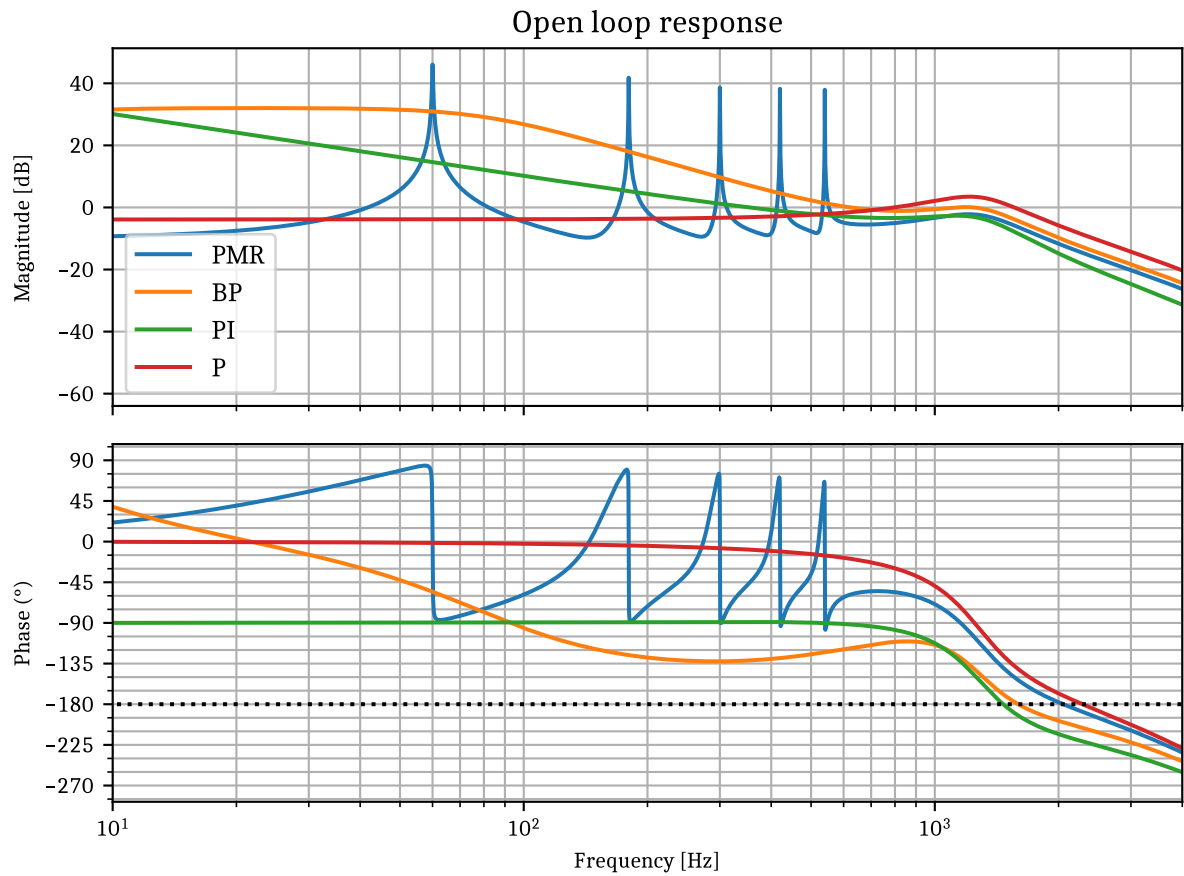
One disadvantage of the PMR control is the increased design and implementation complexity caused by the larger number of tunable parameters. Moreover, its high order transfer function increases the probability of numerical errors when computing the system response as a whole. A solution for this in a practical digital environment consists of calculating the signal processing of each second-order resonant branch separately and then summing them at the end, instead of processing the whole equivalent transfer function.

A discrete implementation of a Proportional Resonant (PR) controller is presented in Appendix C, which can be used to build the PMR controller.

$$C_{PMR}(s) = K_p + \sum_{k=1,3,5,7,9} C_{R_k}(s) \quad (56)$$

$$C_{R_k}(s) = \frac{K_{r_k} \cdot 2 \cdot \omega_{bw_k} \cdot s}{s^2 + 2 \cdot \omega_{bw_k} \cdot s + \omega_k^2} \quad (57)$$

Figure 37: Bode diagram of the open loop transfer function near stability limit with selected controllers.



Controllers legend: PMR=Proportional Multi Resonant, BP=Band Pass filter (start frequency not shown), PI=Proportional Integral, P=Proportional.

Source: own work.

3 Prototype

So far, this thesis has presented an overview on UPS and their topologies, as well as the commonly utilized power converter topologies, especially from a theoretical point of view regarding their working principle, design methodologies, control scheme, etc.

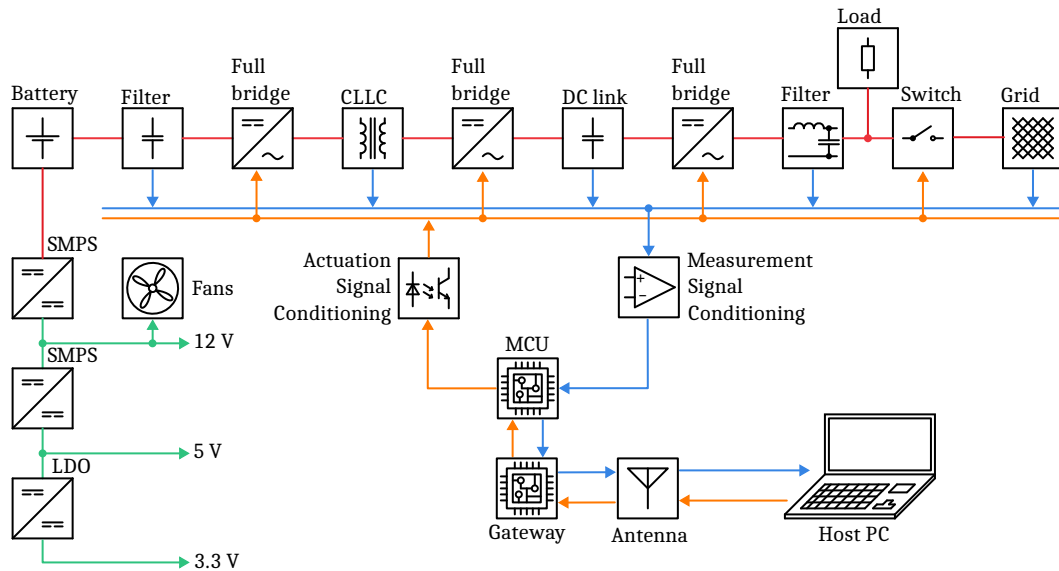
This Section will briefly discuss the practical implementation aspects of the developed prototype, namely Powerlink, which was used to verify the studied concepts, before moving on to the experimental results in section 4.

3.1 Hardware Development

The Powerlink consists of a Printed Circuit Board (PCB) containing all the power stages from the battery to the grid interface and the auxiliary components, such as those in signal conditioning stages, Switched-Mode Power Supply (SMPS), Microcontroller Units (MCUs), including some in thermal dissipation and structural mechanics.

The diagram in Figure 38 shows how the main components are interconnected in terms of power coupling and signal communication.

Figure 38: Powerlink hardware block diagram.

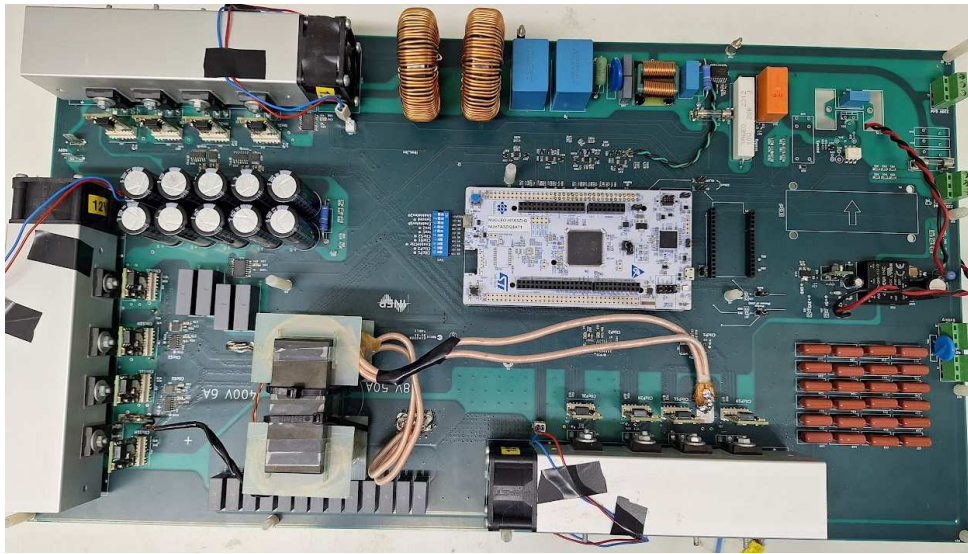


Source: own work.

The battery voltage is used to power the secondary circuits with 12 V, 5 V and 3.3 V outputs used for many auxiliary components.

Measurements are taken from sensors located in regions with stabilized voltages and currents, amplified, filtered for anti-aliasing and redirected to the MCU. Conversely, commanding signals such as those used to control the converters with PWM, Triple Phase Shift Modulation (TPSM), digital enables and relays are emitted from the MCU and distributed throughout the PCB. The manufactured PCB prototype with soldered components is depicted in Figure 39.

Figure 39: Powerlink PCB with soldered components.



Source: own work.

3.1.1 Semiconductors

This project intended to increase power density by utilizing high-frequency switching modulations, thereby reducing the sizes and costs of magnetic cores and capacitors. Due to the increased switching frequency, switching losses become a major concern for selecting semiconductor devices. To keep smaller switching losses and low cost, Si MOSFETs were chosen for the power stages due to their short turn-on and turn-off times. Conduction losses are also an important concern in semiconductors, thus low on-resistance MOSFETs should be preferred.

The CLLC transformer magnetically couples the lower voltage and higher voltage sides, which correspond to the battery side and grid side, respectively. This difference in voltage and current requirements means two set of power switches need to be selected

3.1.1.1 Lower Voltage Switches

For the lower voltage side, the 150 V N-Channel MOSFETs FDH055N15A from onsemi were employed to establish a low loss stage at the CLLC converter. With a nominal value of $R_{DS(on)} = 4.8 \text{ m}\Omega$ at $I_D = 120 \text{ A}$ and $V_{GS} = 10 \text{ V}$, it provides very low conduction losses which is especially important for the lower voltage / higher current side.

Also, the turn-on and turn-off times of 102 ns and 92 ns at the same conditions plus an external gate resistor of $R_G = 4.7 \text{ }\Omega$ and $V_{DS} = 75 \text{ V}$ ensure a quick transition between conducting and blocking states, resulting in low switching losses.

3.1.1.2 Higher Voltage Switches

The 600 V IPW60R070C6FKSA1 MOSFET from Infineon Technologies was selected for the higher voltage side (for both the CLLC and the inverter). An $R_{DS(on)}$ of up to $70 \text{ m}\Omega$ at $I_D = 25.8 \text{ A}$ and $V_{GS} = 10 \text{ V}$ suffices for the higher voltage / lower current conditions.

With turn-on and turn-off times of 28 ns and 88 ns at $V_{DS} = 400 \text{ V}$ and $R_G = 1.7 \text{ }\Omega$, the switching losses can also be very well limited.

3.1.2 Capacitors

Many capacitors of different types were used in the power processing stages for different purposes, such as for decoupling one stage from the other, output filtering, or creating the CLLC circuit resonance characteristics. The most important capacitors are briefly described under this section.

3.1.2.1 CLLC network

The CLLC network requires the capacitors to withstand bipolar voltages (that is, their technology cannot have polarization constraints, such as with many electrolytic capacitors).

Moreover, the high switching frequency and large currents require low Equivalent Series Resistance (ESR) and a stable frequency-dependent impedance.

Because of these reasons, and to maintain an acceptable cost, Polypropylene film capacitors were chosen for the CLLC network.

3.1.2.1.1 Primary Side

Due to the high frequency and high amplitude currents on the primary side of the CLLC network, a bank of 13 parallel 220 nF 400 V capacitors with Part Number (PN) R75MI322050H3J from KEMET were selected, with an ESR of 10.9 m Ω and an Root Mean Square (RMS) AC current rating of around 2.5 A at 50 KHz each.

3.1.2.1.2 Secondary Side

For the secondary side, a 2 series 2 parallel bank with the 39 nF 2 kV R76UN-23905050J capacitors from KEMET were chosen. They present a 16.3 m Ω ESR and can withstand an RMS AC current of up to 4.5 A each.

3.1.2.2 DC Bus

The DC bus is the structure which needs the most capacitance of all others in order to sustain enough voltage while decoupling the DC side power flow from the AC one. Because its voltage is always with the same polarity, polarized capacitors such as aluminum electrolytic may be selected to fulfill the requirements. Using this technology, high power density and comparatively low cost are achieved, though at the expense of filtering capability at frequencies.

The DC bus was built using a set of ten 100 μ F 500 V 20 % 500HXW100MEFR-18X45 capacitors from Rubycon, which offer a good balance between performance and cost.

3.1.2.3 Input Filter

The primary side full bridge of the CLLC stage drains large pulsed currents with a fundamental frequency of f_{sw} from the input DC voltage source (battery). Due to the line impedance connecting the two points, large voltage drops would incur if no filtering was

present. The input capacitive filter is therefore able to decouple the DC source from the high frequency switched AC load.

The filter was built with twenty-four ECW-FD2W105J polypropylene film capacitors from Panasonic, whose ratings are $1\ \mu\text{F}$ 450 V 5 %, and show a low impedance at the required frequencies.

3.1.2.4 Output Filter

At the LCL+RC output filter, two $4.7\ \mu\text{F}$ 630 V 10 % polypropylene film X2 class capacitors from EPCOS-TDK (B32924D3475K000) were chosen to provide grid rated AC filtering capability.

3.1.3 Magnetic Components

3.1.3.1 Output Differential-Mode Filter

A set of two 0076256A7 toroidal cores from Magnetics with a permeance (inductance factor) of $35\ \text{nH per turn}^2$ were used for the differential-mode output filter. Its Kool M μ material consists of distributed gap powder core and provides low losses against high frequencies, and a saturation flux density of up to 1 T.

3.1.3.2 CLLC Transformer

The CLLC transformer was designed with purposely built-in controlled leakage inductances (L_{r1} and L_{r2}). This is possible by selecting a gapped E core, such as the B66387Q0100K187 from EPCOS-TDK, and by adjusting the spacing between both core pieces, thereby creating flux paths which do not couple the primary and secondary sides (leakage flux). More details can be seen in Annex A.

The selected core consists of the N87 material and has a permeance of $100\ \text{nH per turn}^2$. This relatively low permeance is important to facilitate the adjustments of the desired total inductances of both sides (L_1 and L_2).

3.2 Software Development

Nowadays, software plays an essential role to bring great flexibility and capability to the development of power electronics solutions. With advances in the underlying digital hardware such as MCUs, modern digital electronics is capable of offering smaller development and testing time thanks to its faster iteration cycles. Furthermore, the development of many control techniques and processing speeds are hardly achieved using the analog counterparts with the needed reliability, and sometimes are not even feasible.

The MCU is therefore the central hub for data processing in the Powerlink prototype, responsible for reading the measured signals, and for applying the needed signals to regulate the behavior of the power stages.

For the purpose of providing a stable and safe environment to collect data, control and debug the experimental tests, a complete structured software framework has been developed to increase system reliability and to provide insights on the internal working conditions.

3.2.1 Control Firmware

An MCU is a hardware component containing embedded memory for storing instructions and runtime data, a Central Processing Unit (CPU) for executing the instructions, reading from and writing to data memory, and peripherals, which are specialized sub-circuits used to perform various tasks, such as Input/Output (IO) signals management, generating time references, performing complex computation, manipulating memory, etc.

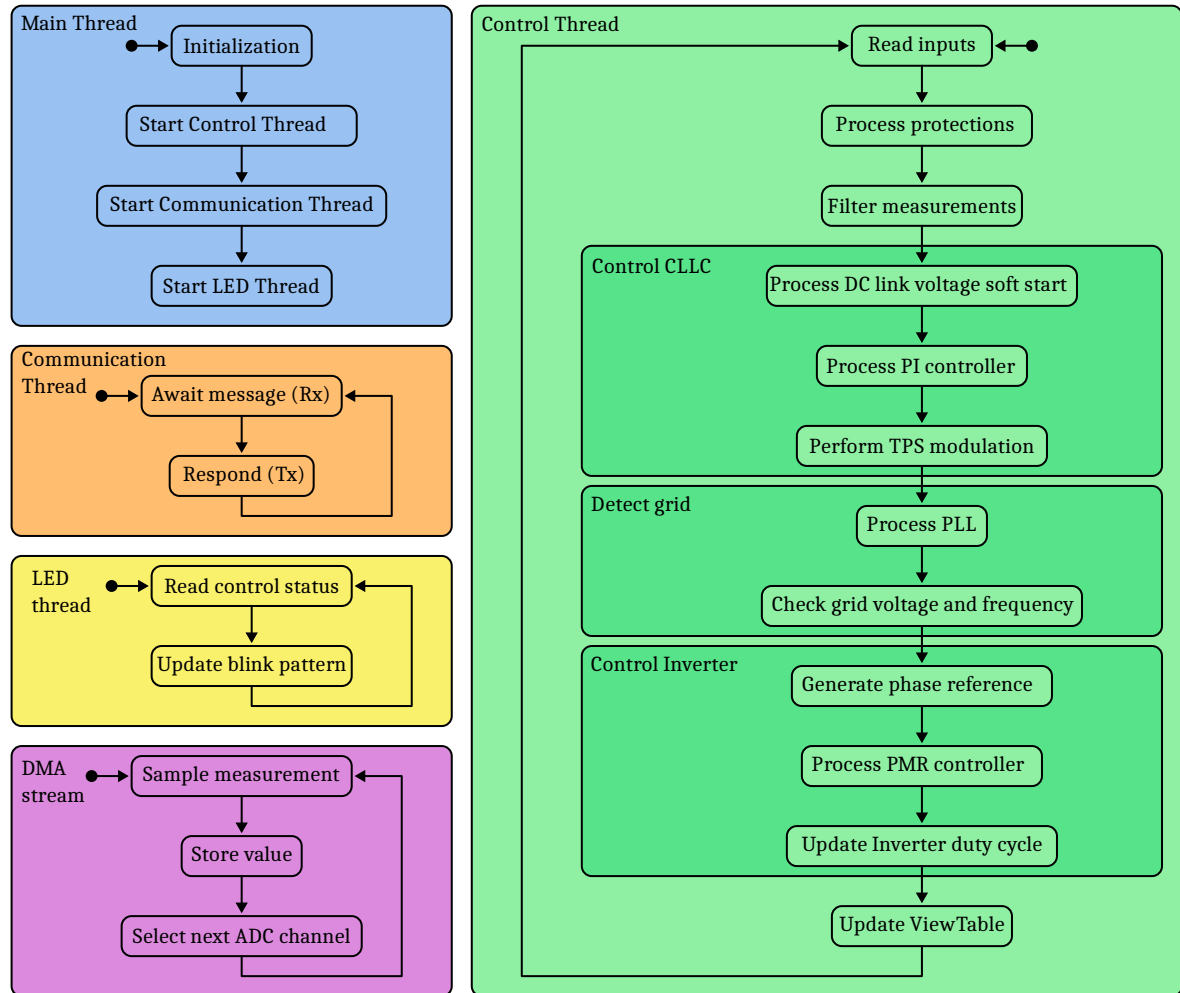
The MCU is responsible for sampling the analog continuous-time measurements and converting them to discrete-time digital signals with its Analog-to-Digital Converter (ADC), filtering the noisy signals, processing the feedback control systems, including the PI and PMR controllers, and finally setting the output signals in the form of PWM and TPSPM for the gate drivers, and the relay commands.

Moreover, a special memory region called `ViewTable` has been allocated to store the measurement values, general status and protection flags, which assert the safe operation of the Powerlink. The `ViewTable` can then have its data queried by an external host, providing an easy solution for data logging.

The diagram in Figure 40 depicts the most important processing groups being executed by the CPU. An STM32H7 has been selected to perform these tasks due to its high

processing power, large pin counts, flexible timers and accurate ADC.

Figure 40: Firmware control loop.



Source: own work.

The main thread is the entry point responsible for initializing the other threads. At first, the control thread is initialized, and then it repeatedly processes the input signals, passing them to the power stage control loops. After each of the CLLC and Inverter controllers, the corresponding modulations are performed, and at the end, relevant data is stored in the ViewTable. Because of its critical importance to the correct operation of the power circuits, this thread has the highest priority and consistently runs at a fixed rate thanks to an interrupt signal.

The communication thread has lower priority and also runs at a (lower) fixed rate interrupt. Its responsibility consists of waiting for a serial UART command, which is validated, processed and then responded if needed.

A simple fail-safe status display is provided by the LED thread, which simply interprets the current system status (i.e., idle, running, stopped) and encodes it into a three LEDs pattern. Instead of using an interrupt, this thread is served by the main thread.

Finally, the Direct Memory Access (DMA) stream continuously triggers ADC conversions from all channels and stores the results in a fixed memory buffer for the control thread to read from. Thanks to its special hardware implementation, no CPU time is used to move the converted values from the ADC peripheral to the memory buffers.

3.2.1.1 Measurements

Analog data acquisition is converted into digital signals with a 16-bit successive approximation ADC[57]. Each of the 6 multiplexed channels is given 810.5 ADC clock cycles to stabilize the voltage of the sampling capacitor, and after 7.5 more cycles to finish the conversion, a total conversion time of 2921.4 ns is elapsed for each of the 6 samples with a 280 MHz system clock.

To improve flexibility and reduce processing time, all the memory transfer operations were performed with the DMA peripheral to offload the CPU.

3.2.1.2 Protection Flags

A set of 12 bits (expandible up to 32) were used to signalize if the power conversion system is allowed to run. If any single bit is set, the controllers immediately stop, put the outputs in safe state, reset all control variables, and the Powerlink is blocked until the complete system is manually reset.

Because all the protection flags lie within a single 32-bit CPU word, a single instruction is able to manipulate and assert all the flags at once. All implemented flags are presented in Figure 42.

3.2.1.3 Control loops

The signal control loops responsible for regulating the power stages are processed sequentially, as seen in Figure 40. They were developed initially in the continuous-time-domain, and then discretized using the bilinear transform with a sampling rate of 20

kHz.

The generalized implementation using C macros is presented in Appendix B, which is able to define and process systems of any feasible order. The PMR controller was developed using this technique, and its definition is presented in Appendix C.

3.2.1.4 Low level drivers

The higher level software implementation notes presented in this thesis provide a wide-picture of what was accomplished in the development of this work. A flexible and noteworthy foundation for the development of the STM32 code was the `modm` [1] toolbox, which offers the capability to generate a rich library of peripheral drivers implemented with abstraction features of C++, improving readability, optimizing execution speed, automating tedious boilerplate code, and making the resulting program much safer and less error-prone.

3.2.2 Remote Control Framework

The possibility of having direct and precise control over the hardware is helpful to reduce development iteration times, increase operation safety and decrease the need to constantly flash the firmware to update internal parameters.

With the addition of real-time data acquisition of internal variables, the remote control framework turns out to be a great tool to solve many of the development and testing issues.

3.2.2.1 Uart—UDP bridge

As seen in Figure 38 and Figure 40, the communication thread in the STM32 MCU is constantly waiting for incoming messages from the Gateway, which is implemented with an ESP32. This gateway consists of a communication bridge between serial Universal Asynchronous Receiver-Transmitter (UART) and User Datagram Protocol (UDP), enabling the seamless bidirectional byte-to-byte conversion between wired Tx/Rx asynchronous serial messages into Internet packets.

Moreover, the embedded ESP32 Wi-Fi antenna provides a wireless path to con-

nect to the Host Personal Computer (PC), which offers a fast and safe interconnection, preventing possible damages to the Host PC due to surges and noise.

3.2.2.2 Data Logging with TLV

A monitoring system consisting of real-time measurements and other internal variables acquisition was implemented to facilitate the understanding of the underlying operation, provide faster feedback and reduce the need for constant monitoring with oscilloscopes.

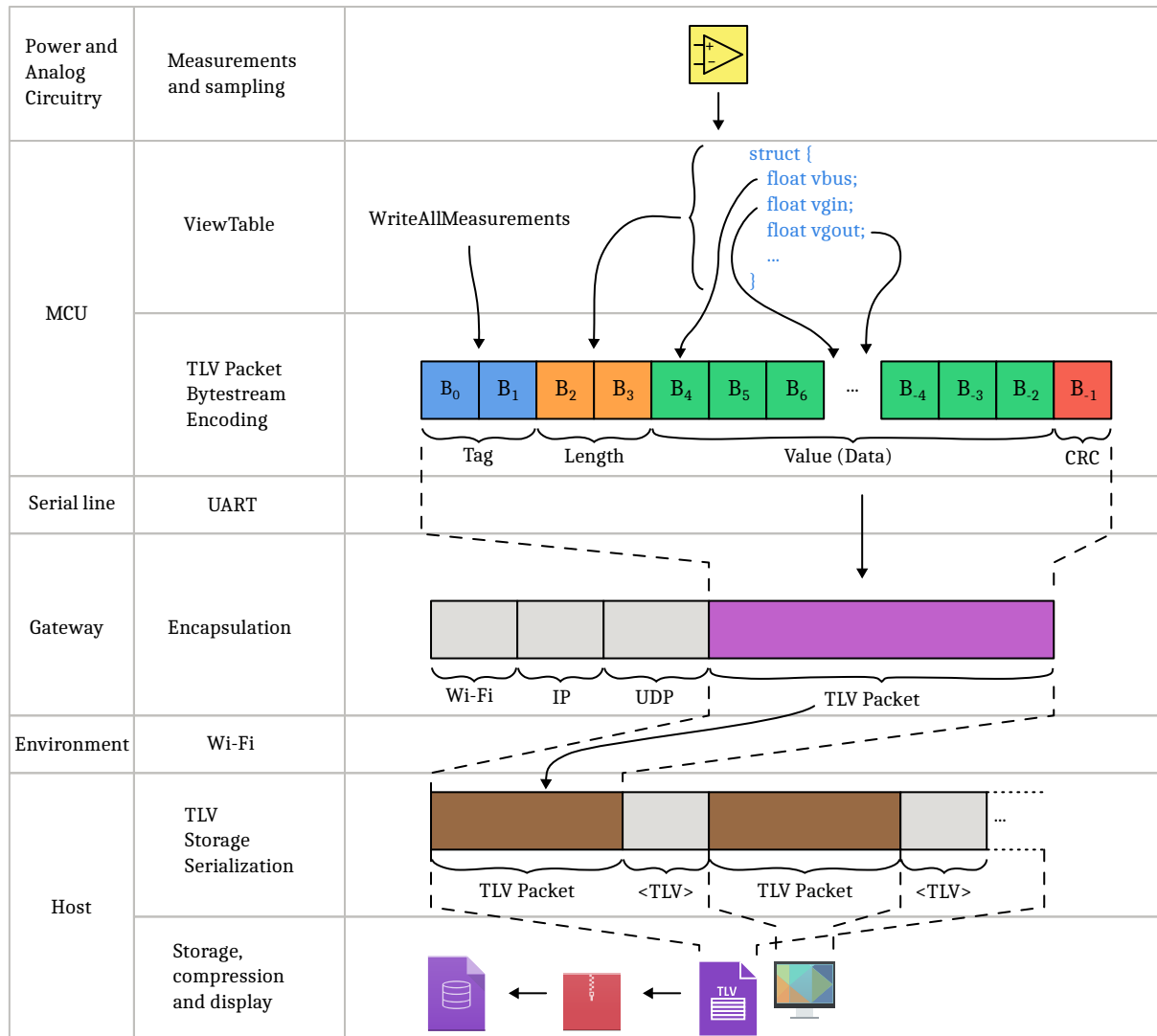
The achieved data sampling rate for all the 10 float variables, 10 bool flags, a uint8_t version number and a uint64_t timestamp (which in total add up to 53 bytes in the ViewTable), varies from 60 to 90 Hz, which although is nowhere near what can be accomplished with an oscilloscope, can provide meaningful insights on the power conversion behavior due to the high number of analog signals, flags and digital data.

All variables to be transmitted are internally stored in the ViewTable structure, which is encoded upon request into a Tag (or Type) Length Value (TLV) packet, as shown in Figure 41. The TLV packets use 2 bytes to encode the Tag (or Type) and length of the encapsulated data, which in this case is the binary stream of the ViewTable contents formatted as little endian. At the end of the TLV frame, a Cyclic Redundancy Check (CRC) byte is appended to allow for data corruption assertion.

The TLV packet is then forwarded to the gateway, which encapsulates it into a nested structure of Wi-Fi, Internet Protocol (IP) and UDP protocol frames.

When arriving at the Host PC, each TLV packet is decoded and displayed on the control Graphical User Interface (GUI). Moreover, the packets are serialized into a binary .tlv file, compressed and when needed, can be transcoded into a SQLite database file for post-processing.

Figure 41: Real-time measurements transmission flowchart.



Source: own work.

3.2.2.3 Control Interface

The Control GUI is a PC software programmed to interface the Powerlink remotely with the user, both in terms of inputs and outputs (IO).

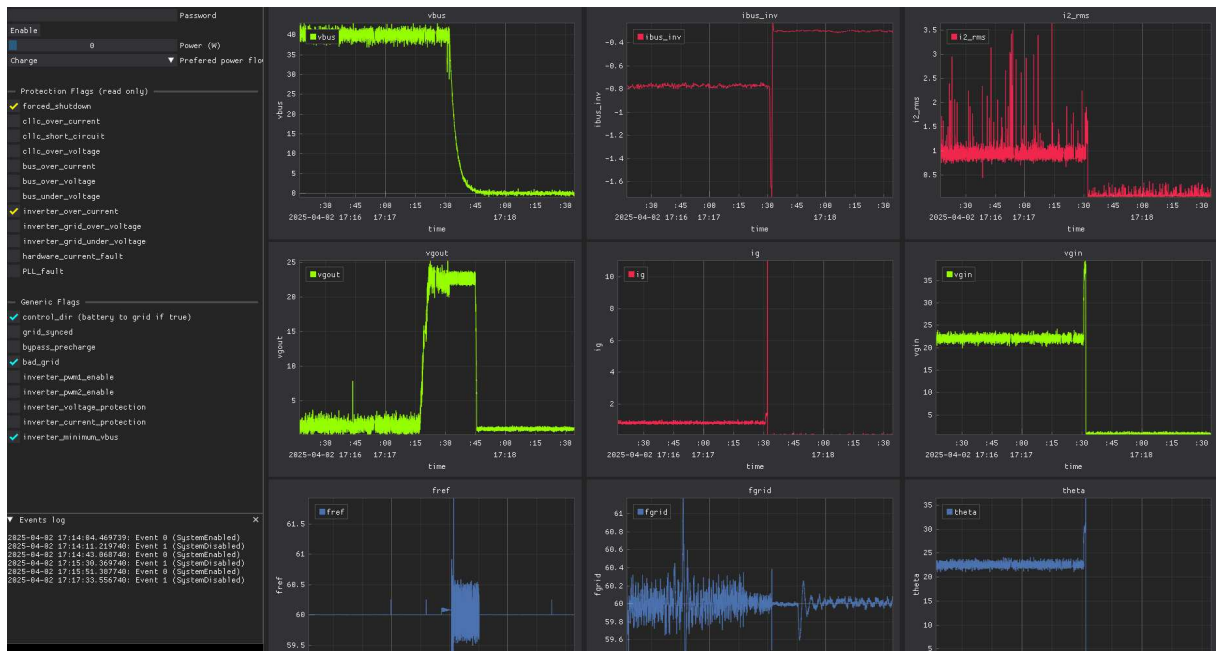
The GUI is the only method developed to start the power converter stages. This, together with a password protection, has been done as a safety measure to prevent accidental turn on by forcing the user to actively unlock it.

When the program is started, it sends a time synchronization command to update the MCU's internal time reference, and as soon as it succeeds, the data stream begins and the analog variables are plotted in real-time, as shown in Figure 42. The protection flags,

along with the generic flags, are displayed as boolean variables with check marks, which represent important status information.

The communication and data logging infrastructure has been an important tool to improve the safety and the quality of the prototype testing, validation and debugging. It helped provide complex internal state variables instantly and effortlessly, while also allowing for powerful post-mortem analysis of unsuccessful tests.

Figure 42: GUI window with real-time measurement and control.



Source: own work.

4 Experimental Results

The experimental tests with the prototype were performed to evaluate its capability of achieving similar results acquired by computational simulations.

The procedures to design the CLLC network parameters in 2.2.2 as well as the differential-mode filter parameters from 2.3.2.1 provide a direct way of estimating the optimal configuration with the given specifications. The resulting numerical values used in the prototype are listed in Table 6.

Table 6: Passive elements parameters.

Parameter	Value
$L_{f1}/2$	$920 \mu H$
L_{f2}	$30 \mu H$
C_f	$4.7 \mu F$
C_d	$4.7 \mu F$
R_d	22Ω
C_{bus}	$920 \mu F$
C_{bat}	$24 \mu F$
L_m	$2.24 \mu H$
L_{r1}	$2.42 \mu H$
n_2/n_1	$400V/48V$
L_{r2}	$167.82 \mu H$
C_{r1}	$2.86 \mu F$
C_{r2}	$39 nF$

Similarly, the control system parameters listed in Table 7 were selected to provide a trade-off between safe and stable operation, and fast response.

Table 7: Control systems parameters.

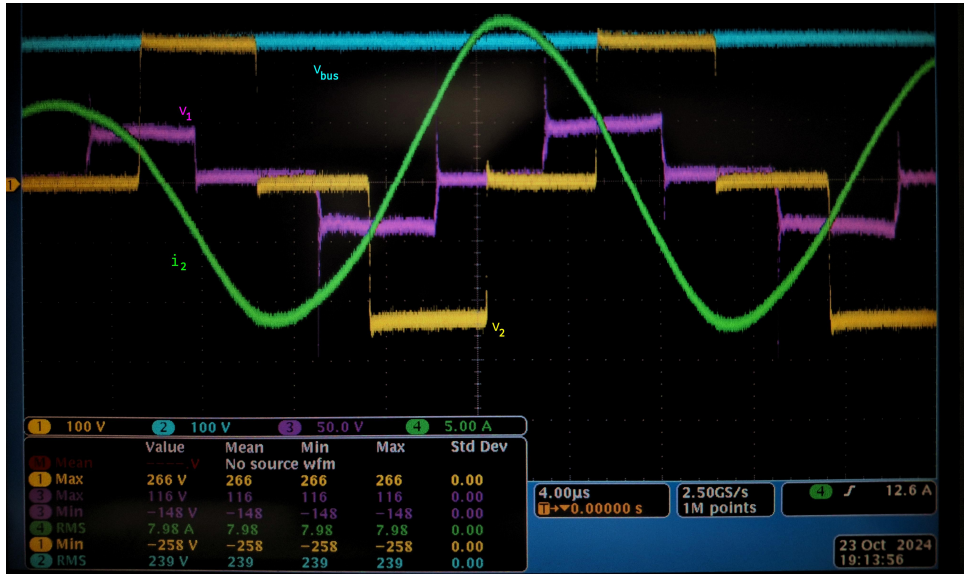
Parameter	Value
PMR: K_p	$8 \cdot 10^{-4}$
PMR: K_{r_1}	0.5 V^{-1}
PMR: K_{r_3}	0.3 V^{-1}
PMR: K_{r_5}	0.2 V^{-1}
PMR: K_{r_7}	0.18 V^{-1}
PMR: K_{r_9}	0.16 V^{-1}
PMR: ω_{bw_k}	$2\pi \cdot 0.1 \text{ rad/s}$
PI: K_p	1° V^{-1}
PI: K_i	10° V^{-1}
v_{bus} 2 nd order LP cutoff	100 Hz
v_{gin} 2 nd order LP cutoff	6 kHz

4.1 CLLC RDAB

The CLLC high frequency waveforms resulting from a phase shift of around $\phi = 90^\circ$ were recorded to verify the correct voltage and current behaviors when driving a resistive load of 146Ω attached to the DC bus. Figure 43 shows the primary and secondary CLLC full bridge voltages v_1 (pink) and v_2 (yellow), as well as the secondary current i_2 (green) and the DC bus voltage (cyan).

It is possible to note that the phase shift θ between v_1 and v_2 is indeed half of ϕ , and that the CLLC network is able to filter out most current switching harmonics. Moreover, because i_2 and v_1 are of opposite sides, they are ideally orthogonal to each other, as was derived in equation (13).

Figure 43: CLLC RDAB converter waveforms.



Source: own work.

4.2 Inverter

To validate the behavior of the PMR controller, experimental tests were performed with a non-linear load formed by a single-phase diode rectifier with an input inductive filter and an output capacitive filter in parallel with the resistive load.

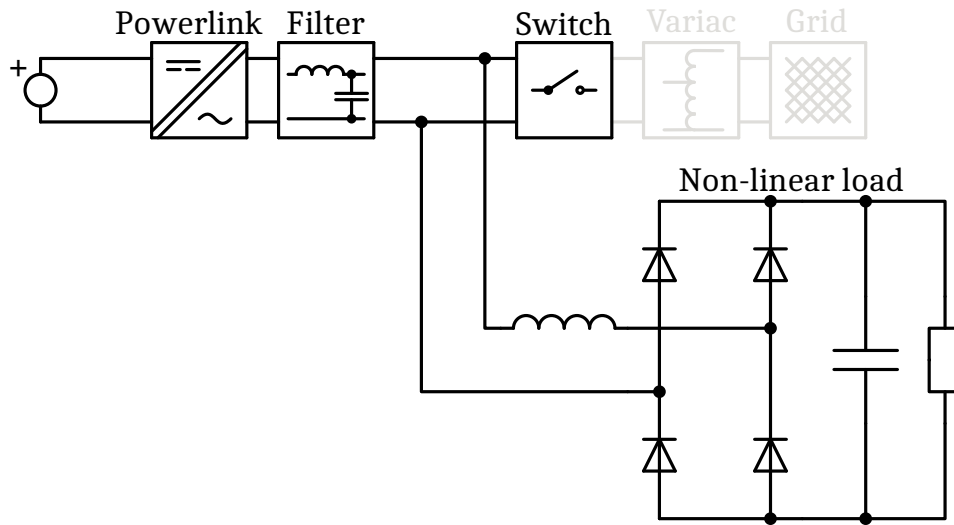
Because the load's filter capacitors are rated to a DC voltage of 250 V, the nominal phase voltage must have a peak amplitude lower than this value.

In addition to the non-linear load tests, the connection and disconnection tests were performed with linear resistive loads.

4.2.1 Initial test with lower-order harmonic compensation

This introductory test evaluates the islanded grid formed by the inverter operating with the PMR control. For this test, the parameters for the inverter and the load are listed in Table 8 and the representing schematic is depicted in Figure 44.

Figure 44: Test setup schematic for the non-linear load harmonic compensation.



Source: own work.

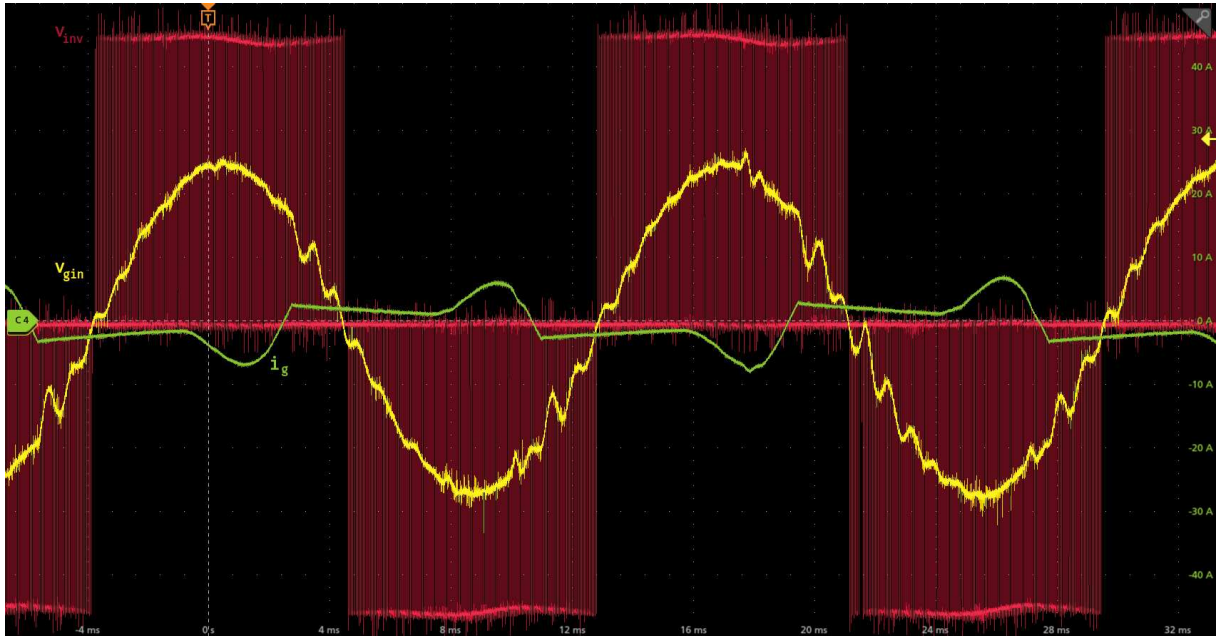
Table 8: Parameter values for the non-linear load test.

Parameter	Value
Load resistance	64 Ω
Capacitive filter	2,3 mF
Inductive filter	2,4 mH
AC RMS voltage	90 V
AC fundamental frequency	60 Hz

Source: own work.

Figure 45 shows the pulse width modulated voltage v_{inv} in red, the filtered voltage v_{gin} in yellow and the resulting current i_g in green.

Figure 45: Inverter in islanded mode with unipolar PWM supplying a non-linear load. Voltages are 50 V/div and current is 10 A/div.



Source: own work.

The distortion caused by the abrupt interruption of the rectifier current (as represented by i_g) can be readily seen as additional harmonics on top of the nominal grid frequency f_g . This distortion in v_{gin} is caused by the interaction of this rough current waveform and the LCL+RC filter.

4.2.2 Comparing the effects of the PMR control

For this test, the voltage has been increased, as shown in Table 9. The objective now is to compare the inverter with and without the harmonic compensation of the PMR controller.

Table 9: Parameter values for the non-linear load test.

Parameter	Value
Load resistance	64 Ω
Capacitive filter	2,3 mF
Inductive filter	2,4 mH

Continuation of Table 9

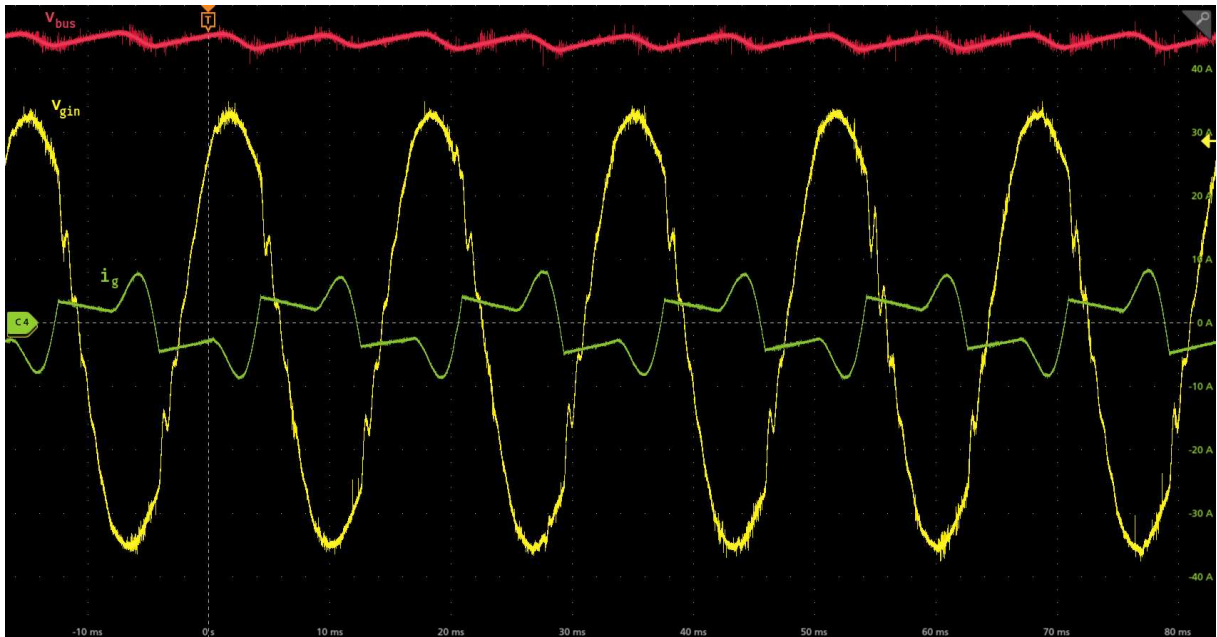
Parameter	Value
AC RMS voltage	127 V
AC fundamental frequency	60 Hz

Source: own work.

The first case shown in Figure 46 considers the non-linear load with uncompensated harmonics. In this case, instead of v_{pwm} , the red channel traces v_{bus} , whose 120 Hz component can be clearly seen.

When compared to the last scenario with 90 V (Figure 45), there is a noticeable improvement in waveform quality if the control settings are kept the same.

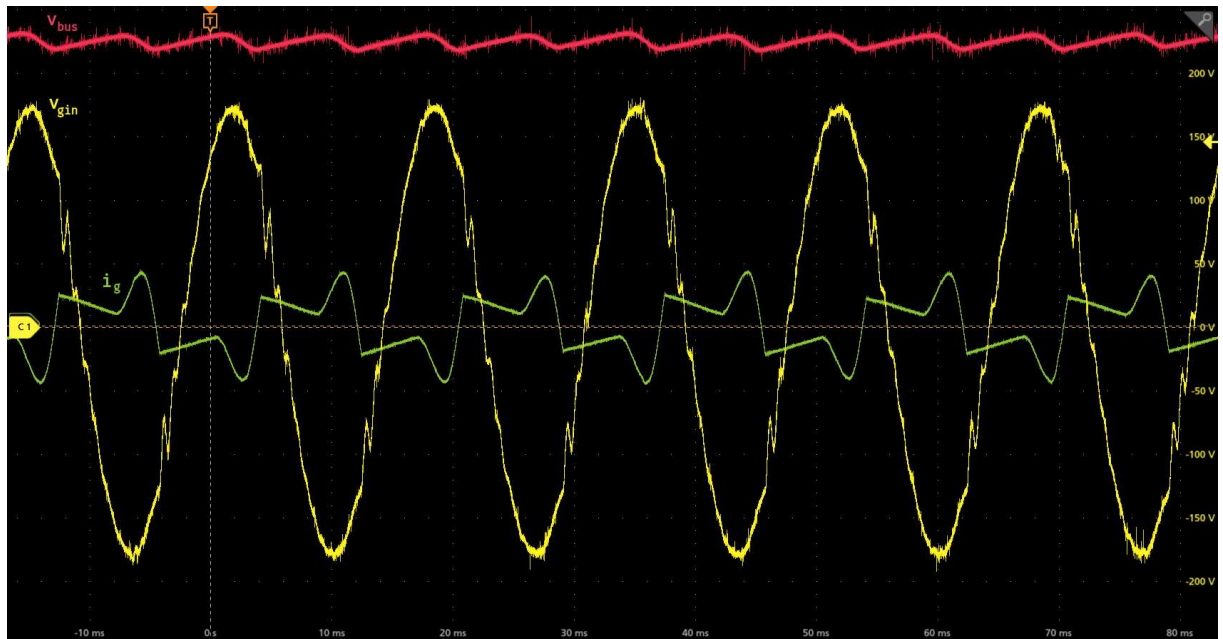
Figure 46: Inverter in islanded mode supplying non-linear load *without* harmonic compensation. Voltages are 50 V/div and current is 10 A/div.



Source: own work.

When the Harmonic Compensation (HC) is activated, the lower-order odd harmonics from 3rd to 9th are attenuated, and the resulting waveforms are depicted in Figure 47.

Figure 47: Inverter in islanded mode supplying non-linear load *with* harmonic compensation. Voltages are 50 V/div and current is 10 A/div.



Source: own work.

Because these lower-order harmonics are superposed with many others, including the fundamental itself, the differences between Figure 46 and Figure 47 are quite subtle in time-domain.

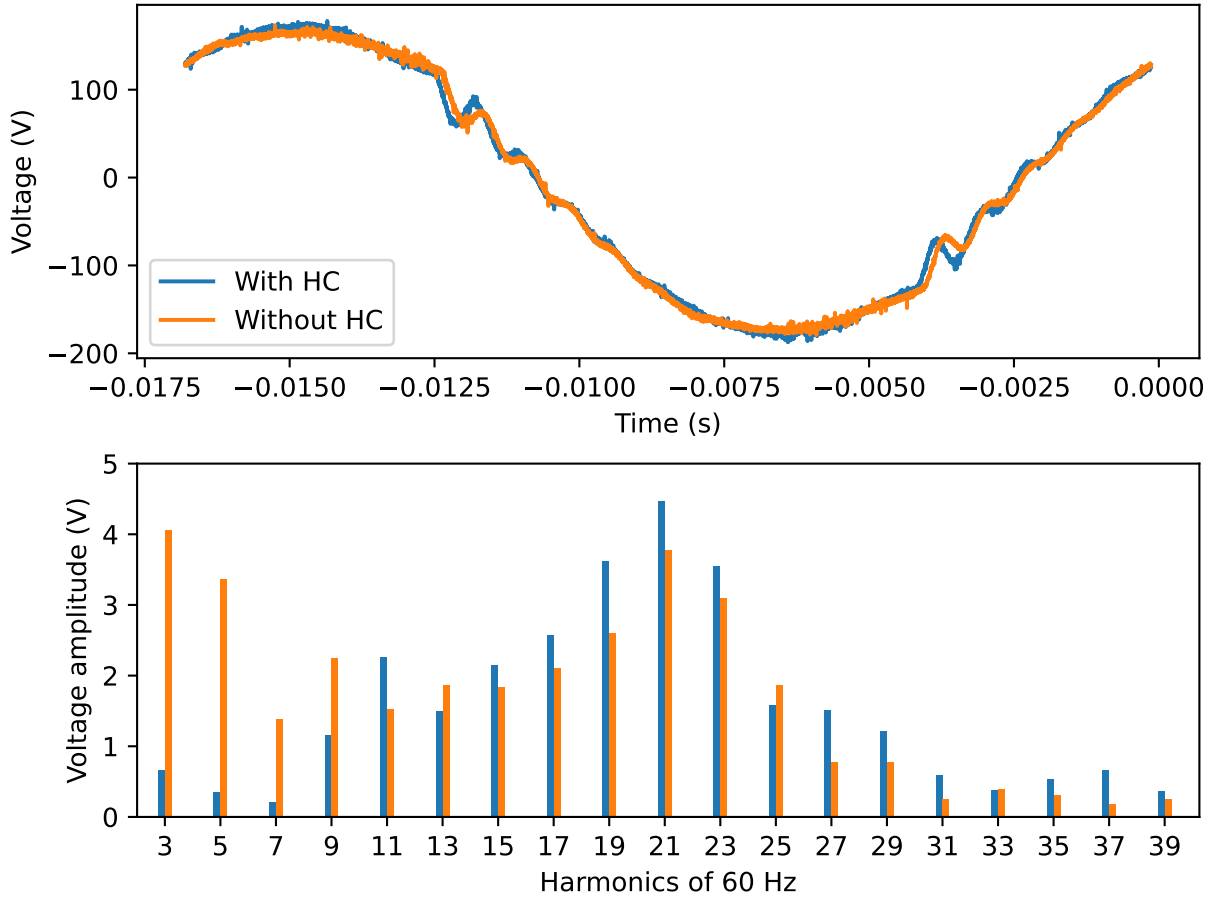
By post-processing the acquired data with the Fast Fourier Transform (FFT) algorithm, the time-domain signal can be converted into its frequency-domain representation, where the voltage amplitude of each harmonic multiple of 60 Hz can be isolated.

Figure 48 shows a single period of v_{gin} from the two situations superposed in time-domain, followed by their corresponding side-by-side Fourier Transform decompositions.

As is clearly shown in Figure 48, the 3rd, 5th, 7th and 9th harmonics are attenuated in different degrees. The effect of the 3rd harmonic can also be seen in time-domain, which causes a slight flattening at the peak of the sinusoidal waveform. The greater the load power, the greater the amplitude of the non-linear current pulses, which are responsible for the harmonic distortion. Therefore, the benefits of the harmonic compensation are more noticeable for large loads.

Moreover, a slight increase in the higher-order harmonics is noticeable. Because the non-ideal resonant harmonic controllers have a non-zero bandwidth, they unfortu-

Figure 48: Comparison of the inverter feeding a non-linear load: with and without HC.



Source: own work.

nately also amplify the frequency band around the LCL+RC filter resonance, which contributes to the increased oscillations around the 21st harmonic in this case.

Although increased oscillations were found, more iterations of the filter design could mitigate these issues. Furthermore, it can be argued that it is preferable to attenuate the lower-order harmonics despite the extra oscillations because lower-order current harmonics are usually more difficult to be attenuated by electric motors and by passive filters of electronic devices and appliances.

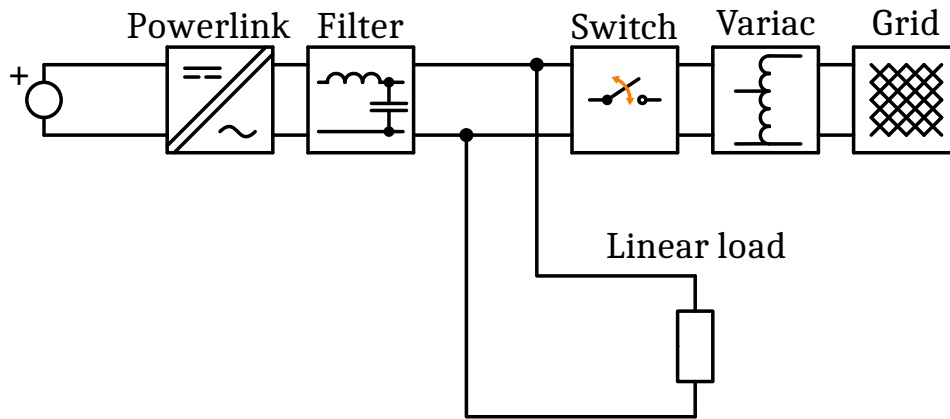
In three-phase four-wire systems, the triplen harmonics formed by the 3rd harmonic and its multiples (mainly the odd 9th, 15th, 21st, etc) constitute the zero-sequence symmetrical components, meaning the contribution from each phase adds up to the neutral wire, even if the system is balanced [58]. This might cause excessive power loss in the neutral wire if not treated, and it is therefore best if these harmonics could be mitigated by as much as possible.

4.2.3 Grid Disconnection

This test was performed to verify the behavior of the protection and synchronization software modules, as well as the grid interface hardware components.

For this test, as seen in Figure 49, a linear resistive load was used to allow for easier comparison between the grid and inverter voltages.

Figure 49: Test setup schematic for the disconnection and reconnection with linear load.



Source: own work.

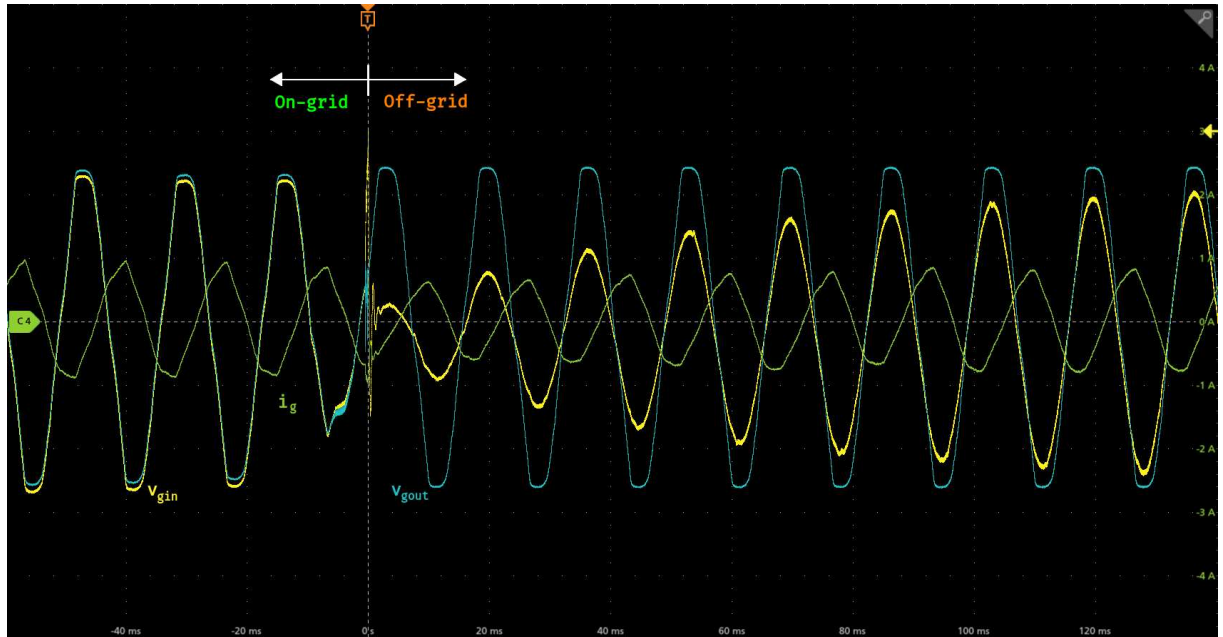
The current and voltages waveforms for this test are shown in Figure 50 during the disconnection event at the mark of 0 s. A few milliseconds before the disconnection, the external grid voltage v_{gout} suffers a surge which prompts the UPS to open the interface relay and start the inverter. In the following dozens of milliseconds, the inverter's internal voltage v_{gin} increases in amplitude under load until the nominal voltage value is reached.

4.2.4 Grid Reconnection

Using the same test setup as in Figure 49, the grid reconnection test aims to verify the prototype behavior after the resynchronization and the switch activation. This event can be observed with the current and voltage waveforms in Figure 51.

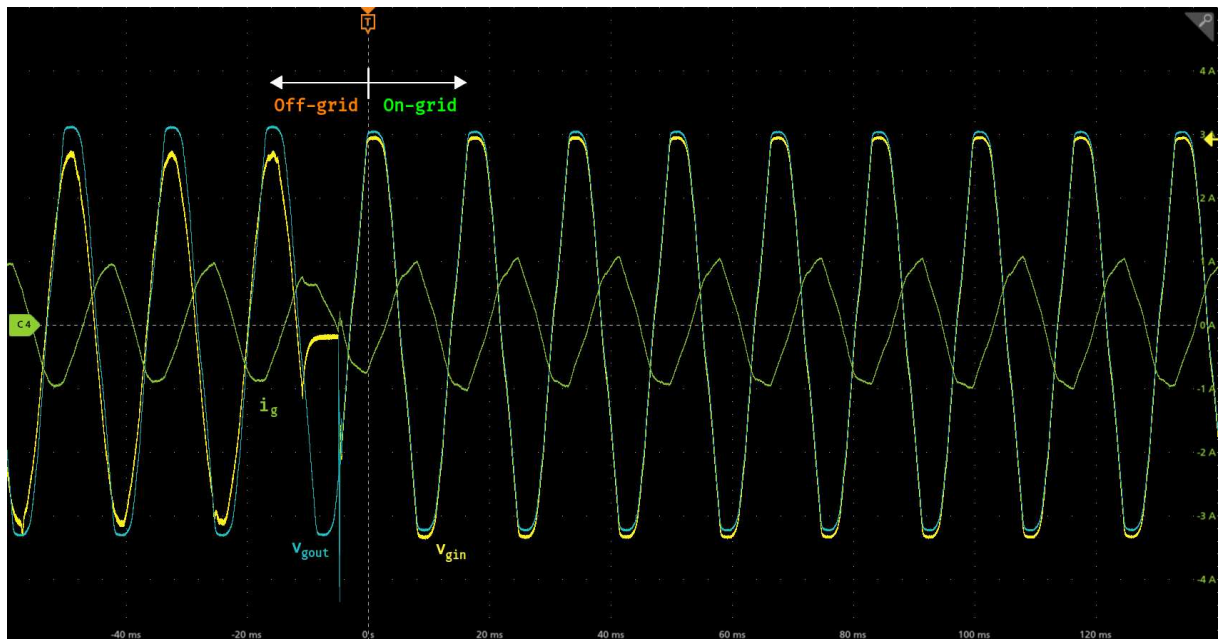
After a time interval of off-grid operation, the UPS resynchronizes and half a grid cycle before the relay closes, the inverter shuts down to prevent voltage mismatch while reconnecting. When the load is once again fed by the grid, the inverter stands by in case another outage or surge causes another disconnection.

Figure 50: Event of grid disconnection due to an emulated outage.



Source: own work.

Figure 51: Reconnection with the grid after resynchronization.



Source: own work.

5 Conclusion

This master thesis aimed to study a solution to harvest the energy storage capability of modern UPS and apply it in low demand residential and commercial applications because UPS systems are important tools to mitigate the undesirable effects on critical loads due to power outages.

Different UPS architectures were compared, and many power electronics topologies were analyzed to arrive at the proposed system. The selected topology was mathematically modeled, the hardware components and digital controllers were sized to fulfill the requirements, and the complete system was simulated. Moreover, the procedures to choose the converter parameters were presented as a direct methodology to provide applicable guidelines when sizing the system.

After the working principle was validated, the Powerlink UPS prototype was conceived in a PCB aimed to enable components mounting, experimental tests and debugging. Besides the firmware code to provide digital control, a communication framework was implemented to establish a safe and efficient user control interface.

The experimental tests focused on the output voltage control, including harmonics suppression caused by non-linear loads and the grid connection/disconnection capability. These tests showed the efficacy of the proposed control techniques and algorithms to achieve their targets regarding the output voltage control. The acquired results together with more rigorous testing, research and development lead to the conclusion that the UPS subject of this thesis could safely be utilized as a general transient backup solution for low power applications.

Although not thoroughly covered, this work could be extended by future works if on-grid current control was tested and validated to both recharge the batteries and to provide grid support functionalities, such as load shifting, voltage and frequency regulations.

Moreover, one functionality not implemented in the scope of this master thesis is the parallelization of two or more Powerlinks with a self-regulating power flow which would include an additional output droop control capable of increasing power throughput proportionally to the number of parallel devices.

It is hoped that this thesis will serve as a useful resource for others seeking an overview of the topic and as a reference for the methods proposed.

References

- [1] Modm Team, “Modular Object-oriented Development for Microcontrollers — modm: a barebone embedded library generator,” <https://modm.io/>, 2025.
- [2] J. D. Hunter, “Matplotlib: A 2d graphics environment,” *Computing in Science & Engineering*, vol. 9, no. 3, pp. 90–95, 2007.
- [3] S. Fuller, B. Greiner, J. Moore, R. Murray, R. van Paassen, and R. Yorke, “The python control systems library (python-control),” in *60th IEEE Conference on Decision and Control (CDC)*. IEEE, 2021, pp. 4875–4881.
- [4] A. Meurer, C. P. Smith, M. Paprocki, O. Čertík, S. B. Kirpichev, M. Rocklin, A. Kumar, S. Ivanov, J. K. Moore, S. Singh, T. Rathnayake, S. Vig, B. E. Granger, R. P. Muller, F. Bonazzi, H. Gupta, S. Vats, F. Johansson, F. Pedregosa, M. J. Curry, A. R. Terrel, v. Roučka, A. Saboo, I. Fernando, S. Kulal, R. Cimrman, and A. Scopatz, “SymPy: symbolic computing in python,” *PeerJ Computer Science*, vol. 3, p. e103, Jan. 2017. [Online]. Available: <https://doi.org/10.7717/peerj-cs.103>
- [5] C. R. Harris, K. J. Millman, S. J. van der Walt, R. Gommers, P. Virtanen, D. Cournapeau, E. Wieser, J. Taylor, S. Berg, N. J. Smith, R. Kern, M. Picus, S. Hoyer, M. H. van Kerkwijk, M. Brett, A. Haldane, J. F. del Río, M. Wiebe, P. Peterson, P. Gérard-Marchant, K. Sheppard, T. Reddy, W. Weckesser, H. Abbasi, C. Gohlke, and T. E. Oliphant, “Array programming with NumPy,” *Nature*, vol. 585, no. 7825, pp. 357–362, Sep. 2020. [Online]. Available: <https://doi.org/10.1038/s41586-020-2649-2>
- [6] The pandas development team, “pandas-dev/pandas: Pandas,” Feb. 2020. [Online]. Available: <https://doi.org/10.5281/zenodo.3509134>
- [7] S. N. Rezaei, L. Chouinard, S. Langlois, and F. Légeron, “Analysis of the effect of climate change on the reliability of overhead transmission lines,” *Sustainable Cities and Society*, vol. 27, pp. 137–144, 2016. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S2210670716300075>
- [8] J. Dowejko and J. Jaworski, “Beyond traditional grid: A novel quantitative framework for assessing automation’s impact on system average interruption duration index and system average interruption frequency index,” *Energies*, vol. 18, no. 11, p. 2671, 2025.

- [9] S. Saha, M. Saleem, and T. Roy, "Impact of high penetration of renewable energy sources on grid frequency behaviour," *International Journal of Electrical Power & Energy Systems*, vol. 145, p. 108701, 2023. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0142061522006974>
- [10] J. Marqusee and D. Jenket, "Reliability of emergency and standby diesel generators: Impact on energy resiliency solutions," *Applied Energy*, vol. 268, p. 114918, 2020. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S030626192030430X>
- [11] T. B. Lazzarin and I. Barbi, "Design of a 660 v / 15 kva single-phase ups based on series connection of low-output-voltage modular ups," *Eletrônica de Potência*, vol. 17, no. 3, pp. 584–591, Aug. 2012.
- [12] R. F. Coelho, L. Schmitz, and D. C. Martins, "Grid-connected renewable hybrid system for uninterruptible dc load maintenance," in *XI Brazilian Power Electronics Conference*, 2011, pp. 155–161.
- [13] R. Krishnan and S. Srinivasan, "Topologies for uninterruptible power supplies," in *ISIE '93 - Budapest: IEEE International Symposium on Industrial Electronics Conference Proceedings*, 1993, pp. 122–127.
- [14] M. Reinert, J. Sperb, M. Mezaroba, C. Rech, and L. Michels, "Ups de dupla conversão não isolada usando snubber regenerativo," *Eletrônica de Potência*, vol. 16, p. 158, 03 2011.
- [15] M. Marei, I. Abdallah, and H. Ashour, "Transformerless uninterruptible power supply with reduced power device count," *Electric Power Components and Systems*, vol. 39, pp. 1097–1116, 11 2011.
- [16] A. Nasiri, "Digital control of three-phase series-parallel uninterruptible power supply systems," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1116–1127, 2007.
- [17] International Electrotechnical Commission (IEC), "IEC 62040-3, Uninterruptible power systems (UPS) — Part 3: Method of specifying the performance and test requirements," 2021.

- [18] J.-H. Choi, J.-M. Kwon, J.-H. Jung, and B.-H. Kwon, "High-performance online ups using three-leg-type converter," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 889–897, 2005.
- [19] J.-C. Wu and H.-L. Jou, "A new ups scheme provides harmonic suppression and input power factor correction," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 6, pp. 629–635, 1995.
- [20] F. Kamran and T. Habetler, "A novel on-line ups with universal filtering capabilities," *IEEE Transactions on Power Electronics*, vol. 13, no. 3, pp. 410–418, 1998.
- [21] "IEEE guide for batteries for uninterruptible power supply systems," *IEEE Std 1184-2022 (Revision of IEEE Std 1184-2006)*, pp. 1–110, 2022.
- [22] M. A. Abusara, J. M. Guerrero, and S. M. Sharkh, "Line-interactive ups for microgrids," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1292–1300, 2014.
- [23] S. Oliveira da Silva, R. Modesto, A. Neto, and S. Cervantes, "A single-phase ups system with harmonic suppression and reactive power compensation," 09 2009, pp. 558–563.
- [24] M. Schweizer, N. Notari, S. Colombi, and I. Furlan, "Frequency control and inertia provision with ups," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022, pp. 1–8.
- [25] A. Chen and P. K. Sen, "Advancement in battery technology: A state-of-the-art review," in *2016 IEEE Industry Applications Society Annual Meeting*, 2016, pp. 1–10.
- [26] Generac , "Generac PWRcell Battery Module — Datasheet," <https://web.archive.org/web/20230706112441/https://www.generac.com/generacorporate/media/library/content/clean%20energy/a0000953959.pdf?ext=.pdf>, 2022.
- [27] Panasonic, "Panasonic EverVolt Standard — Datasheet," https://ftp.panasonic.com/batterystorage/datasheet/evervolt_datasheet.pdf, 2021.
- [28] BYD, "BYD BatteryBox LV Flex Lite — Datasheet," https://bydennergia.com/wp-content/uploads/2024/12/BBOX_LV-FLEX-LITE_Datasheet_PT_V1.0_240802.pdf, 2025.

- [29] Enphase, “Enphase IQ Battery 10T — Datasheet,” <https://enphase.com/download/iq-battery-10t-data-sheet>, 2024.
- [30] Tesla Inc., “Tesla Powerwall 2 — Datasheet,” https://www.tesla.com/sites/default/files/pdfs/powerwall/Powerwall%20AC_Datasheet_en_northamerica.pdf, 2019.
- [31] W. Li, X. Mou, Y. Zhou, and C. Marnay, “On voltage standards for dc home microgrids energized by distributed sources,” in *Proceedings of The 7th International Power Electronics and Motion Control Conference*, vol. 3, 2012, pp. 2282–2286.
- [32] S. Anand and B. G. Fernandes, “Optimal voltage level for dc microgrids,” in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 3034–3039.
- [33] Generac, “Generac PWRcell Inverter — Datasheet,” https://web.archive.org/web/20230705195748/https://www.generac.com/generacorporate/media/library/content/clean%20energy/a0000909057_pwrcell_inverter-1phase_ss_rev-b_eng-spa.pdf?ext=.pdf, 2023.
- [34] I. Aouichak, S. Jacques, S. Bissey, C. Reymond, T. Besson, and J.-C. Le Bunetel, “A bidirectional grid-connected dc–ac converter for autonomous and intelligent electricity storage in the residential sector,” *Energies*, vol. 15, no. 3, 2022. [Online]. Available: <https://www.mdpi.com/1996-1073/15/3/1194>
- [35] Creative Commons, “Creative Commons Attribution 4.0 International,” <https://creativecommons.org/licenses/by/4.0/>, 2025.
- [36] J. Zeng, G. Zhang, S. S. Yu, B. Zhang, and Y. Zhang, “Llc resonant converter topologies and industrial applications — a review,” *Chinese Journal of Electrical Engineering*, vol. 6, no. 3, pp. 73–84, 2020.
- [37] L. Li, G. Xu, D. Sha, Y. Liu, Y. Sun, and M. Su, “Review of dual-active-bridge converters with topological modifications,” *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 9046–9076, 2023.
- [38] B. Zhao, Q. Song, W. Liu, and Y. Sun, “Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system,” *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091–4106, 2014.

- [39] L. Farias Martins, D. Stone, and M. Foster, "Modelling of phase-shift modulated bidirectional clc resonant converter," *IET Power Electronics*, vol. 13, no. 12, pp. 2628–2637, 2020. [Online]. Available: <https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2018.5672>
- [40] Z. Pavlović, J. A. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "Bidirectional dual active bridge series resonant converter with pulse modulation," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 503–508.
- [41] W. L. Malan, D. M. Vilathgamuwa, and G. R. Walker, "Modeling and control of a resonant dual active bridge with a tuned clc network," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7297–7310, 2016.
- [42] V. R. Vakacharla, A. K. Rathore, P. R. Tripathi, and R. K. Keshri, "A comprehensive review of fundamental harmonic approximation analysis techniques for series-parallel resonant converters with capacitive filter," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 2581–2585.
- [43] R. Twinaime, W. Malan, J. Minogue, D. J. Thrimawithana, U. K. Madawala, and C. Baguley, "A novel dual active bridge topology with a tuned clc network," in *2014 IEEE International Conference on Industrial Technology (ICIT)*, 2014, pp. 895–900.
- [44] Tellegen, B.D.H., "The gyrator, a new electric network element," *Philips Research Reports*, 1948.
- [45] S. M. Kotian and K. N. Shubhanga, "Dynamic phasor modelling and simulation," in *2015 Annual IEEE India Conference (INDICON)*, 2015, pp. 1–6.
- [46] S. Sanders, J. Noworolski, X. Liu, and G. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251–259, 1991.
- [47] A. Bodrov, Y. Nael, R. Todd, and J. Apsley, "Equivalence of generalized state-space averaging with dq modelling methods in a balanced three-phase system," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5519–5524.

- [48] Y. Xia and R. Ayyanar, "Comprehensive comparison of thd and common mode leakage current of bipolar, unipolar and hybrid modulation schemes for single phase grid connected full bridge inverters," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 743–750.
- [49] J. Soomro, T. D. Memon, and M. A. Shah, "Design and analysis of single phase voltage source inverter using unipolar and bipolar pulse width modulation techniques," in *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEEES)*, 2016, pp. 277–282.
- [50] E. E. Behr, "Filtros passivos aplicados a inversores monofásicos conectados à rede elétrica," Final Course Project, UFSC — Universidade Federal de Santa Catarina, Florianópolis, Brazil, 2019, <https://repositorio.ufsc.br/handle/123456789/197977?show=full>.
- [51] F.-Y. Shih, D. Chen, Y.-P. Wu, and Y.-T. Chen, "A procedure for designing emi filters for ac line applications," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 170–181, 1996.
- [52] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.
- [53] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A new design method for the passive damped lcl and llcl filter-based single-phase grid-tied inverter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4339–4350, 2013.
- [54] R. Ozenbaugh and T. Pullen, *EMI Filter Design, Third Edition*. Taylor & Francis, 2011. [Online]. Available: <https://books.google.com.br/books?id=dzMCvbGoHiQC>
- [55] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase pll structure based on second order generalized integrator," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–6.
- [56] L. Yan, Z.-Q. Zhu, J. Qi, Y. Ren, C. Gan, S. Brockway, and C. Hilton, "Multiple synchronous reference frame current harmonic regulation of dual three phase pmsm with en-

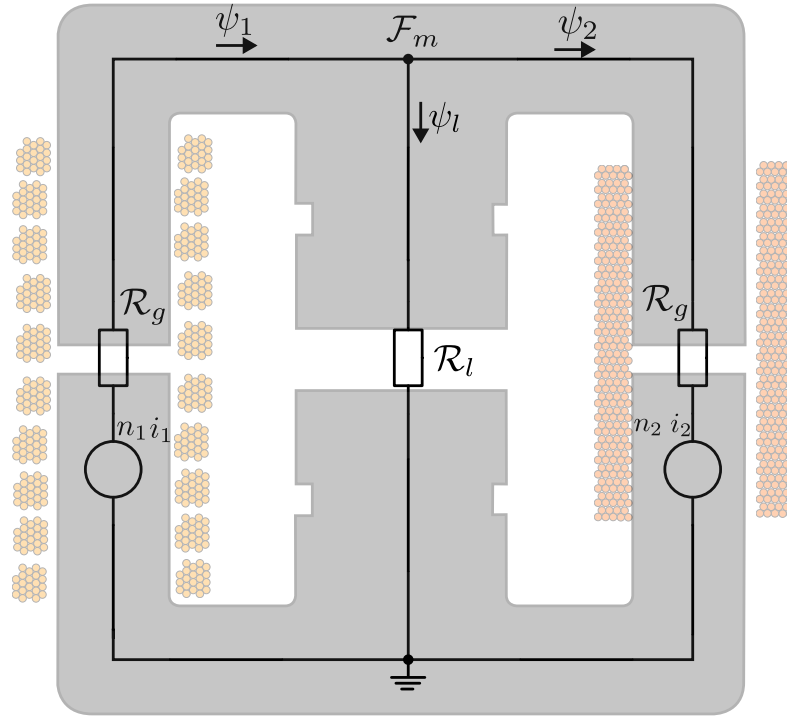
- hanced dynamic performance and system stability,” *IEEE Transactions on Industrial Electronics*, vol. 69, no. 9, pp. 8825–8838, 2022.
- [57] STMicroelectronics, “Reference Manual RM0455 — STM32H7A3/7B3 and STM32H7B0 Value line advanced Arm-based 32-bit MCUs,” [STMicroelectronics Reference Manual RM0455](#), 2025.
- [58] G. Chicco, P. Postolache, and C. Toader, “Triplen harmonics: Myths and reality,” *Electric Power Systems Research*, vol. 81, no. 7, pp. 1541–1549, 2011. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0378779611000708>
- [59] H. E. Dijk, “On transformer modelling: A physically based three-phase transformer model for the study of low frequency phenomena in electrical power systems,” Ph.D. dissertation, Technische Universiteit Delft, 1988.
- [60] M. Lambert, M. Martinez, J. Mahseredjian, F. de Leon, and F. Sirois, “Transformer leakage flux models for electromagnetic transients: Critical review and validation of a new model,” in *2014 IEEE PES General Meeting — Conference & Exposition*, 2014, pp. 1–1.

A Magnetic Reluctance Model

A magnetic circuit can be mostly treated as analogous to an electric one due to the mathematical symmetry between them. When designing a high frequency transformer with embedded leakage inductance, it is important to understand the internal relationships of magnetic quantities.

Assuming the ferrite has a magnetic permeability μ much greater than that of the air (μ_0), the reluctances in the magnetic flux path are mostly caused by the air gaps, as shown in Figure 52.

Figure 52: Reluctance model of an E core ferrite transformer.



Source: own work.

A brief calculation method will be presented below using the integral flux method as explained by [59, 60].

A.1 Primary side inductance L_1

The inductance on the primary side measures the amount of linked flux $n_1 \psi_1$ generated by the primary current i_1 when the secondary side is open circuit, according to

$$L_1 = \frac{n_1 \psi_1}{i_1}. \quad (58)$$

In the magnetic circuit, primary side flux and current are related by Hopkinson's law:

$$\mathcal{F}_1 = i_1 n_1 = \mathcal{R}_{eq} \psi_1, \quad (59)$$

where $\mathcal{R}_{eq}$ is the equivalent reluctance measured by the primary side. Then, the primary coil inductance is found by

$$L_1 = \frac{n_1^2}{\mathcal{R}_{eq}}, \quad (60)$$

which after expanded to the discrete gap and leakage reluctances $\mathcal{R}_g$ and $\mathcal{R}_l$ results in

$$L_1 = \frac{n_1^2 (\mathcal{R}_g + \mathcal{R}_l)}{\mathcal{R}_g (\mathcal{R}_g + 2\mathcal{R}_l)}. \quad (61)$$

A.2 Magnetizing inductance L_m

Similarly, the magnetizing inductance L_m seen by the primary side measures the amount of linked flux $n_2 \psi_2$ on the secondary side induced by the primary current i_1 , or vice-versa, according to

$$L_m = \frac{n_1}{n_2} \frac{\psi_2 n_2}{i_1}. \quad (62)$$

To calculate ψ_2 , first the Magnetomotive Force (MMF) $\mathcal{F}_m$ at the central core leg must be found with

$$\mathcal{F}_m = i_1 n_1 - \mathcal{R}_g \psi_1. \quad (63)$$

To solve (63), ψ_1 must first be computed by

$$\psi_1 = \frac{i_1 n_1}{\mathcal{R}_{eq}} \rightarrow \psi_1 = \frac{i_1 n_1 (\mathcal{R}_g + \mathcal{R}_l)}{\mathcal{R}_g (\mathcal{R}_g + 2\mathcal{R}_l)}, \quad (64)$$

and substituting ψ_1 into (63) yields

$$\mathcal{F}_m = i_1 n_1 - \frac{i_1 n_1 (\mathcal{R}_g + \mathcal{R}_l)}{\mathcal{R}_g + 2\mathcal{R}_l}. \quad (65)$$

The secondary flux ψ_2 is then calculated by the MMF on the secondary gap reluctance $\mathcal{R}_g$, as in

$$\psi_2 = \frac{\mathcal{F}_m}{\mathcal{R}_g} \rightarrow \psi_2 = \frac{i_1 \mathcal{R}_l n_1}{\mathcal{R}_g (\mathcal{R}_g + 2\mathcal{R}_l)}. \quad (66)$$

Substituting ψ_2 into (62) finally yields

$$L_m = \frac{\mathcal{R}_l n_1^2}{\mathcal{R}_g (\mathcal{R}_g + 2\mathcal{R}_l)}. \quad (67)$$

A.3 Primary side leakage inductance L_{r1}

The leakage inductance measured at the primary side is simply the total minus the magnetizing inductance: $L_{r1} = L_1 - L_m$

A.4 Calculating reluctances

Similar to resistance, a magnetic reluctance $\mathcal{R}$ can be found by relating the materials permeability μ with its cross section area A_e and path length l_e , as in

$$\mathcal{R} = \frac{l_e}{A_e \mu}. \quad (68)$$

When using the relationships presented above, an approximation for all transformer inductances can be found purely as function of geometric parameters. However, note that this method does not take into account the effects of temperature, core saturation, etc.

B System Discretization

The control discretization is the process of converting a continuous-time analog system into the discrete-time digital domain.

A transfer function in s domain can be transformed into the z domain with the bilinear transform using trapezoidal integration according to the substitution (69).

$$s = \frac{2}{T_s} \frac{z-1}{z+1} \quad (69)$$

After factoring the coefficients of z to form a proper rational transfer function of two polynomials of z , the discrete system may be represented by the Infinite Impulse Response (IIR) filter in (70).

$$\frac{Y(z)}{U(z)} = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0} \quad (70)$$

In explicit form, the current output sample $y[0]$ can be represented as a function of all the n previous inputs and $n-1$ outputs (excluding itself), as defined by (71).

$$y[0] = \frac{1}{b_n} \left[\sum_{i=0}^n a_i u_{[i-n]} - \sum_{i=0}^{n-1} b_i y_{[i-n]} \right] \quad (71)$$

The expression (71) can then be programmatically solved in real time by a computer using the macros defined in C source code 1. The systems defined by these macros may be of any order. However, note that high order systems may become unstable in discrete domain due to numerical errors caused by finite arithmetic.

Source code 1: Generic structure and function call to process any order of discrete system in Z domain in explicit form.

```

1  /**
2   * @brief Implements the discrete Z transfer function in time-domain,
   *      according to the following equation:
3   *
4   * $$y[0] = \frac{1}{b_n} \left[ \sum_{i=0}^n \{a_i u[i-n]\} - \sum_{i=0}^{n-1} \{b_i y[i-n]\} \right]$$
5   *
6   * @note
7   * a is the array of the numerator, and b the array of the denominator.
8   * The index represent the power of z (e.g. a[0] is the term without z, and
   *      a[2] is the term with z**2)
9   *
10  * @details Example:
11  *
12  *      DECLARE_DISCRETE_SYSTEM(2);

```

```

13  *
14  *      DiscreteSystemOrder2_t sys;
15  *
16  *      memset(&sys, 0, sizeof(DiscreteSystemOrder2_t));
17  *
18  *      float output = discrete_system_order_2_process(&sys, input);
19  *
20  */
21 #pragma once
22
23 #define DECLARE_DISCRETE_SYSTEM(order) \
24 \
25 typedef struct { \
26     float a[order+1]; \
27     float b[order+1]; \
28     float u[order+1]; \
29     float y[order+1]; \
30 } DiscreteSystemOrder##order##_t; \
31 \
32 float discrete_system_order_##order##_process(DiscreteSystemOrder##order##_t * sys, float input);
33
34
35 #define DEFINE_DISCRETE_SYSTEM(order) \
36 float discrete_system_order_##order##_process(DiscreteSystemOrder##order##_t * sys, float input) { \
37     sys->u[0] = input; \
38     sys->y[0] = 0; \
39     for(int i=0; i<=order; i++){ \
40         sys->y[0] += sys->a[i] * sys->u[order-i]; \
41         if(i <= order-1){ \
42             sys->y[0] -= sys->b[i] * sys->y[order-i]; \
43         } \
44     } \
45     sys->y[0] = sys->y[0]/sys->b[order]; \
46 \
47     for(int i=order; i>0; i--){ \
48         sys->u[i] = sys->u[i-1]; \
49         sys->y[i] = sys->y[i-1]; \

```

```
50     }\
51     return sys->y[0];\
52 }
```

C Proportional Resonant Controller Implementation

Equation (57) defines a resonant transfer function with central frequency, bandwidth and gain in the s domain. The discretized transfer function of the resonant controller with a proportional gain is implemented by the source code 2 with the same discretization technique presented in Appendix B.

The PMR controller with harmonic compensation is implemented in a digital system by summing the output of multiple resonant controllers and a single proportional gain. Since each resonant controller has transfer functions of order two, the overall discrete system is numerically stable as long as each one of the transfer functions is stable. If a high-order transfer function containing all the harmonics suppressors were to be used, numerical instability would arise due to the finite precision of the discretized system.

Source code 2: Implementation of a discrete proportional resonant controller using the bilinear transformation.

```
1  /**
2   * @author Eduardo Eller Behr
3   * @brief Implements a discrete-time Proportional Resonant (PR) controller
4   *        using the bilinear transform
5   */
6
7  #include "z_domain_system.h" // Code for system discretization as in
8                               Appendix A
9  #include <math.h>
10
11  DECLARE_DISCRETE_SYSTEM(2);
12
13  typedef struct {
14     DiscreteSystemOrder2_t sys;
```

```

14 } BilinearResonant_t;
15
16 void bilinear_resonant_reset(BilinearResonant_t* resonant){
17     // Input stream
18     resonant->sys.u[0] = 0;
19     resonant->sys.u[1] = 0;
20     resonant->sys.u[2] = 0;
21
22     // Output stream
23     resonant->sys.y[0] = 0;
24     resonant->sys.y[1] = 0;
25     resonant->sys.y[2] = 0;
26 }
27
28 void bilinear_resonant_init(BilinearResonant_t* resonant, float fc, float
    fbw, float kr, float Ts){
29     const float wbw = (2.0f*M_PI)*fbw;
30     const float wc = (2.0f*M_PI)*fc;
31     const float common = 4.0f*Ts*wbw;
32     const float squares = Ts*Ts*wc*wc;
33
34     // Numerator coefficients
35     resonant->sys.a[0] = -common*kr;
36     resonant->sys.a[1] = 0;
37     resonant->sys.a[2] = common*kr;
38
39     // Denominator coefficients
40     resonant->sys.b[0] = squares - common + 4.0f;
41     resonant->sys.b[1] = 2.0f*squares - 8.0f;
42     resonant->sys.b[2] = squares + common + 4.0f;
43
44     // Set all states to zero
45     bilinear_resonant_reset(resonant);
46 }
47
48 float bilinear_resonant_process(BilinearResonant_t* resonant, float input){
49     return discrete_system_order_2_process(&resonant->sys, input);
50 }

```

D Recursive Moving Mean Squared Filter

The recursive moving mean squared filter is an efficient procedure to compute the RMS of a signal because when using long buffers, only the samples at the two extremities need to be processed.

Consider the definition of the instantaneous RMS $y_{[n]}$ for a discrete signal stored in buffer u , as represented by (72).

$$y_{[n]} = \sqrt{\frac{1}{L} \cdot \sum_{l=0}^{L-1} u_{[n-l]}^2} \quad (72)$$

If the square of the RMS of two consecutive samples are subtracted from each other as in (73), the current value of the RMS squared can be computed simply using the previous value of the RMS $y_{[n-1]}$, the newest sample $u_{[n]}$ and the oldest sample $u_{[n-L]}$. This result is shown in (74).

$$\begin{aligned} y_{[n]}^2 &= \frac{1}{L} \left(u_{[n]}^2 + u_{[n-1]}^2 + u_{[n-2]}^2 + \cdots + u_{[n-L+1]}^2 \right) \\ -y_{[n-1]}^2 &= -\frac{1}{L} \left(u_{[n-1]}^2 + u_{[n-2]}^2 + \cdots + u_{[n-L+1]}^2 + u_{[n-L]}^2 \right) \end{aligned} \quad (73)$$

$$y_{[n]}^2 - y_{[n-1]}^2 = \frac{1}{L} \left(u_{[n]}^2 - u_{[n-L]}^2 \right)$$

$$y_{[n]} = \sqrt{y_{[n-1]}^2 + \frac{1}{L} \left(u_{[n]}^2 - u_{[n-L]}^2 \right)} \quad (74)$$

All this procedure is implemented using the C++ template class `MovingMeanSquared` in the source code 3, whose process function returns the current mean squared of the input signal (the RMS value can be computed by taking its square root when needed). This code can also be adapted for the simpler moving mean filter by removing the square and square root operators.

Source code 3: Efficient recursive moving mean squared filter.

```
1  /**
2   * @brief Implements a recursive moving Mean Square of a signal
3   *
```

```

4  */
5  #pragma once
6  #include <cstdint>
7  #include <cstddef>
8
9
10 template<size_t bufferLength>
11 class MovingMeanSquared {
12 public:
13     MovingMeanSquared() = default;
14
15     /**
16      * @brief Computes the current mean squared value of the signal, given
17      *        a new input sample
18      *
19      * @return float current mean squared value. The RMS is the square root
20      *        of it.
21      */
22     float process(float input){
23         float input_squared = input * input;
24
25         float* const buffer = this->circular_buffer_squared;
26
27         // Save n-L sample before overwriting it
28         float n_minus_L = buffer[this->buffer_index];
29
30         // Store value in circular buffer (for use in Nth sample)
31         buffer[this->buffer_index] = input_squared;
32
33         // Update circular buffer pointer
34         if(this->buffer_index >= (this->L - 1)){
35             this->buffer_index = 0;
36         } else {
37             this->buffer_index++;
38         }
39
40         this->out_squared += this->invL * (input_squared - n_minus_L);
41
42         if(this->out_squared < 0){

```

```

41         return 0;
42     }
43     return this->out_squared;
44 }
45
46 /**
47  * @brief Returns the cumulative moving mean squared
48  * @note This is the value which, after taking the square root of, is
49  *       the moving RMS value
50  *
51  * @return float
52  */
53 [[nodiscard]] float get_moving_mean_squared() {
54     return this->out_squared;
55 }
56 private:
57     static constexpr size_t L{bufferLength}; /// Window Length
58     static constexpr float invL{1.0f/bufferLength}; /// 1/L
59
60     float circular_buffer_squared[L]{}; // {x(n)^2, x(n-1)^2, ...}
61     uint32_t buffer_index{};
62     float out_squared{};
63 };

```