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Marina Longo Dias

**Impact of Process Variability on Circuit-Level Radiation-Hardening Techniques**

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Marina Longo Dias

# Impact of Process Variability on Circuit-Level Radiation-Hardening Techniques

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Orientadora: Prof. Cristina Meinhardt, Dr.

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O presente trabalho em nível de mestrado foi avaliado e aprovado por banca examinadora composta pelos seguintes membros:

Prof. José Luis Almada Güntzel, Dr.
Universidade Federal de Santa Catarina

Alexandra Lackmann Zimpeck, Dr.
Cadence Design Systems

Prof. Rafael Budim Schvittz, Dr.
Universidade Federal de Rio Grande

Certificamos que esta é a **versão original e final** do trabalho de conclusão que foi julgado adequado para obtenção do título de mestre em Ciência da Computação.

Prof. Carina Friedrich Dorneles, Dr.
Coordenadora do Programa

Prof. Cristina Meinhardt, Dr.
Orientadora

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"비 온 뒤에 땅이 굳어진다"
*"After the rain, the ground hardens."*
(Korean proverb)

# RESUMO

A tecnologia FinFET oferece vantagens como menor consumo de energia e redução dos efeitos de canal curto, mas também está sujeita a desafios relacionados à variabilidade de processo e à sensibilidade à radiação. A principal fonte de variabilidade de processo em dispositivos FinFET está relacionada à granularidade do metal gate, que afeta a função trabalho, causando o efeito chamado flutuação da função trabalho (WFF). Isso afeta o comportamento esperado das correntes do dispositivo e dos tempos de propagação devido ao impacto na tensão limiar. Algumas abordagens propostas em nível de transistor ou de circuito para mitigação de ruído e efeitos de single-event transient (SET) podem ser exploradas para mitigar o impacto da variabilidade de processo. Este trabalho avalia o impacto da variabilidade de processo em técnicas de robustez em nível de circuito aplicadas a inversores. A primeira avaliação considera o impacto de técnicas de robustez em nível de circuito no desempenho e na confiabilidade de circuitos baseados em FinFET, comparando os resultados com achados prévios para tecnologias CMOS bulk. Quatro técnicas inicialmente propostas na literatura para mitigação de ruído e efeitos de SET são investigadas: Schmitt Trigger, Pseudo-Strengthening, Strengthening e Rad-Hard, sob condições de tensão nominal e near-threshold. Os resultados indicam que, sob condições nominais, a técnica Schmitt Trigger apresentou os melhores resultados de atraso e de near-threshold, enquanto a técnica Strengthening apresentou o menor atraso. A análise do consumo de energia revelou que a técnica Schmitt Trigger teve o menor consumo de energia entre as técnicas analisadas. Essa análise reforça a relevância da variabilidade de processo, especialmente em operações near-threshold, e destaca a necessidade de técnicas de robustez para mitigar os efeitos da variabilidade no projeto de circuitos digitais em tecnologias nanométricas. A segunda análise observa a robustez à radiação dessas quatro técnicas em nível de circuito para falhas SET. Os resultados mostram alta robustez para o Schmitt Trigger, mesmo considerando a variabilidade de processo. A terceira avaliação investiga a integração seletiva de topologias de inversores tolerantes à radiação em circuitos aritméticos de uma arquitetura RISC-V, visando melhorar a resiliência do sistema contra soft errors com sobrecarga mínima. As quatro técnicas foram então integradas a células somadoras completas para avaliar seu impacto no desempenho e na robustez. Esses somadores foram posteriormente incorporados ao processador RS5, uma implementação RISC-V, e sintetizados utilizando tecnologias CMOS de 45 nm e FinFET de 7 nm para avaliar seus trade-offs de área. O maior impacto em área é observado em 7 nm, com um aumento de 16,7% na contagem de transistores, um aumento marginal de 0,73% na ULA e apenas 0,031% em todo o processador RS5. Isso demonstra que o projeto de circuitos robustos pode ser alcançado com impacto mínimo na área total de silício, mesmo em nós de tecnologia avançados. Desta forma, os resultados obtidos demonstram que técnicas de robustez baseadas em inversores oferecem benefícios concretos para a mitigação simultânea dos efeitos de variabilidade de processo e radiação em dispositivos FinFET.

**Palavras-chave:** Variabilidade de Processo. Técnicas de Robustez em Nível de Circuito. Dispositivos FinFET.

## RESUMO ESTENDIDO


**Introdução**

O avanço contínuo da indústria de semicondutores tem sido impulsionado pela miniaturização dos dispositivos e pelo uso de arquiteturas mais eficientes, como os transistores FinFET, que sucedem os transistores planares convencionais. Embora ofereçam melhor controle de canal, menor consumo energético e mitigação de efeitos de canal curto, dispositivos FinFET permanecem vulneráveis a dois desafios fundamentais em tecnologias nanométricas: a variabilidade de processo e os efeitos de radiação, especialmente single-event transients (SETs). Em dispositivos avançados, a variabilidade física não decorre mais predominantemente de dopantes, mas da granularidade do metal do gate, que provoca a work-function fluctuation (WFF), afetando diretamente a tensão de limiar, as correntes ION/IOFF e os tempos de propagação. Em paralelo, a redução de capacitâncias internas e da tensão de alimentação diminui a carga crítica necessária para alterar estados lógicos, tornando circuitos digitais cada vez mais suscetíveis a falhas induzidas por partículas energéticas. Esse cenário reforça a importância de estratégias de robustez em nível de circuito, capazes de mitigar simultaneamente variabilidade de processo e radiação, especialmente para aplicações que demandam elevado grau de confiabilidade. Neste contexto, esta dissertação investiga o comportamento de quatro técnicas de robustez baseadas em inversores, Schmitt Trigger, Strengthening, Pseudo-Strengthening e Rad-Hard, considerando sua sensibilidade à variabilidade de processo e sua resposta a eventos transientes, além de avaliar sua viabilidade prática quando integradas em um processador RISC-V.

**Objetivos**

O objetivo principal deste trabalho é avaliar técnicas de robustez a nível de circuito aplicadas a inversores, considerando de forma conjunta os efeitos da variabilidade de processo e de eventos transientes induzidos por radiação. Para isso, são estabelecidos objetivos específicos que sustentam o desenvolvimento da pesquisa: (i) revisar e caracterizar técnicas de robustez baseadas em inversores; (ii) analisar o comportamento elétrico dessas técnicas sob operação nominal e near-threshold; (iii) quantificar o impacto da variabilidade induzida por WFF em múltiplos níveis; (iv) comparar os resultados obtidos em FinFET com achados prévios em tecnologias CMOS bulk; (v) avaliar a robustez radiativa das topologias considerando processo e radiação de forma combinada; e (vi) investigar os impactos de área decorrentes da adoção dessas técnicas em um processador RISC-V implementado em tecnologias de 45 nm e 7 nm.

**Metodologia**

A metodologia segue um fluxo integrado composto por três partes complementares. Primeiro, as quatro técnicas selecionadas são descritas em nível elétrico e simuladas em tecnologia FinFET 7 nm utilizando o PDK ASAP7. São consideradas duas configurações de tamanhos, 1 fin e 3 fins, e dois regimes de operação. A avaliação engloba medições de atraso de propagação e energia consumida, seguidas de uma análise estatística baseada em simulações Monte Carlo. A variabilidade de processo é modelada por meio da flutuação da função trabalho, com desvios gaussianos de 1%, 3% e 5%, totalizando 2000 iterações por técnica e tamanho de transistor.

Na segunda etapa, as mesmas topologias são submetidas à análise de radiação utilizando o fluxo de simulação do Quasar, uma ferramenta projetada para estimar o Linear Energy Transfer threshold sob diferentes condições de sensibilidade. A ferramenta permite investigar como a interação entre WFF e perturbações induzidas por partículas altera o comportamento transiente dos circuitos.

Por fim, as técnicas são implementadas em células somadoras completas e integradas ao processador RS5, uma implementação RISC-V de 32 bits. São realizados fluxos de síntese lógica e física tanto em 45 nm CMOS quanto em 7 nm FinFET, permitindo avaliar o impacto de área dessas técnicas em um caminho crítico de um circuito complexo.

**Resultados e Discussão**

A análise inicial, considerando comportamento regular dos circuitos, mostra que o Schmitt Trigger apresenta o menor consumo de energia entre todas as técnicas avaliadas, enquanto o Strengthening proporciona o menor atraso de propagação. O Pseudo-Strengthening, por outro lado, acumula as maiores penalidades em atraso e energia, indicando baixa atratividade prática. Operações near-threshold amplificam naturalmente a dispersão de desempenho, reforçando a necessidade de técnicas alternativas à simples redução de tensão.

Quando submetidas a eventos transientes, as topologias avaliada exibem respostas distintas. Os resultados mostraram que o inversor ST novamente alcançou a maior robustez, mantendo um LET mais elevado mesmo quando a variabilidade foi introduzida. A variabilidade de processo não apenas reduziu o limiar de LET em todos os circuitos, como também aumentou a dispersão da distribuição de robustez, às vezes alterando o nó mais sensível dentro de uma determinada topologia. O inversor Rad-Hard, por outro lado, apresenta valores de limiar de LET essencialmente iguais aos do inversor padrão, o que indica que essa abordagem de robustez não produz uma melhoria significativa na tolerância à radiação na tecnologia FinFET de 7 nm.

A análise sistêmica revela que, apesar de aumentarem o número de transistores das células somadoras, as técnicas de robustez exercem impacto mínimo na área total do processador. Em 7 nm, observa-se um aumento de 9,58% na contagem de transistores das células somadoras, quando consideradas com inversores Rad-Hard, mas correspondente a apenas 0,73% de acréscimo na área da ULA e 0,031% em todo o RS5, demonstrando que a inserção seletiva de técnicas de robustez é viável mesmo em nós de tecnologia avançados. Considerando somadores com inversores Schmitt Trigger, o aumento estimado da área total do processador é de 0.13%.

**Considerações Finais**

Os resultados obtidos demonstram que técnicas de robustez baseadas em inversores oferecem benefícios concretos para a mitigação simultânea dos efeitos de variabilidade de processo e radiação em dispositivos FinFET. Entre as técnicas avaliadas, o Schmitt Trigger emerge como a solução mais equilibrada, apresentando baixa penalidade energética, boa regularidade sob WFF e elevada robustez radiativa. Além disso, a investigação em nível sistêmico confirma que a adoção seletiva dessas técnicas introduz custos de área negligenciáveis quando inserida estrategicamente em blocos aritméticos de processadores RISC-V. Assim, este trabalho contribui com um panorama completo sobre a viabilidade de soluções de robustez a nível de circuito para tecnologias avançadas, evidenciando seu potencial para aplicações que exigem alta confiabilidade. Futuras extensões podem explorar técnicas capacitivas, como DCELLs, ou combinações híbridas que integrem elementos como C-elements, ampliando o conjunto de estratégias disponíveis para o projeto robusto em tecnologias nanométricas.

**Palavras-chave:** Variabilidade de Processo. Técnicas de Robustez a Nível de Circuito. Dispositivos FinFET.

**ABSTRACT**

FinFET technology offers advantages such as lower power consumption and reduced short-channel effects, but it is also subject to challenges related to process variability and radiation sensitivity. The main source of process variability in FinFET devices is related to the metal gate granularity, which affects the work function, causing the effect called work function fluctuation (WFF). This affects the expected behavior of device currents and propagation times due to the impact on the threshold voltage. Some proposed transistor-level or circuit-level approaches for noise mitigation and single-event transient (SET) effects can be explored to mitigate the impact of process variability. This work evaluates the impact of process variability on circuit-level hardening techniques applied to inverters. The first evaluation considers the impact of circuit-level robustness techniques on the performance and reliability of FinFET-based circuits, comparing the results with previous findings for bulk CMOS technologies. Four techniques initially proposed in the literature for noise mitigation and SET effects are investigated: Schmitt Trigger, Pseudo-Strengthening, Strengthening and Rad-Hard, under nominal and near-threshold voltage conditions. Results indicate that, under nominal conditions, the Schmitt Trigger technique yielded the best delay and near-threshold voltage results, while the Strengthening technique yielded the lowest delay. The analysis of energy consumption revealed that the Schmitt Trigger technique had the lowest energy consumption among the techniques analyzed. This analysis reinforces the relevant role of process variability, especially in near-threshold operations, and highlights the need for robustness techniques to mitigate the effects of variability in the design of digital circuits in nanometric technologies. The second analysis observes the radiation robustness of these four circuit-level for SET faults. The results show high robustness to the Schmitt Trigger, even accounting for process variability. The third evaluation investigates the selective integration of radiation-hardening inverter topologies into arithmetic circuits of a RISC-V architecture, aiming to improve system resilience against soft errors with minimal overhead. The four techniques were then integrated into full adder cells to evaluate their impact on performance and robustness. These full adders were further incorporated into the RS5 processor, a RISC-V implementation, and synthesized using both 45 nm CMOS and 7 nm FinFET technologies to assess its area trade-offs. The higher impact in area is observed on 7 nm, with 16.7% increase in transistor count, a marginal increase of 0.73% in the ALU and only 0.031% in the complete RS5 processor. This demonstrates that robust circuit design can be achieved with minimal impact on the overall silicon area, even in advanced technology nodes. Thus, the results obtained demonstrate that inverter-based robustness techniques offer concrete benefits for the simultaneous mitigation of process variability and radiation effects in FinFET devices.

**Keywords:** Process Variability. Circuit Level Hardening Techniques. FinFET Devices.

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## LIST OF SYMBOLS

| | |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DCELL | Decoupling Cells |
| DWC | Duplicate With Compare |
| eV | Work Function |
| FET | Field-effect transistor |
| FinFET | Fin-Shaped Field Effect Transistor |
| HFIN | Fin Height |
| H-Level | High-level |
| IC | Integrated Circuits |
| LG | Gate Length |
| LET | Linear Energy Transfer |
| $LET_{th}$ | LET Threshold |
| L-Level | Low Level |
| LPST | Low Power Schmitt Trigger |
| MC | Monte Carlo |
| MGG | Metal Grain Granularity |
| NFET | N-channel Field-effect transistor |
| NT | Near-Threshold |
| PDK | Process Design Kit |
| PDP | Power Delay Product |
| PFET | P-channel Field-effect transistor |
| PPA | Parallel Prefix Adder |
| RCA | Ripple Carry Adder |
| RH | Rad-Hard |
| RPR | Reduced Precision Redundancy |
| SEE | Single Event Effect |
| SEFI | Single Event Functional Interrupt |
| SEL | Single Event Latchup |
| SET | Single Event Transient |
| SEU | Single Event Upset |
| SNM | Static Noise Margin |
| ST | Schmitt Trigger |
| TOX | Oxide Thickness |
| TMR | Triple Modular Redundancy |
| VLSI | Very Large Scale Integration |
| WFF | Work-Function Fluctuation |
| WFIN | Fin Width |

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# 1 INTRODUCTION

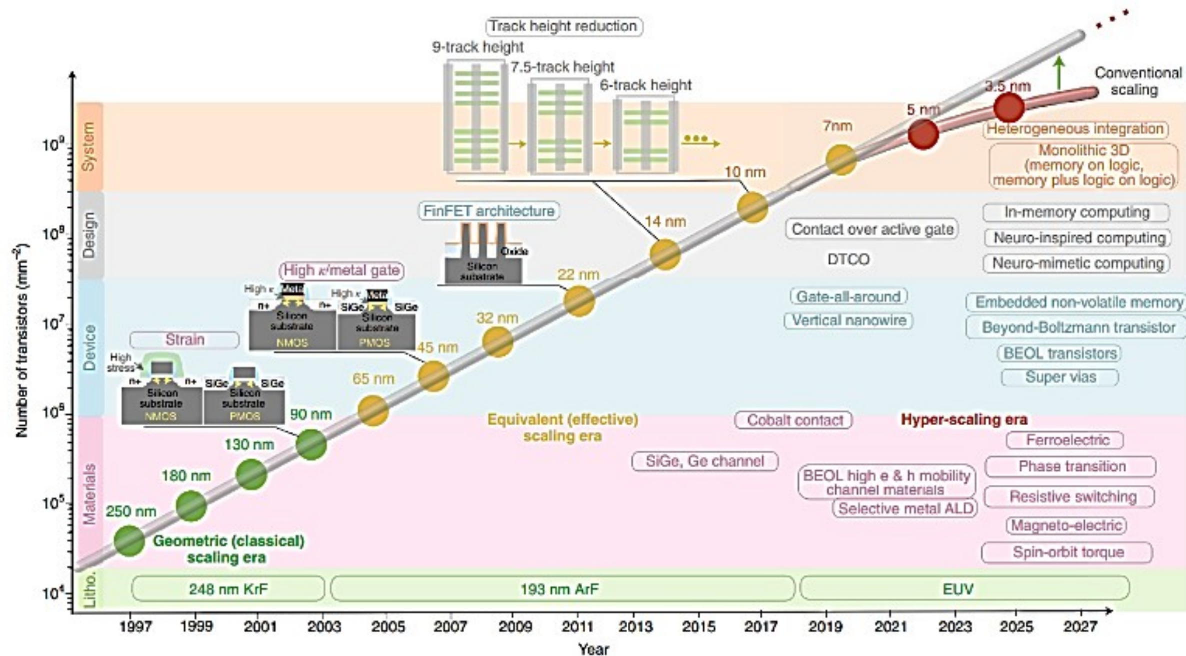
Modern society heavily depends on digital technology, and integrated circuits (IC) have become fundamental to nearly every essential infrastructure, from communication networks and transportation systems to industrial automation and personal electronic devices. As expectations for computational capability and energy efficiency continue to rise, the semiconductor industry responds through increasingly refined design and manufacturing techniques that allow more functionalities to be delivered by smaller and faster devices.

Over the past decades, this progress has been driven by the continuous miniaturization of transistors. According to Moore's Law [Moore 1998], the number of transistors integrated into a chip doubles approximately every two years, leading to an exponential increase in computational capability while simultaneously reducing manufacturing costs. However, recent technology generations no longer strictly follow the historical two-year scaling cadence, as physical and manufacturing constraints increasingly limit traditional transistor scaling, while the same technological evolution also introduces new design challenges. As devices shrink, their physical behavior becomes more complex, and each new technology generation must address limitations that were less significant in earlier nodes.

FinFET technology represents the technological evolution of classic bulk CMOS devices, also known as planar transistors, which has been part of the manufacturing of integrated circuits for several decades. Transistors have been continuously reduced in size over the years, bringing the advantages of reduced energy consumption per transistor and reduced delays, reflected in the increase in operating frequency. Also, the reduced scale allows the increase in the density of components in the same area, thus increasing the functionalities that can be designed while respecting power, performance and area restrictions. However, the nanometer scale of the planar transistors reduces the controllability of the gate over the channel charge and disturbs the flow of charge through the channel, causing the short channel effect. The impact of this effect deteriorates the performance of the device and makes it unsuitable for scaling below 20 nm [Pal, Sharma & Dasgupta 2017].

Figure 1 shows the evolution and future trend of transistor density scaling. The figure shows the evolution of technologies and materials adopted in the lithography and device manufacturing stages, as well as the types of devices and trends for the coming years. The distinct eras of scaling, geometric (or classical) scaling and equivalent (or effective) scaling stand out. The era of geometric scaling is characterized by proportional scaling of various aspects of the transistor such as gate oxide, channel doping, junctions and physical gate length. The current era of equivalent scaling has established the use of new materials such as silicon-germanium and introduced non-planar device structures, such as FinFETs, which scaled the effective mobility, the electrical gate oxide thickness and the effective transistor width. During this time, the effective oxide thickness decreased [Chau et al. 2004], and the effective width of the smallest transistor, defined mainly by the fin height and fin pitch, has increased [Doyle et al. 2003].

Figure 1 – Evolution of transistor density scaling.




Source: [Salahuddin, Ni & Datta 2018].

The transition from planar CMOS to FinFET devices addressed many limitations of geometric scaling, yet it did not eliminate several fundamental challenges associated with the continuous evolution of integrated circuits [Duan 2024]. As technology nodes advance, the cost of VLSI (Very Large Scale Integration) design increases significantly due to the growing complexity of fabrication, verification and testing. At the same time, circuits become more susceptible to both permanent and transient faults, which intensifies the need for robust reliability strategies. Furthermore, propagation delay no longer scales proportionally with frequency, and long interconnects require multiple clock cycles to traverse the chip. These effects reveal that the progression of semiconductor technology introduces not only performance opportunities but also a set of critical reliability and design challenges. As a consequence, integrated circuits must be designed with the expectation that faults will occur, since manufacturing imperfections coexist with increased sensitivity to noise and radiation effects [Azambuja, Kastensmidt & Becker 2014].

Among the factors that contribute to fabrication complexity, process variability stands out as one of the most critical challenges. The effects of process variability are undeniable and relevant to be considered in the digital design of nanometer circuits [Zimpeck et al. 2021]. The main source of process variability in FinFET devices is related to metal gate granularity, which affects the work-function provoking the effect named work-function fluctuation (WFF). This fluctuation affects the expected behavior of the Ion and Ioff device currents and propagation times due to the impact on the threshold voltage [Zimpeck et al. 2021].

In addition to the effects introduced by process variability, FinFET technologies are also increasingly sensitive to radiation induced disturbances. The continuous reduction in supply voltage and in the capacitance of internal nodes decreases the amount of charge required to flip a logic state, which makes transistors more vulnerable to single event transients generated by energetic particles. As a result, even small charge deposits can generate glitches that may propagate through logic paths and compromise the correct operation of nanometer circuits [Aguiar et al. 2025]. This growing susceptibility reinforces the relevance of circuit level techniques that were originally proposed for noise or radiation mitigation and highlights their potential role in improving the robustness of FinFET-based designs.

Some of these transistor-level or circuit-level approaches proposed for noise and SET mitigation can also be explored to mitigate process variability impact [Toledo, Reis & Meinhardt 2019] [Moraes et al. 2021]. In [Moraes et al. 2021], the relationships between transistor sizing, supply voltage, and process variability are evaluated on 7 nm FinFET Schmitt Trigger (ST) Inverters to get a low energy consumption circuit while still keeping low levels of deviations due to the impact of process-induced variability. These evaluations primarily concern the hysteresis ST design challenge. In [Toledo, Reis & Meinhardt 2019], a set of circuit level hardening techniques applied to inverters is investigated concerning the process variability effects on a bulk CMOS technology showing that these techniques demonstrate potential to mitigate the effects of variability, but may introduce drawbacks such as power and timing degradation. However, these mitigation approaches have not yet been evaluated considering FinFET devices and recent technology nodes. Although several circuit-level mitigation techniques have been proposed to address noise, process variability, or radiation effects individually, their behavior under the combined influence of process variability and single-event transients in advanced FinFET technologies remains insufficiently explored. In particular, the effectiveness, trade-offs, and system-level implications of inverter-based hardening techniques under such conditions are still open research questions.

## 1.1 OBJECTIVES

In this context, to evaluate the research gap about the behavior of the inverter-based circuit-level mitigation approaches, this dissertation has as main objective:

- Examine circuit-level hardening techniques to jointly mitigate the effects of process variability and radiation.

The development of the proposed dissertation also provides some secondary results:

1. A review about the inverter-based circuit-level hardening techniques
2. An evaluation of hardening techniques under nominal and near-threshold conditions with regular behavior.

3. An analysis of process variability under a range of work-function fluctuation conditions.
4. A comparative discussion of the impact of work-function fluctuations on FinFET devices related to bulk CMOS technology.
5. A panorama view of the consequences of adopting the evaluated circuit level techniques on the SET effects considering process variability.
6. An application of these circuit-level techniques on the synthesis of a RISC-V design to evaluate area drawbacks.

## 1.2 WORK ORGANIZATION

The structure of this work is organized as follows:

**Chapter one** introduces the technological context of FinFET devices, discusses the challenges associated with miniaturization of technology, and presents the motivation for analyzing the combined influence of process variability and radiation effects. It also outlines the main and secondary objectives of this work.

**Chapter two** provides the necessary background on FinFETs, process variability, single event effects and the Quasar tool, offering a conceptual foundation for understanding the reliability concerns addressed throughout the dissertation.

**Chapter three** reviews related work on inverter-based circuit level hardening techniques and highlights previous attempts to mitigate the effects of noise, radiation, and variability. It also positions the current research within the broader literature.

**Chapter four** presents the methodology adopted in this dissertation. It details the design flow used in the study, describes the experimental setup, and explains the modeling choices and simulation parameters employed for both electrical and statistical analyses.

**Chapter five** evaluates the impact of process variability on the selected inverter based hardening techniques. It examines regular behavior, analyzes variability under different work-function fluctuation scenarios, and compares the findings with previous results reported for bulk CMOS technologies.

**Chapter six** focuses on the influence of single event transients on the same inverter topologies. It introduces the simulation flow used to quantify radiation robustness, examines the effects of variability on the LET threshold, and discusses how the interaction between variability and SETs affects circuit reliability.

**Chapter seven** extends the study to a system level perspective by analyzing the integration of the evaluated hardening techniques into arithmetic circuits of a RISC V design. It presents the electrical and statistical results and discusses the corresponding area impact in both 45 nm and 7 nm technologies.

Finally, **Chapter eight** summarizes the main conclusions of the dissertation, outlines the contributions achieved, and discusses possible directions for future work.

# 2 BACKGROUND

The development of this work involves some different concepts about reliability and technology. This section is intended to help the reader to become more familiar with the most relevant topics for the general understanding of the discussions provided in this work. The section starts by providing a overview about the FinFET technology differences from the planar CMOS devices. After that, we introduce the main sources of process variability in metal-gate devices. In the sequel, the chapter addresses the radiation-faults concepts and evaluation tool, focusing on the type of fault (SET) and evaluation tool (Quasar) considered in this work methodology.

## 2.1 FINFET TECHNOLOGY

Fin Field-Effect Transistors, commonly known as FinFETs, are non-planar transistors where the conducting channel is surrounded by a “fin”, which is a thin silicon structure. Historically, the first mention to a FinFET device appeared in 1989 in a paper published by [Hisamoto et al. 1989]. After that, the first circuit demonstrated with FinFETs was given by [Rainey et al. 2002], with a 4-stage inverter. These works demonstrated the potential of multigate devices with technology up to 20 nm. Currently, industry and research already reach the scale of 2 nm and below devices [TSMC 2026], due to the change of planar for multigate devices.

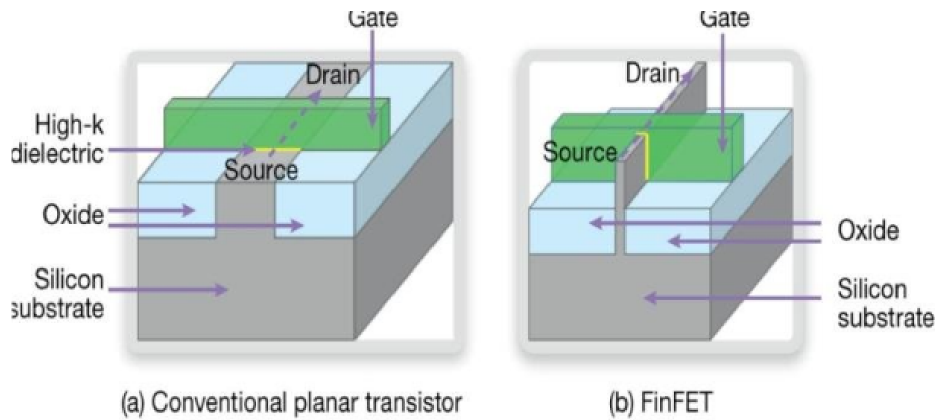
The scaling of FinFET devices is represented by the size of the “fin”, which is determined by the effective channel length of the device. The channel width of the FinFET is defined in terms of the height of the fin, which is known as the quantization width. Consequently, the charge flow in the FinFET can be improved by increasing the number of fins in the structure, which provides better gate control of the channel charge [Pal, Sharma & Dasgupta 2017].

The main differences between the conventional planar transistor and the FinFET are their three-dimensional structure, while the planar transistor is two-dimensional, with the silicon fins projecting vertically from the silicon substrate and the gate completely enclosing the fin. Figure 2 below shows a planar transistor and a FinFET transistor for comparison.

FinFETs have several advantages such as minimal power consumption, immunity to short channel effect, smaller area requirements and higher operating speed [Hisamoto et al. 2000]. However, they also have to deal with a variety of challenges. FinFET structures have more parasitic capacitances compared to planar structures, which impacts static timing analysis methodologies [Meinhardt 2014]. Figure 3 shows an example of how the parasitic capacitance of FinFET is accounted for for a 2-fin device. The additional overlap area increased at the front gate and back gate increases the device capacitance. The increase in fin height helps to reduce the parasitic capacitance of the device [Kang et al. 2013].

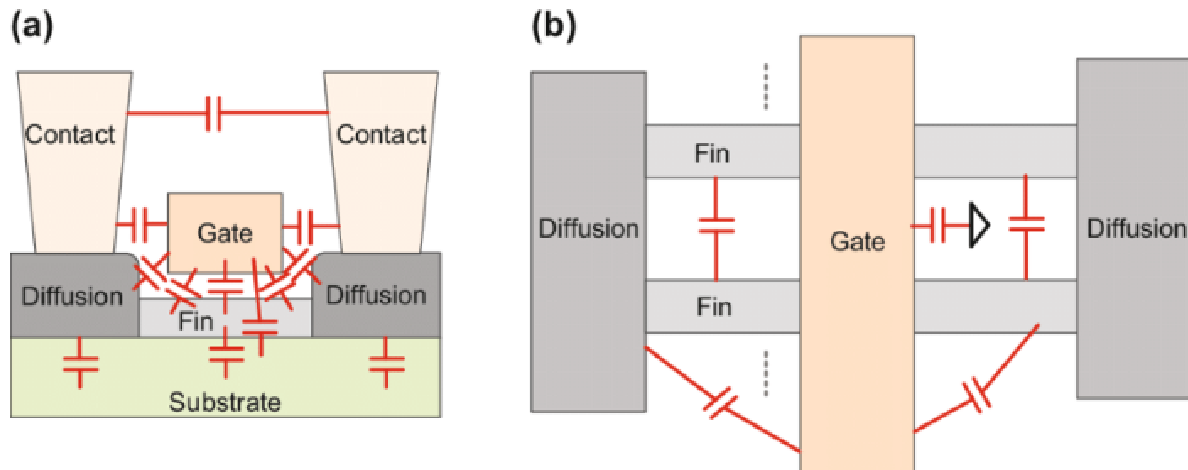
FinFETs offer superior channel control, but remain sensitive to process, voltage, and temperature (PVT) variations. Variability in gate length, fin thickness, work function, and oxide thickness can significantly influence delay and energy consumption in logic circuits. As device

Figure 2 – Conventional planar transistor versus FinFET.




Source: [Kumar et al. 2019].

Figure 3 – Capacitance components for a FinFET device: (a) cross-sectional view and (b) top view




Source: [Guo & Stan 2020]

dimensions continue to shrink, random dopant fluctuations, which strongly impacted planar transistors, become less dominant, but new reliability concerns emerge. One major issue is self-heating, the fin is surrounded by gate dielectric rather than being in direct thermal contact with the substrate, so, heat dissipation becomes less efficient, making FinFETs more susceptible to temperature-induced performance degradation [Amrouch et al. 2019].

Even with the challenges introduced by their three-dimensional structure, FinFET architectures resolve many of the limitations observed in planar MOSFETs. Their strong gate control and suppression of short-channel effects reduce the influence of parasitic variations, and the ability to employ a thicker gate oxide allows aggressive gate-length scaling while keeping leakage manageable, enabling higher density and improved energy efficiency. Additionally, FinFETs also have a lower intrinsic sensitivity to short-channel degradation and reduced vulnerability to single-event transients [Seifert et al. 2012]. However these devices are still sensitive to radiation and noise problems [Zimpeck et al. 2021]. Compared to planar CMOS devices, FinFETs generally exhibit improved electrostatic control and smaller sensitive volumes, which

can reduce charge collection efficiency during a particle strike. However, aggressive scaling, reduced supply voltages, and lower node capacitances significantly decrease the critical charge required to produce a transient [Seifert et al. 2012]. As device scaling continues and lithography challenges persist, it becomes increasingly important to consider strategies to mitigate the radiation and noise effects on digital designs, particularly for critical applications.

## 2.2 PROCESS VARIABILITY

Variability in integrated circuits can be classified into three main categories: environmental, reliability-related, and physical sources [Brendler et al. 2018]. Environmental variations arise during circuit operation and typically include fluctuations in supply voltage and temperature.

Reliability-related variations stem from device aging mechanisms, which are aggravated by the high electric fields present in modern technologies [Zimpeck, Meinhardt & Reis 2014]. Physical variability is associated with deviations in geometric and electrical parameters introduced during fabrication and is commonly referred to as process variability.

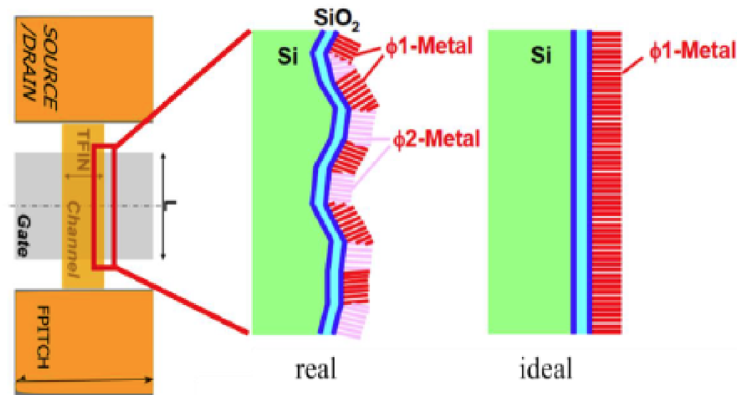
As transistor dimensions continue to shrink, controlling these variations during the manufacturing process becomes increasingly difficult, reducing predictability in nanometer-scale circuit performance and directly affecting timing, power, and functional behavior, impacting circuit operation and reliability.

Process variability originates primarily from lithographic limitations and material imperfections. Such deviations cause circuits fabricated on the same wafer to differ in electrical characteristics, potentially leading to timing degradation, unexpected power consumption, or accelerated device wear-out. In bulk CMOS technologies, random dopant fluctuation has historically been one of the dominant contributors to threshold voltage shifts and drive current variations, especially through changes in channel length [Meinhardt 2014].

In FinFET technologies, however, the lightly doped channel largely suppresses dopant-induced variability. As a result, geometric parameters such as gate length, fin height, fin width, and silicon thickness become more influential in determining device behavior.

Although geometric variations remain significant contributors to device dispersion, advanced FinFET nodes are predominantly affected by metal gate work-function fluctuations (WFF). Because the gate is composed of polycrystalline metal, differences in grain orientation lead to local variations in surface potential, a phenomenon known as metal grain granularity (MGG). These fluctuations introduce threshold voltage variability and significantly impact $I_{ON}$ and $I_{OFF}$ currents [Zimpeck, Meinhardt & Reis 2014]. While an ideal fabrication process would produce uniformly aligned metal grains with minimal variation, real manufacturing conditions result in gates composed of grains with different work functions, as shown in Figure 4, increasing the magnitude of WFF and making it the dominant source of process variability in sub-20 nm FinFET technologies. The parameter exhibits a strong correlation between the variability of $I_{ON}$ and $I_{OFF}$ currents and the threshold voltage fluctuation in the presence of MGG.

Figure 4 – Metal Gate Granularity Representation




Source: [Zimpeck, Meinhardt & Reis 2014]

## 2.3 RADIATION FAULTS

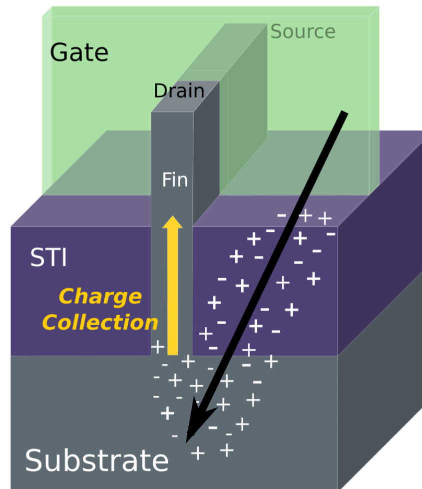
Ionizing radiation is an inherent component of both natural and artificial environments and its interaction with semiconductor devices is a central concern in the reliability analysis of modern integrated circuits. As technology nodes continue to downscale and operating voltages decrease, the charge required to disturb or modify the electrical state of a device becomes progressively smaller. In parallel, the density of transistors increases and the intrinsic electrical margins that once masked transient disturbances are reduced, making circuits more susceptible to radiation induced effects [Baumann 2002].

Radiation environments relevant to electronic systems include space, the terrestrial atmosphere and accelerator facilities. In the near Earth space environment radiation originates mainly from solar energetic particle events caused by solar flares and coronal mass ejections, from galactic cosmic rays originating outside the solar system, and from the trapped particles that constitute the Van Allen belts.

These sources vary significantly in energy spectrum and particle composition and produce diverse effects on devices depending on the orbital altitude and shielding conditions. At ground level secondary neutrons generated by cosmic ray interactions with the atmosphere represent the dominant cause of radiation induced soft errors in commercial electronics [Ziegler & Lanford 1979]. In accelerator environments high energy particles produced by interactions along the beam line create controlled but intense radiation fields that are often used to characterize the response of electronic components.

Regardless of the environment, the mechanism that triggers a fault begins with the interaction between an ionizing particle and the semiconductor material, as seen in Figure 5. As a particle traverses the sensitive volume of a device it loses energy primarily through ionization, generating a dense track of electron hole pairs along its path, as illustrated in Figure 6. This process is well described in models of Linear Energy Transfer (LET) which quantify the energy deposited per unit distance by the incident particle.

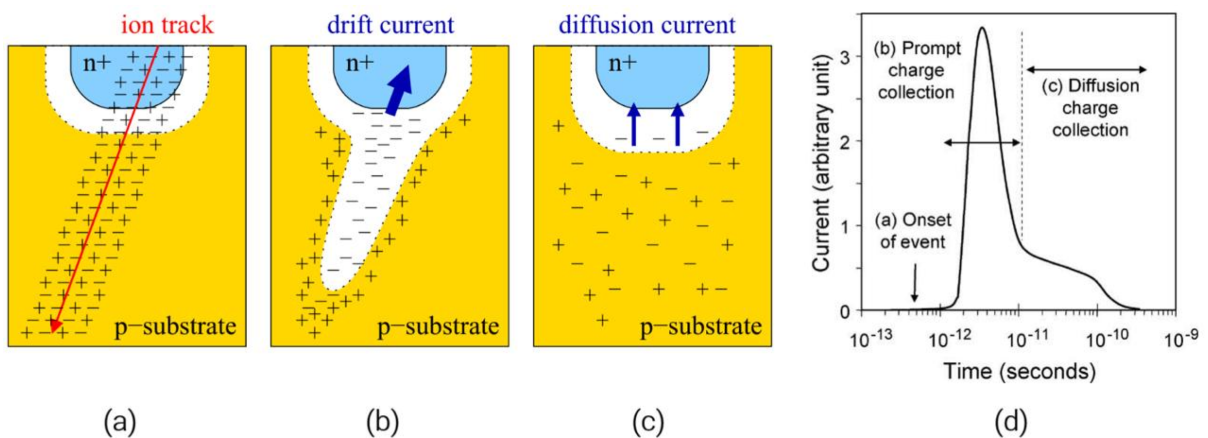
Figure 5 – Strongly ionized particle colliding with a transistor.




Source: [Lee et al. 2015]

The generated charges may then be collected by drift when located inside or near the depletion region of a reverse biased junction or by diffusion when excess carriers migrate from a region of low electric field toward a nearby junction. In scaled technologies charge sharing becomes an important phenomenon since several adjacent transistors may collect portions of the same charge cloud. The total amount of collected charge and the resulting current pulse depend not only on the device geometry and the strength of the internal electric fields, but also on the particle characteristics, such as its type, energy, angle of incidence, and impact location, as well as on circuit-related parameters, including the capacitance of the struck node [Aguiar et al. 2025].

Figure 6 – Charge Generation and Collection Process

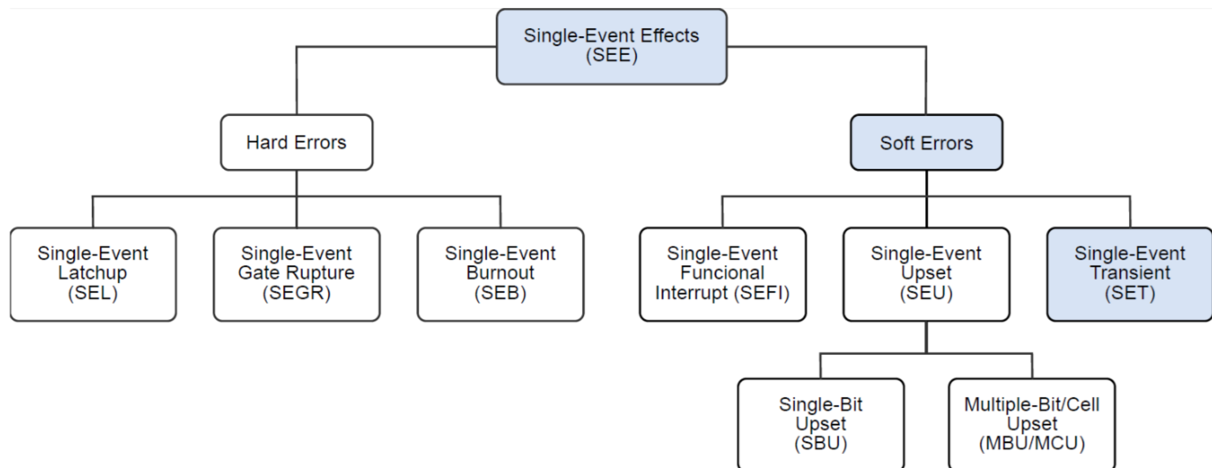



Source: [Baumann 2002]

These interactions are known as Single Event Effects. The term refers to any observable disturbance produced by the interaction of a single ionizing particle with an electronic device [Ferlet-Cavrois, Massengill & Gouker 2013]. Classical taxonomies, indicated in Figure 7, describe several categories including Single Event Upset (SEU) which corresponds to the

unintended change of state in a memory element, Single Event Latchup (SEL) which is the activation of parasitic structures that produce a high current path, Single Event Functional Interrupt (SEFI) which causes the temporary loss of functionality of a subsystem, and Single Event Transient (SET) which is the generation of a voltage glitch in a combinational logic path. Although these categories differ in manifestation they share a common origin: the localized deposition and collection of charge in a sensitive node.

Figure 7 – Classification of Single-Event Effects




Source: [Slayman 2010]

Among these effects Single Event Transients have acquired increasing relevance because their occurrence is strongly amplified by technology scaling. A Single Event Transient corresponds to a temporary perturbation in the output of a combinational gate caused by the current pulse generated during a particle strike. The resulting voltage disturbance propagates through the logic network and may or may not be captured by a sequential element. The likelihood that a transient becomes a functional error depends on three masking mechanisms. Logical masking occurs when the Boolean function of the circuit prevents the perturbation from affecting the output. Electrical masking arises when attenuation due to resistive and capacitive loading decreases the amplitude or duration of the glitch as it travels through successive gates. Temporal masking depends on the position of the transient relative to the sampling window of the receiving register. These effects historically provided strong mitigation, but in nanoscale devices their effectiveness is reduced because the drive strength of transistors is lower, node capacitances are smaller and path logical depths are shallower, which increases the probability that a transient pulse will propagate without significant attenuation [Shivakumar et al. 2002].

The relevance of SETs in modern electronics is further reinforced by the reduction of critical charge which is the minimum charge required to alter a node voltage sufficiently to affect circuit behavior [Baumann 2002]. As critical charge decreases, particles with low linear energy transfer can induce transients. Moreover, the combined effect of low supply voltages and aggressive device scaling amplifies the impact of small variations in deposited charge, making circuits more vulnerable not only to high energy cosmic rays but also to atmospheric radiation

present at ground level.

In the design of radiation robust inverters, considering single event transients, the part which is most sensitive to disturbance is the drain node of a transistor in "off" state, connected directly to the output node [Calomarde et al. 2014]. There are some circuit level hardening techniques proposals in the literature for noise and SET mitigation [Calomarde et al. 2014] [Rathod, Saxena & Dasgupta 2009] [Dokic 1984]. These works explore the following assumptions, which drive a series of area optimizations: 1) Some area optimizations could be obtained considering the frequency dependency of soft error rates [Sugisaki et al. 2023] and the single-effects cross-section characteristics [Xiong et al. 2021]. Therefore, the number and the probability of disturbances depend on the number of drains and of their size when connected directly to the output; and 2) to reduce area overhead it is not necessary to include all the original pull-up or pull-down logic networks in the circuit level hardening approach, only those values that are not logically masked in the circuit should be added.

## 2.4 QUASAR

Quasar is an electrical level evaluation tool designed to automate and accelerate the characterization of how digital circuits respond to radiation induced transient faults under process variability [Sandoval et al. 2025]. Traditional SET analysis relies on large numbers of SPICE simulations to identify which fault scenarios lead to an observable error at the circuit outputs. As circuits become more complex and process variations become more pronounced, this brute force approach becomes increasingly time consuming. Quasar addresses this challenge by structuring the evaluation as a sequence of abstraction layers that combine logical filtering, optimized electrical simulations and prediction-based techniques. This design enables the tool to determine robustness metrics such as the critical Linear Energy Transfer required to generate an error in each sensitive configuration of a circuit. In this work, Quasar is adopted to identify the most sensitive nodes and to determine the critical LET threshold under process variability conditions.

Quasar receives a SPICE netlist describing a combinational circuit and explores every configuration in which a Single Event Transient may be generated and potentially propagate to an output. For each configuration, it emulates the transient current injected at the struck node following standard SET current pulse models. The simulation infrastructure is independent of technology, transistor model and SPICE engine, allowing the tool to operate with both open source and proprietary simulators. By abstracting SET generation into a parameterized current source, Quasar can search for the minimum current amplitude, and thus the critical LET, required to produce a voltage excursion at the output large enough to invert its logic state.

For valid fault scenarios, Quasar determines the critical LET using a root search formulation. The output voltage is viewed as a monotonic function of the injected current pulse amplitude, making it possible to apply numerical methods to find the current that places the output at the switching threshold. Earlier versions of the tool adopted binary search, whereas the

most recent implementation employs a false position algorithm that further reduces the number of required simulations by exploiting the near linear behavior of the voltage response close to the threshold.

Once the critical LET is computed for all valid configurations, Quasar produces a detailed robustness profile of the circuit. This characterization can reveal which nodes are most sensitive and how the topology influences fault propagation paths.

Building on this structure, the tool also integrates a variability evaluation framework. Process variability parameters such as threshold voltage shifts or work function fluctuation can be sampled across a distribution, and multiple circuit level evaluations are performed to assess how these variations affect the critical LET values. To reduce computational effort, Quasar incorporates a k nearest neighbors regression model that predicts the sensitivity for a large portion of the sampled points, requiring electrical simulation only for a subset of them. This approach reduces variability evaluation time by approximately a factor of two.

## 3 INVERTER-BASED CIRCUIT-LEVEL MITIGATION TECHNIQUES

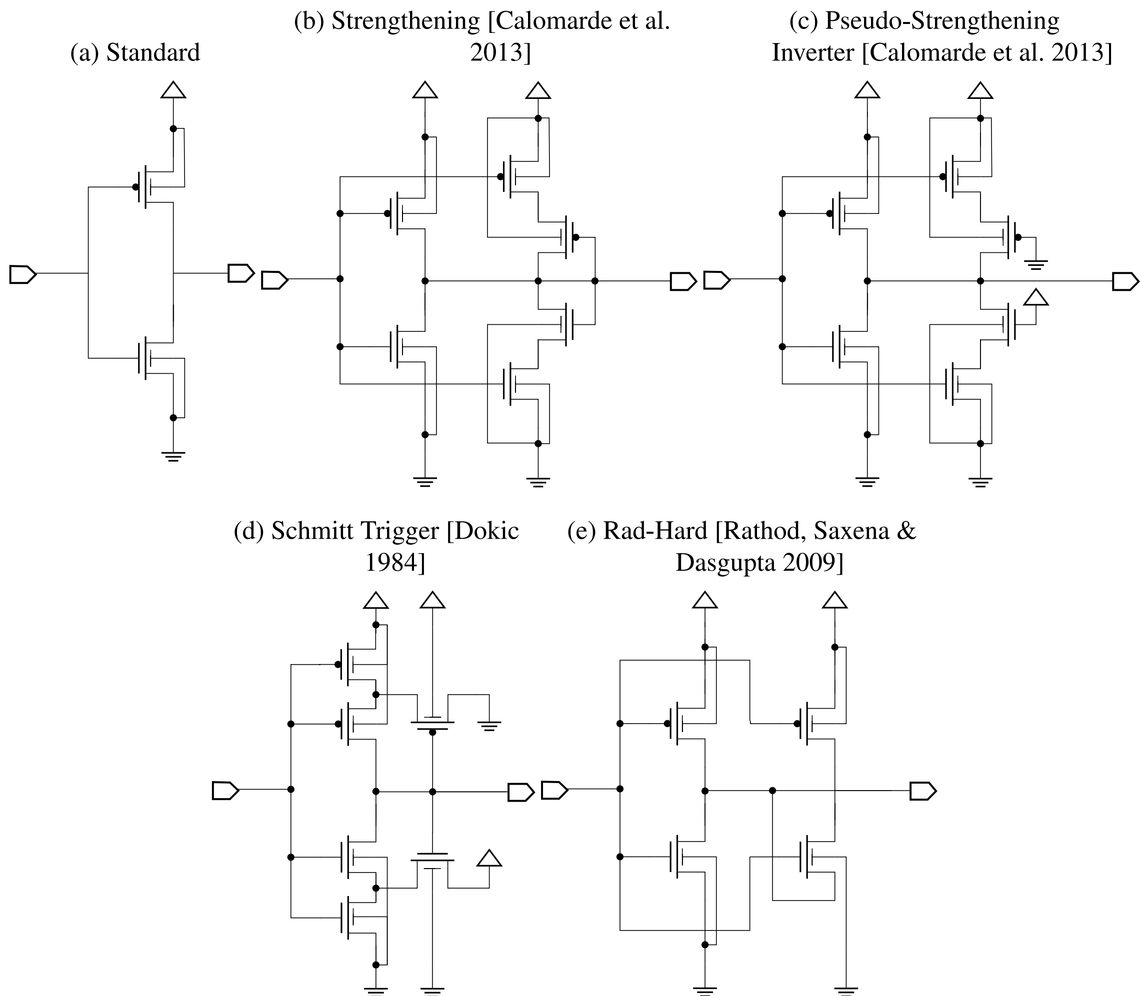
Techniques originally proposed for noise suppression and single-event transient mitigation have long been used to improve the reliability of digital circuits. These approaches remain relevant in modern nanometer technologies. Approaches such as Triple Modular Redundancy [Neumann 1956] (TMR), Duplicate with Compare (DWC) [Quinn et al. 2016], and Reduced Precision Redundancy (RPR) [Garcia-Astudillo et al. 2020] aim to filter or mask transient disturbances, but their architectural or system-level overheads often make them impractical for area and energy-constrained designs. These limitations motivate the use of circuit-level hardening strategies, which strengthen the robustness of logic gates without the high cost of large-scale redundancy [Zoellin et al. 2008]. Within this context, inverter-based modifications have emerged as effective mechanisms for attenuating or blocking transient pulses and for improving tolerance to parameter fluctuations inherent to advanced technology nodes.

Traditional circuit-level hardening techniques are inspired by noise-control approaches that have shown considerable effectiveness in mitigating SETs in robust designs. Some of these circuit-level hardening techniques are based on the insertion of inverter-based circuits at critical points of a design [Toledo, Reis & Meinhardt 2019]. This work begins by evaluating four of these techniques applied to the traditional inverter structure presented in Figure 8: Schmitt Trigger (ST) [Dokic 1984]], Pseudo-Strengthening [Calomarde et al. 2013], Strengthening [Calomarde et al. 2013], and Rad-Hard [Rathod, Saxena & Dasgupta 2009]. These circuits are selected to enable evaluation of process variability in FinFET devices relative to the bulk CMOS transistors described.

Schmitt Triggers (ST) are commonly used as internal circuits on systems to provide enhanced noise tolerance, and robustness against random variations in the input waveform [Dokic 1984] [Kader et al. 2012]. The original circuit is presented in Fig.8 (d). Traditional inverters, presented in Fig. 8(a), switch their binary value simultaneously on both rising and falling edges. A slow rising edge near the threshold can cause frequent switching, requiring current from the power supply and potentially inducing voltage drops that shift the threshold voltage. This shift can lead to continuous switching or oscillation, exacerbated by input noise. Schmitt Triggers (STs) address these issues by introducing upper and lower threshold voltages to filter noise effectively.

STs circuits present a hysteresis characteristic. If the input level is within the hysteresis region, the ST shall not switch. Such characteristic gives a higher static noise margin (SNM) in comparison to traditional inverters, ensuring a high noise immunity. A variety of CMOS STs has been proposed and implemented over the years based on different requirements. In this work, we consider the Low-Power Schmitt Trigger (LPST) [Dokania & Islam 2015]. It is designed for operation at a supply voltage of 0.4V to achieve low power consumption and consists of two inverters where the output from the second one will be the bulk for the first one.

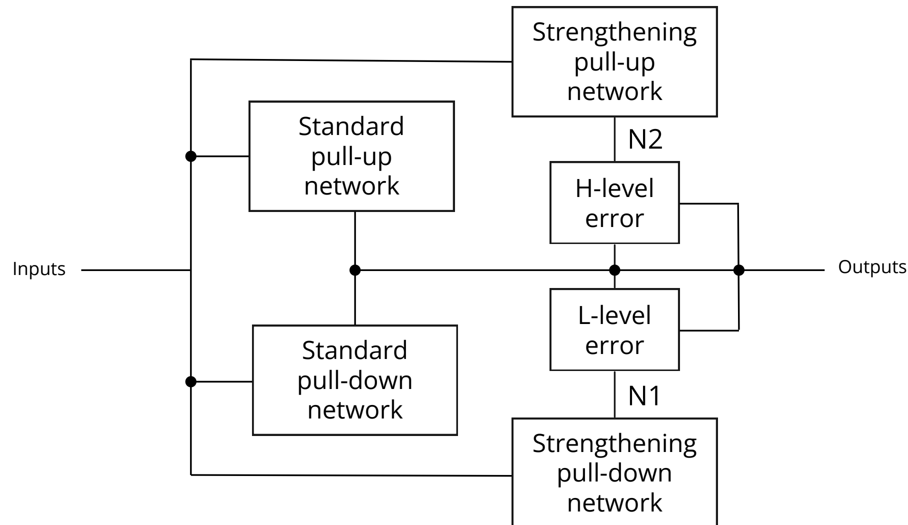
Figure 8 – Standard CMOS Inverter, adopted as baseline in this work, and Hardening Inverter Topologies




Source: The author.

The Strengthening and Pseudo-Strengthening circuits are presented in Fig. 8 (b) and (c), respectively. These circuits explore the Strengthening concept, detailed in Figure 9. This concept was introduced to make logic systems more robust to noise and radiation effects [Calomarde et al. 2014]. In this approach, a static CMOS gate includes inserted replicas of its pull-up and pull-down networks. Thus, the output node is also controlled by two additional networks: "High-level (H-level) error" for the pull-up network and "Low-level (L-level) error" for the pull-down network. These error blocks monitor the outputs, and if an output changes to the opposite level, or tries to, these blocks connect the Strengthening network to the output to recover the correct value. In all other situations, both H-level and L-level error networks remain off (i.e., high impedance). Strengthening networks force the logical value whenever there is any error (soft or single event) and can be as complex as the original network. To implement the "level error" networks, several configurations are available, but to avoid introducing more sensitive nodes, a network with the minimum number of elements should be used. Under this constraint, the most basic element to carry out the function of the "error block" is a simple transistor.

Figure 9 – Strengthening Concept.




Source: [Calomarde et al. 2014].

The difference between Pseudo-Strengthening and Strengthening is in their inserted replica, where in Pseudo the drain and gate signals are supplied by ground and VDD respectively.

The Rad-Hard inverter [Rathod, Saxena & Dasgupta 2009], presented in Fig. 8 (e), mitigates the noise and SET effects by a mechanism that more efficiently turns the inverter "off". When the input is at high level, the extra PFET device is "off", and the input NFET device is "on", thus, the initial circuit operation is not affected. This approach may turn the inverter slower, however, this can be overcome by doubling the size of each NFET device. On the other hand, when the input is at low level, the extra PFET transistor pulls up the node where the drains of these extra PFET and the extra NFET are connected to a high level. As a consequence, the pull down network of the traditional inverter is turned "off".

These four inverter-based circuit-level techniques are the selected approaches for further investigation in this dissertation. Some of them have been previously explored to noise mitigation, to reduce the process variability impact, or to increase the radiation robustness of combinational cells. The next section will address the most relevant literature related to these mitigation strategies in the view of the goal of this dissertation.

## 3.1 RELATED WORK

The circuit-level techniques based in the inverter behavior described in the previous section have been investigated in the context of radiation or noise mitigation in a limited set of other research; however, the evaluation of these approaches still presents some open questions relevant to the nanometer design of robust circuits. In addition, other techniques can also be found in the literature exploring capacitance-based approaches, such as the adoption of decoupling strategies [Oliveira, Schvittz & Meinhardt 2025], increasing the load size [Dhillon

et al. 2006], insertion of charge sharing logic [Azimi, Du & Sterpone 2018] or the C-element architecture [Toro et al. 2014] and a insertion of a guard gate filter [Shuler et al. 2006] [Balasubramanian et al. 2005]. The C-element architecture also provides detection and correction capabilities [Toro et al. 2014]. As a time definition of the scope of this work, the focus of the dissertation is defined to the circuit-level techniques due to the reduced impact on area and ease of inserting them in different cells from a standard cell library, despite the capacitive-based approaches that will demand a more detailed evaluation of the impact on the final area of the circuits. It is important to note that many commercial standard cell libraries have included some of these techniques in the cells available to designers, such as the C-element, adopted for different optimization objectives, for example, in the design of asynchronous circuits [Moreira 2011].

In this context, Table 1 summarizes key related work and the techniques they adopt to mitigate process variability and SET effects. The table outlines approaches such as gate upsizing, the insertion of rad-hard inverters, Schmitt triggers, and decoupling cells, highlighting how different authors combine these methods according to their objectives. For example, [Dokania & Islam 2015] focuses on process variability mitigation through the use of Schmitt triggers, while [Toledo, Reis & Meinhardt 2019] leverages both rad-hard inverters and Schmitt triggers as mitigation strategies.

A broader perspective is presented in [Zimpeck et al. 2021], which integrates Schmitt triggers and decoupling cells with additional SET-oriented techniques, addressing variability and transient events in a unified manner. The work in [Oliveira, Schvittz & Meinhardt 2025] distinguishes itself by leveraging gate upsizing and decoupled cells to effectively mitigate SETs.

In parallel, [Andjelkovic 2022] conducts a comprehensive evaluation, characterizing a wide range of SET mitigation techniques, including gate upsizing, duplication, Schmitt triggers, decoupling cells, and other gate-level strategies, and systematically quantifying their impact on robustness, delay, and power.

Building on these insights, the present dissertation adopts an inclusive approach by evaluating all four inverter-based techniques, namely Strengthening, Pseudo Strengthening, Schmitt Trigger, and Rad Hard, to assess their combined potential for reducing both process variability and SET sensitivity.

Table 1 – Overview of Related Works on Process Variability and SET Mitigation Techniques

| **Work** | Gate Upsizing | Insertion of Rad-Hard | Insertion of ST | Decoupling Cells | Process Variability | SET Mitigation |
|---|---|---|---|---|---|---|
| Rathod, 2009 | | X | | | | X |
| Dokania, 2015 | | | X | | X | |
| Moraes, 2018 | | | X | | X | |
| Toledo, 2019 | | X | X | | X | |
| Zimpeck, 2021 | | | X | X | X | X |
| Andjelkovic, 2022 | X | | X | X | | X |
| Oliveira, 2025 | X | | | X | | X |
| **Proposed Work** | X | X | X | | X | X |

Source: The author.

# 4 METHODOLOGY

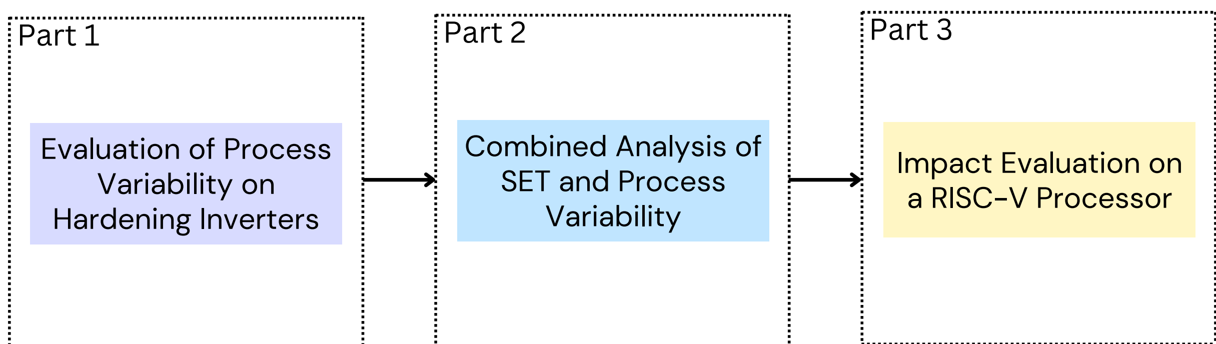
This work defines a development flow, presented in Fig. 10, to achieve the main objective of evaluating the mitigation achievements of inverter-based circuit-level techniques against process variability effects, also considering radiation effects. This flow is divided into three main parts:

1. An evaluation of the impact on process variability considering four circuit-level techniques and adopting FinFET devices [Dias & Meinhardt 2024].
2. The combined analysis of SET and process variability mitigation due to the circuit-level techniques considered [Dias et al. 2026] .
3. A discussion about the drawbacks in the area of applying these circuit-level techniques in a RISC-V design [Dias et al. 2025].

The general definitions adopted in the three steps of the development flow are described in the next section. The following chapters detail the particular aspects of the development of each of the three parts, the results found, and also the main discussions and comparisons for each one of these development steps.

The initial phase of this work focused on establishing a solid theoretical background on FinFET technology and circuit-level variability mitigation techniques. The research began with a literature review on techniques for mitigating the effects of variability at the circuit level. This brief review identifies the work [Toledo, Reis & Meinhardt 2019] as one of the main related work on this topic among the literature on process variability and SET mitigation techniques.

Figure 10 – Three main parts of this work.




Source: The author.

## 4.1 GENERAL EXPERIMENTAL SETUP

The methodology for the general evaluation adopts the 7nm FinFET ASAP Physical Design Kit (PDK) [Clark et al. 2016] as the technology node. The transistor models used in all

simulations are the regular-threshold devices (RVT), and the main parameters are presented in Table 2. In this technology, the nominal supply voltage is 0.7 V. Simulations without variability were also conducted for comparison. We compare the behavior of the circuits under regular operating conditions, without process variability and SET faults, which defines the regular behavior, with that of the circuits under evaluation (with process variability, under SET effects).

Table 2 – Parameters applied in the electrical simulations

<table>
<tr><th colspan="2">Parameter</th><th colspan="2">7nm</th></tr>
<tr><td colspan="2">Nominal Supply Voltage</td><td colspan="2">0.7 V</td></tr>
<tr><td colspan="2">Gate Length (LG)</td><td colspan="2">21nm</td></tr>
<tr><td colspan="2">Fin Width (WFIN)</td><td colspan="2">6.5nm</td></tr>
<tr><td colspan="2">Fin Height (HFIN)</td><td colspan="2">32nm</td></tr>
<tr><td colspan="2">Oxide Thickness (TOX)</td><td colspan="2">2.1nm</td></tr>
<tr><td colspan="2">Channel Doping</td><td colspan="2">$1 \cdot 10^{16} cm^{-3}$</td></tr>
<tr><td colspan="2">Source/Drain Doping</td><td colspan="2">$2 \cdot 10^{16} cm^{-3}$</td></tr>
<tr><td colspan="2" rowspan="2">Work Function (eV)</td><td>NFET</td><td>4.372</td></tr>
<tr><td>PFET</td><td>4.8108</td></tr>
<tr><td rowspan="4">Threshold Voltage (V)</td><td rowspan="2">Saturation</td><td>NFET</td><td>0.17</td></tr>
<tr><td>PFET</td><td>-0.16</td></tr>
<tr><td rowspan="2">Linear</td><td>NFET</td><td>0.19</td></tr>
<tr><td>PFET</td><td>-0.19</td></tr>
</table>

Source: [Clark et al. 2016]

We evaluate the behavior by considering two transistor sizes, which means for a multi-gate device, such as FinFET, different numbers of fins are used in parallel:

1. the minimum device sizing: adopting 1 fin device to evaluate the highest sensitivity;
2. the recommended device sizing: adopting 3 fins per device, adhering to ASAP PDK recommendations.

All the inverter-based circuit-level techniques were described at the electrical level in SPICE language. The electrical simulations were performed using HSPICE electrical simulator from Synopsys. All circuits receive the input signal from a chain of inverters to simulate real inputs, and each circuit has an inverter of the same size connected to its output. The load at the output was modeled using a fan-out-of-four (FO4) inverter to ensure consistency across simulations.

In the process variability evaluation, we also consider the behavior at near-threshold voltage (NT), which is explicitly adopted for low-power applications, at 0.4 V. The evaluated temperature was 25°C (typical). The technology parameters are presented in Table 2.

All propagation delay and energy measurements were recorded for the two voltage operations (nominal and near-threshold). The delay is calculated as the worst-case propagation time across the outputs of all inverters. The energy is calculated by HSPICE itself, accounting for all current drive from the source voltage during all timing evaluations.

For these experiments, considering metal gate devices as the 7 nm FinFET devices, the dominant source of process variability is the metal-gate work-function fluctuation (WFF), which directly influences delay and power behavior. The effect of process variability on the WFF is electrically simulated through the Monte Carlo statistical method, modeling the WFF as a Gaussian distribution. In this work, the WFF was modeled to observe three scenarios about the process variability: a conservative, medium, and aggressive. For each of these levels of process variability, the Gaussian distribution is defined with a $3\sigma$ deviation from the nominal value, and variation levels of 1%, 3%, and 5%, respectively. For each inverter topology and for both device configurations (1-fin and 3-fins), 2000 Monte Carlo iterations were performed at each variability level [Zimpeck et al. 2021] [Artola, Hubert & Alioto 2014].

The data extracted from the Monte Carlo simulations are: mean ($\mu$), standard deviation ($\sigma$), variance ($\sigma^2$), coefficient of variation ($\sigma/\mu$), and minimum and maximum value. We also adopt the normalized standard deviation as a figure of merit to enable comparison of designs with different means and standard deviations. The coefficient of variation is used because it allows comparison of the variability of the parameter across different means, i.e., higher percentages indicate greater variation in the circuit with respect to delay and energy consumption. Finally, Power-Delay Product (PDP) analyses were also performed to evaluate the overall energy–performance trade-off.

In addition to the electrical and statistical evaluation under process variability conditions described in this section, the overall methodology also encompasses a radiation robustness analysis using the Quasar simulation framework to estimate critical LET threshold and identify sensitive nodes under SET conditions. Moreover, a system-level assessment is performed through the integration of the evaluated inverter topologies into arithmetic cells and their subsequent incorporation into a 32-bit RISC-V processor, enabling the analysis of area overhead and design-level implications. More details about the experiments executed in each one of the three parts of the development flow are presented in the respective chapter in the following part of this text, together with the results and discussions.

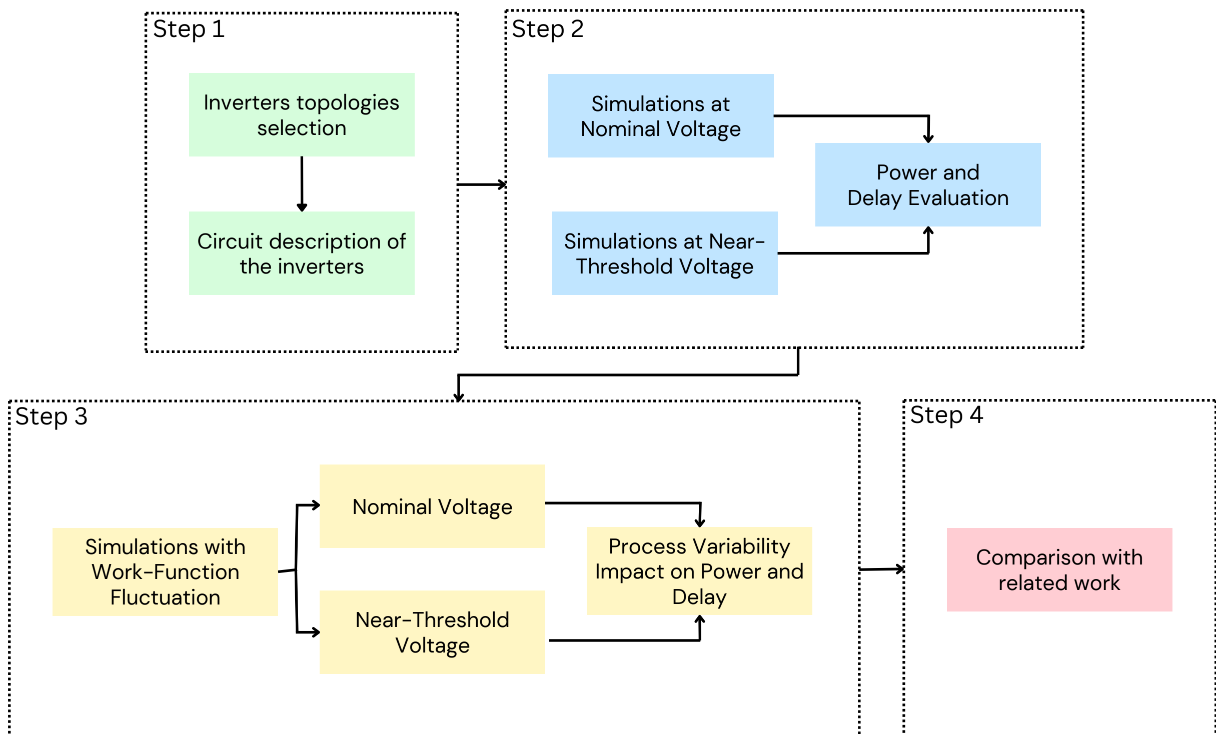
# 5 PROCESS VARIABILITY IMPACT ON THE HARDENING INVERTERS

The evaluation of the process variability impact on the hardening inverters starts with the analyzes of the process variability in FinFET inverter cells using four fault-tolerance techniques, assessing their impact on circuit electrical characteristics. The circuits presented in Figure 8, are based on the related work [Toledo, Reis & Meinhardt 2019] and modified to the FinFET technology constraints.

The techniques applied in the traditional inverter structure are Schmitt Trigger (ST), Pseudo-Strengthening, Strengthening and Rad-Hard. A detailed workflow of the first part is shown in Figure 11.

The results for this first evaluation of this research project are divided into three parts: 1) examining hardening techniques under normal and near-threshold (NT) conditions with regular behaviour, 2) assessing process variability under three WFF conditions, and 3) revisiting results related to bulk CMOS technology with a comparison to the impact of work-function fluctuations on FinFET devices.

Figure 11 – Detailed view of the Part 1: First case-study workflow




Source: The author.

## 5.1 REGULAR BEHAVIOR

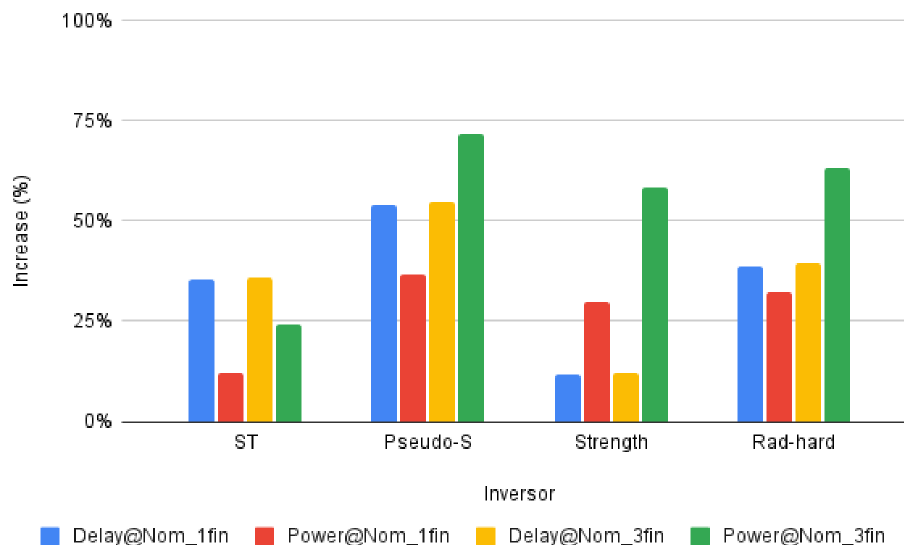
The initial segment of the results focuses on the nominal and NT inverter circuits with regular behavior, as presented in Table 3. The results show that for both voltages, there is a reduction in delay but a significant increase in energy values when comparing the transistors sizing from 1 to 3 fins. Under nominal conditions, with the adoption of hardening techniques, ST demonstrate to be the best in terms of energy consumption, with an increase of only 12.2% with 1 fin and 24.2% with 3 fins compared to the Standard Inverter, as seen in Figure 12. Strengthening displayed better performance concerning delay time, with an increase of approximately 12% for both cases, nominal and near-threshold operation, compared to the Standard Inverter. Pseudo-strengthening presented the worst results, with over a 53% increase in delay time and a 71.6% increase in energy consumption compared to the Standard Inverter.

Table 3 – Results for Nominal and NT operation, considering 1 fin for device and 3 fins for device on the evaluated Inverters

| **Inverter** | **Nominal** | | | | **Near-threshold** | | | |
|---|---|---|---|---|---|---|---|---|
| | **Nfin = 1** | | **Nfin = 3** | | **Nfin = 1** | | **Nfin = 3** | |
| | **Delay(ps)** | **Energy(fJ)** | **Delay(ps)** | **Energy(fJ)** | **Delay(ps)** | **Energy(fJ)** | **Delay(ps)** | **Energy(fJ)** |
| Standard | 2.76 | 0.99 | 2.73 | 1.55 | 9.16 | 0.53 | 9.08 | 0.81 |
| ST | 3.73 | 1.11 | 3.71 | 1.92 | 11.76 | 0.58 | 11.70 | 0.96 |
| Pseudo-S | 4.25 | 1.36 | 4.23 | 2.66 | 12.98 | 0.69 | 12.94 | 1.28 |
| Strength | 3.09 | 1.29 | 3.06 | 2.45 | 10.32 | 0.66 | 10.24 | 1.21 |
| Rad-hard | 3.83 | 1.31 | 3.81 | 2.53 | 12.05 | 0.68 | 11.99 | 1.26 |

Source: The author.

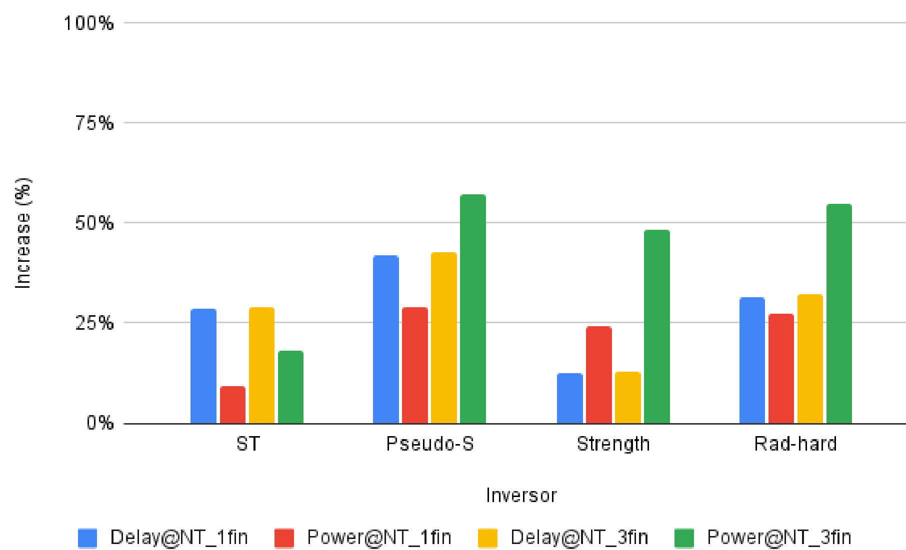
Figure 12 – Delay and Power at Nominal Voltage




Source: The author.

As for the NT operation, Strengthening demonstrated better performance in both aspects, as illustrated in Figure 13, with an increase of 12.7% for delay and 24.2% for energy, for the circuits with 1 fin, compared to the Standard Inverter. When considering 3 fins, there was a significant increase of 48.4% in energy compared to the standard, but it still demonstrated to have the lowest energy consumption. As for the worst results compared to the standard inverter, Pseudo-Strengthening showed an increase of almost 42% in delay and 29% in power consumption with 1 fin and 42.5% increase in delay and 57.1% in power consumption with 3 fin. Ultimately, as expected, circuits operating under nominal voltage exhibit better results in terms of delays, while circuits in near-threshold conditions demonstrate better energy consumption.

Figure 13 – Delay and Power at Near-Threshold Voltage




Source: The author.

Using the power delay product (PDP) as a figure of merit allows for a balanced evaluation between delay and power to determine the best technique. Table 4 illustrates the results. The Strengthening technique shows the best performance at nominal voltage and NT with one fin, with up to 45.2% increase. With three fins at nominal voltage, the Schmitt Trigger (ST) technique presented the smallest increase relative to the standard inverter, at 68.8% and also at NT voltage, with a 52.4% increase.

## 5.2 PROCESS VARIABILITY IMPACT

During Monte Carlo simulations, anomalies were observed, particularly with WFF deviations of 5% in near-threshold operation, leading to outliers in the data. These outliers, representing up to 3.5% of the Monte Carlo (MC) sample outcomes, were removed from the analysis due to model inaccuracies. The evaluation conducted here helps us observe that these

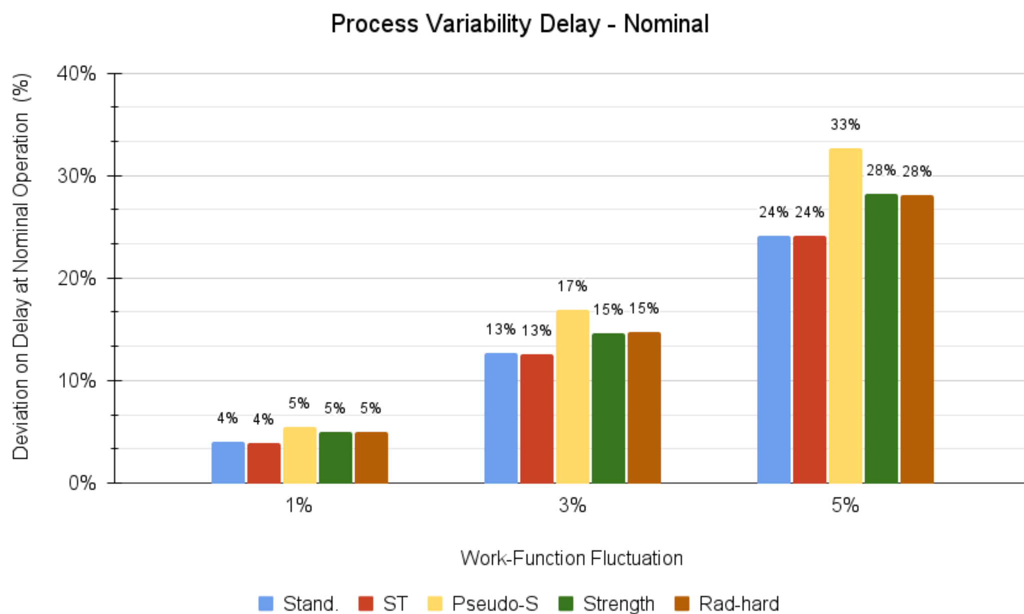
Table 4 – Power Delay Product for Nominal and NT conditions

| PDP | Nominal | | Near-threshold | |
|---|---|---|---|---|
| **Inverter** | **Nfin = 1** | **Nfin = 3** | **Nfin = 1** | **Nfin = 3** |
| ST | 51.84% | 68.81% | 40.38% | 52.43% |
| Pseudo-S | 110.59% | 165.77% | 82.75% | 123.90% |
| Strength | 45.20% | 77.29% | 40.02% | 67.33% |
| Rad-hard | 83.66% | 127.45% | 67.90% | 105.22% |

Source: The author.

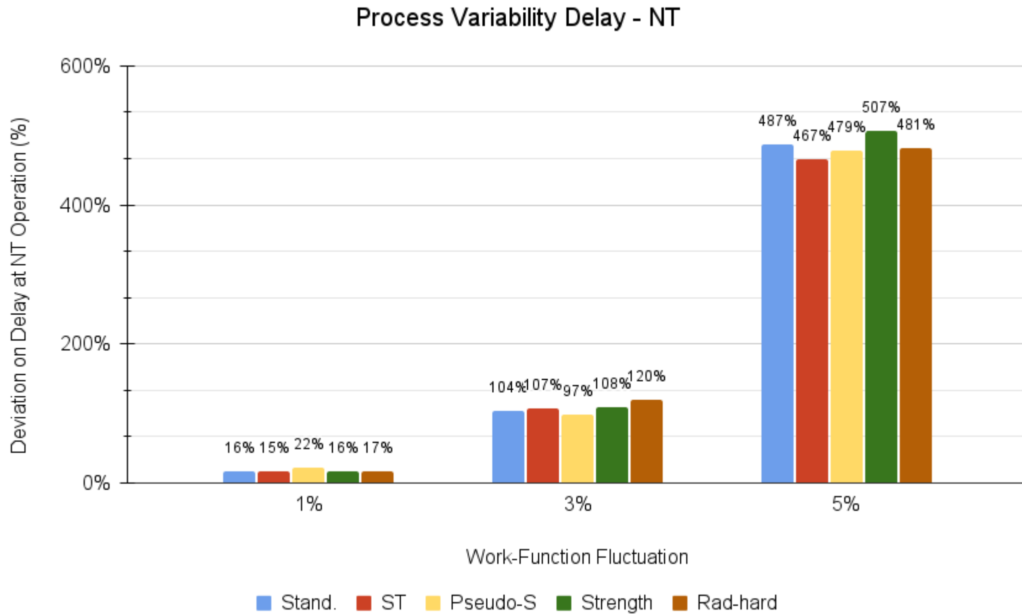
four techniques have different profiles and can be employed for various circuit requirements. The following evaluation discuss the results of the inverter circuits under process variability. Figures 14 and 15 show the impact of process variability on the delay at nominal and NT operation and demonstrate the considerable increase in deviation as the WFF increases. The figures pertain to transistor sizing with 1 fin, where no difference in delay times is observed between 1 and 3 fins. Under nominal conditions, the standard and ST inverters exhibit the smallest deviations, ranging from approximately 4% with WFF = 1% to 24% with WFF = 5%.

Figure 14 – Impact of process variability on the delay at nominal voltage operation




Source: The author.

Figure 15 – Impact of process variability on the delay at NT operation




Source: The author.

Regarding the delay in near-threshold conditions, it is possible to observe that the deviation values are much higher, and the standard inverter suffers more from higher variability effects, reaching a 487% deviation. Except for Strengthening, all other techniques perform better than the standard inverter under conditions of greater variability. The ST technique presented the best results when the WFF is 1% and 5%.

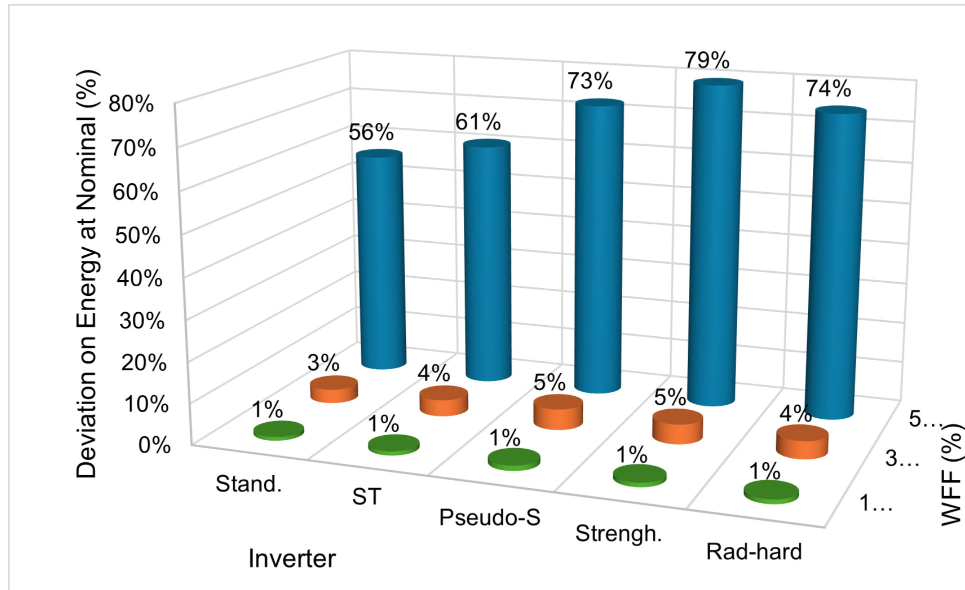
The impact of process variability on energy in nominal and NT conditions is detailed in Table 5. Transistor sizing significantly influences energy consumption. At nominal voltage with a WFF of 5%, Strengthening shows the highest deviation, increasing by 41.3% compared to the standard inverter for both 1 fin and 3 fins. Pseudo-Strengthening performs worst at WFFs of 1% and 3%. Figure 16 shows the impact on energy in nominal operation with 3 fins. When the WFF exceeds 3% a considerable impact on energy can be seen. ST obtained the best results while Strengthening presents the largest deviation. Figure 17 focuses on NT operation, with 3 fins, also revealing substantial energy impacts when WFF exceeds 3%. Among the techniques studied, ST demonstrates superior performance compared to the standard inverter.

Table 5 – Results of Impact of Process Variability on energy at the Nominal and NT operation, considering 1 fin and 3 fins

| Inverter | Sizing | WFF | Nominal | | | Near-threshold | | |
|---|---|---|---|---|---|---|---|---|
| | | | $\mu$ (fJ) | $\sigma$ (fJ) | $\sigma/\mu(\%)$ | $\mu$ (fJ) | $\sigma$ (fJ) | $\sigma/\mu(\%)$ |
| Standard | 1 fin | 1 | 0.96 | 0.0053 | 0.56 | 0.52 | 0.0018 | 0.36 |
| | | 3 | 0.96 | 0.0174 | 1.80 | 0.52 | 0.0105 | 2.00 |
| | | 5 | 0.96 | 0.2780 | 28.77 | 0.52 | 0.1940 | 36.69 |
| | 3 fin | 1 | 1.48 | 0.0137 | 0.92 | 0.78 | 0.0055 | 0.71 |
| | | 3 | 1.48 | 0.0509 | 3.44 | 0.78 | 0.0298 | 3.81 |
| | | 5 | 1.48 | 0.8330 | 56.20 | 0.78 | 0.5590 | 71.25 |
| ST | 1 fin | 1 | 1.06 | 0.0061 | 0.57 | 0.57 | 0.0025 | 0.45 |
| | | 3 | 1.06 | 0.0243 | 2.29 | 0.57 | 0.0140 | 2.44 |
| | | 5 | 1.07 | 0.3610 | 33.82 | 0.57 | 0.2480 | 43.15 |
| | 3 fin | 1 | 1.78 | 0.0179 | 1.01 | 0.92 | 0.0077 | 0.84 |
| | | 3 | 1.78 | 0.0722 | 4.06 | 0.92 | 0.0403 | 4.38 |
| | | 5 | 1.78 | 1.0800 | 60.77 | 0.92 | 0.7390 | 80.17 |
| Pseudo-S | 1 fin | 1 | 1.29 | 0.0118 | 0.91 | 0.67 | 0.0055 | 0.82 |
| | | 3 | 1.29 | 0.0419 | 3.25 | 0.67 | 0.0232 | 3.43 |
| | | 5 | 1.29 | 0.5960 | 46.12 | 0.67 | 0.4190 | 61.73 |
| | 3 fin | 1 | 2.44 | 0.0311 | 1.27 | 1.21 | 0.0161 | 1.33 |
| | | 3 | 2.44 | 0.1250 | 5.11 | 1.22 | 0.0682 | 5.59 |
| | | 5 | 2.46 | 1.7900 | 72.79 | 1.23 | 1.2600 | 101.93 |
| Strength. | 1 fin | 1 | 1.21 | 0.0081 | 0.67 | 0.64 | 0.0036 | 0.56 |
| | | 3 | 1.21 | 0.0365 | 3.00 | 0.64 | 0.0208 | 3.20 |
| | | 5 | 1.22 | 0.5930 | 48.76 | 0.64 | 0.4040 | 62.10 |
| | 3 fin | 1 | 2.23 | 0.0233 | 1.05 | 1.14 | 0.0107 | 0.94 |
| | | 3 | 2.23 | 0.1080 | 4.82 | 1.14 | 0.0611 | 5.34 |
| | | 5 | 2.24 | 1.7800 | 79.44 | 1.15 | 1.2100 | 105.07 |
| Rad-Hard | 1 fin | 1 | 1.24 | 0.0091 | 0.74 | 0.66 | 0.0036 | 0.55 |
| | | 3 | 1.25 | 0.0345 | 2.77 | 0.66 | 0.0200 | 3.01 |
| | | 5 | 1.25 | 0.5810 | 46.52 | 0.66 | 0.4120 | 61.80 |
| | 3 fin | 1 | 2.33 | 0.0255 | 1.10 | 1.19 | 0.0110 | 0.92 |
| | | 3 | 2.33 | 0.1010 | 4.35 | 1.19 | 0.0588 | 4.93 |
| | | 5 | 2.34 | 1.7400 | 74.43 | 1.20 | 1.2300 | 102.84 |

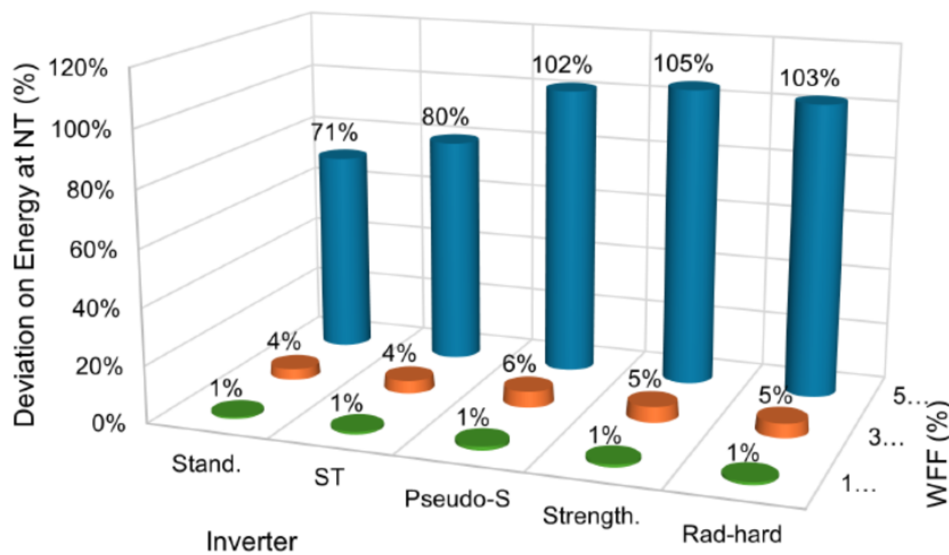
Source: The author.

Figure 16 – Impact of process variability on the energy at nominal operation with 3 fins




Source: The author.

Figure 17 – Impact of process variability on the energy at NT operation with 3 fins




Source: The author.

Finally, using the power delay product (PDP) to achieve a balanced evaluation between delay and power, Table 6 presents the normalized results with a work-function fluctuation of 3%. At nominal voltage with one fin, the Strengthening technique demonstrates the best performance, showing an increase of up to 42%. In near-threshold conditions, the Schmitt Trigger technique shows an increase of 37.2%. When using three fins at nominal voltage, the ST technique exhibits the smallest increase relative to the standard inverter, at 64.1%, and also at NT voltage, with a 48.9% increase.

Table 6 – Process Variability Power Delay Product with 3% WFF

| PDP | Nominal | | Near-threshold | |
|---|---|---|---|---|
| **Inverter** | **Nfin = 1** | **Nfin = 3** | **Nfin = 1** | **Nfin = 3** |
| ST | 50.27% | 64.06% | 37.21% | 48.88% |
| Pseudo-S | 106.17% | 156.28% | 77.58% | 117;59% |
| Strength | 41.98% | 70.46% | 37.48% | 64.13% |
| Rad-hard | 78.97% | 119.10% | 63.42% | 98.62% |

Source: The author.

## 5.3 COMPARISON WITH RELATED WORK

The study by [Toledo, Reis & Meinhardt 2019] on bulk CMOS technology contrasts with our findings on 7nm FinFET technology regarding process variability effects. Table 7 presents a comparative analysis of the 16 nm bulk CMOS results from [Toledo, Reis & Meinhardt 2019] and the 7 nm FinFET results, evaluated under both nominal and near-threshold (NT) operation. The comparison considers scenarios of regular behavior, i.e., without process variability (Reg), and, with process variability effects simulated by work-function fluctuation (WFF). The cells marked in red indicate the highest values, representing the worst-case results, while cells highlighted in blue indicate the lowest values, corresponding to the best-case outcomes. Under regular behavior assessment, Pseudo-Strengthening exhibited the lowest delay time at both nominal and near-threshold voltages, while the ST technique showed the highest delay times in both scenarios. In contrast to our study, where the Strengthening technique achieved the best delay results and Pseudo-Strengthening the worst under nominal conditions and at near-threshold voltage.

In terms of energy consumption, [Toledo, Reis & Meinhardt 2019] demonstrated that Strengthening had the lowest consumption compared to the standard inverter in both voltage conditions. Conversely, the ST technique showed significantly higher power consumption than the other techniques. However, in this study, the Schmitt Trigger technique had the lowest energy consumption among the techniques analyzed, across both voltage levels.

Regarding process variability results, in [Toledo, Reis & Meinhardt 2019] under nominal conditions Rad-Hard showed the lowest delay time deviation in their study, whereas ST performed best in ours. Under near-threshold conditions, Pseudo-Strengthening exhibited the highest deviation in their study, while Strengthening was most sensitive to variability in ours. In terms of energy, [Toledo, Reis & Meinhardt 2019] observed Rad-Hard as highly sensitive to process variability in both nominal and NT conditions. Similarly, Strengthening showed similar behavior in our study, being the most sensitive technique across both voltage conditions, meanwhile ST obtained the results with the lowest increase in energy consumption. Table 7 summarizes the comparison between the two works.

Table 7 – Comparison between 16 nm Bulk CMOS and 7 nm FinFET technologies operating at nominal and near-threshold (NT) voltage, considering regular behavior (Reg.) and with process variability effects (WFF).

| Inverter [1,2,3,4] | 16 nm bulk CMOS | | | | | | | | 7 nm FinFET | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Nominal | | | | NT | | | | Nominal | | | | NT | | | |
| | Reg. | | WFF | | Reg. | | WFF | | Reg. | | WFF | | Reg. | | WFF | |
| | E | D | E | D | E | D | E | D | E | D | E | D | E | D | E | D |
| ST | H | H | L | | H | H | | | L | | L | L | L | | L | L |
| Pseudo-S | | L | | | | L | | H | H | H | | H | H | H | | |
| Strength | L | | | H | L | | L | | | L | H | | | L | H | H |
| Rad-hard | | | H | L | | | H | L | | | | | | | | |

[1]E is adopted to represent the Energy(E) results.
[2]D is adopted to represent the Delay (D) results.
[3]H indicates the Highest (H) values, marked as red cells.
[4]L indicates the Lowest (L) values, marked as blue cells.

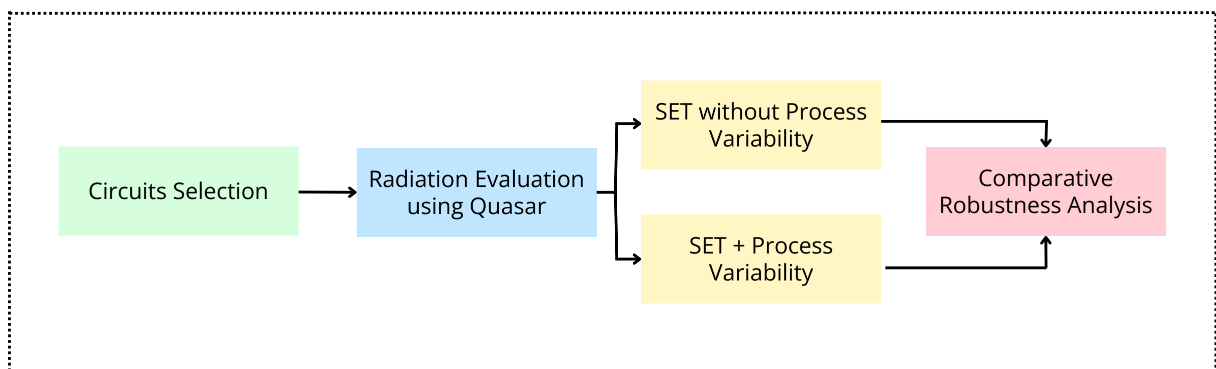
Source: The author.

One of the possible reasons for the differences of FinFET ST circuit compared the planar bulk CMOS results are related to the superior driven capability and higher signal stability of a FinFET device. A device with only 1 fin is equivalent to a planar CMOS transistor with a transistor width superior to 3 times the minimum width [Anil et al. 2003]. Thus, the FinFET device deals better with the hysteresis behavior of the ST, reducing the impact on power consumption. This behavior is under evaluation to provide a more detailed discussion about these main founded divergences on the previously reported behavior. As a complementary discussion, the four investigated techniques will be applied in arithmetic circuits and other benchmarks to evaluate the mitigation effects when applied to digital circuits.

# 6 SET IMPACT ON THE HARDENING INVERTERS

This chapter presents an extended analysis of Single Event Transients in hardening FinFET inverters. The evaluation reported in this chapter was submitted to the LATS 2026 [Dias et al. 2026]. This second evaluation analysis the SET impact on four investigated hardening techniques in 7 nm FinFET technology. While Chapter 5 focused exclusively on process variability effects, here the emphasis shifts to understanding how these circuits behave under energetic particle strikes and how this behavior changes once variability is introduced. The evaluation workflow adopted for the SET robustness analysis is summarized in Figure 18.

Figure 18 – Evaluation Workflow for SET Robustness Analysis




Source: The author.

The experiment begins by selecting the circuits, characterizing radiation tolerance in the absence of variability, and then incorporates work-function fluctuations to observe how variability modifies the LET threshold ($LET_{th}$), the spread of the robustness distribution, and the identity of the most sensitive node. Particular attention is given to the Schmitt Trigger inverter because its hysteresis mechanism strongly interacts with both SETs and variability, giving rise to behaviors that do not appear under deterministic conditions. The results also allow a comparative assessment of the strengthening and rad-hard designs, clarifying their limitations and effectiveness in advanced FinFET nodes.

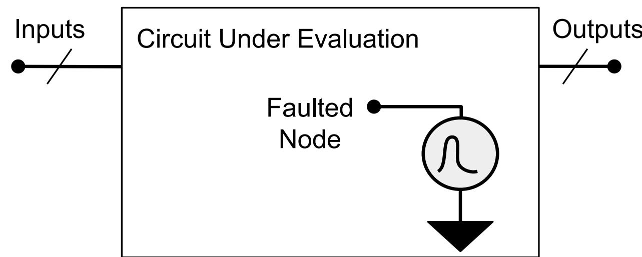
The analysis of the influence of process variability and radiation effects on circuit-level hardening techniques was carried out through a simulation flow designed to quantify the Linear Energy Transfer threshold under different circuit topologies, sizing, and levels of process variability. The four inverter topologies considered were Standard, Strengthening, Schmitt Trigger, and Rad-Hard. We remove the Pseudo-Strength circuit from further evaluation due to its worst performance in power, delay, and process-variability impact observed in the previous analysis.

Radiation sensitivity and the influence of process variations were examined using Quasar [Sandoval et al. 2025], an open-source environment designed for SET analysis that operates in conjunction with SPICE-level simulators. By employing Quasar, the number of HSPICE simulations required for the SET characterization is significantly reduced. The assessment begins with simulations of the inverter topologies without variability. For each design,

Quasar generates detailed data for multiple particle-strike scenarios, including the struck node, the corresponding input/output transitions, the injected current pulse, and the resulting Linear Energy Transfer (LET) threshold.

The injected current follows the conventional double-exponential model. The geometry of the pulse should be configured in Quasar to explore different pulse models. In these approaches, the pulse is modeled as a current source. It is injected into the node to represent the current pulse generated by a fault that occurred in the devices connected to this particular node. This fault model is represented in Figure 19, which illustrates the circuit under evaluation and the fault node insertion within its internal nodes.

Figure 19 – Fault Model




Source: [Sandoval et al. 2025]

The LET is computed using Eq. 6.1, where $I_P(t)$ denotes the injected current, $\tau_\alpha$ represents the junction charge-collection time constant, and $\tau_\beta$ corresponds to the ion-track formation time constant. In its default configuration, Quasar assigns $\tau_\alpha = 164$ ps and $\tau_\beta = 50$ ps [Carreno, Choi & Iyer 1990]. The charge-collection depth ($L$) is a configurable parameter in the Quasar tool and is determined by the target technology parameters. For the 7 nm node, the $L$ was set to 21. Due to differences in the charge collection mechanism of FinFET devices [Artola, Hubert & Alioto 2014], the gate length of the fin should be adopted as the charge collection depth restriction. Some studies have indicated that the behavior of the current pulse in some cases resembles a double exponential source, followed by a longer hold period before it decays. In [Nsengiyumva et al. 2017], a TCAD evaluation is presented that obtained low-LET (LET of 1 MeV cm$^2$/mg) results, with behavior similar to that of the traditional double exponential curve. However, when considering a high LET (LET of 60 MeV cm$^2$/mg), the curve has a hold period before decay. Despite the different pulse geometries according to the particular conditions of each experiment, in this work, we are interested in the relative robustness discussion, not in the absolute LET threshold values found.

$$LET = \frac{I_P(t) \times (\tau_\alpha - \tau_\beta)}{10.8 f \times L \times (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})} \tag{6.1}$$

Quasar incorporates process variability through Monte Carlo simulations to assess its impact on radiation robustness. The tool allows modeling different sources of variability, which

allows exploring the same three process-variability scenarios. The tool produces distributions of LET thresholds for all combinations of inverter type, fin count, and variability level. For each distribution, the statistical descriptors reported by Quasar were extracted, including the mean ($\mu$) LET and standard deviation ($\sigma$). The coefficient of variation ($\sigma/\mu$) was computed by dividing the LET standard deviation by the mean LET value, providing a normalized measure of the spread introduced by process variability. All simulation results were exported for post-processing, where deterministic simulations were represented solely by the extracted minimum LET for each inverter topology, while the Monte Carlo simulations were summarized through the mean LET, standard deviation, and coefficient of variation.

## 6.1 RADIATION ROBUSTNESS WITHOUT PROCESS VARIABILITY

The radiation response of the inverter topologies was initially examined without considering process variability, isolating the effects of SET under nominal electrical operating conditions. Table 8 reports the LET threshold ($LET_{th}$) obtained from Quasar for the four evaluated configurations (Standard, Strengthening, Schmitt Trigger, and Rad Hard), each simulated with devices using one fin and three fins.

The results indicate a clear dependence on device sizing: increasing the number of fins produces a pronounced increase in the LET threshold for every topology, which reflects a lower sensitivity to single-event effects. Among the investigated designs, the Schmitt Trigger inverter consistently achieves the highest LET threshold, followed by the Strengthening approach. Previous studies also show that the Schmitt Trigger supports favorable trade offs between energy efficiency and robustness when operated at very low power [Moraes et al. 2019] [Moraes et al. 2020]. It has also been demonstrated that this topology can substantially reduce energy consumption under voltage scaling that accounts for variability while still maintaining resilience, especially in deeply scaled FinFET technologies. Although energy oriented optimization is outside the scope of this study, these findings support the decision to include the Schmitt Trigger in the analysis and reinforce the strong results presented in Table 8.

The Rad Hard inverter, on the other hand, presents LET threshold values that are essentially the same as those of the Standard inverter, which indicates that this hardening approach does not produce a significant improvement in radiation tolerance at the 7 nm FinFET technology. In [Rathod, Saxena & Dasgupta 2009], the radiation evaluation of the Rad Hard inverter is performed by exploring variations in oxide thickness and shifts in threshold voltage, effects that are strongly reduced in metal-gate FinFET devices. Consequently, hardening strategies that rely on these mechanisms fail to deliver the expected protection at highly scaled technologies, even though they still offer the benefit of reduced area [Dias et al. 2025].

Table 8 – LET threshold for inverter designs with one and three fins under no variability

| Inverter | $LET_{th}$( MeV.cm$^2$/mg) | | Increase | |
|---|---|---|---|---|
| | 1 fin | 3 fins | 1 fin | 3 fins |
| Standard | 21.8 | 65.3 | baseline | baseline |
| Strengthening | 23.8 | 71.6 | 9.17% | 9.65% |
| Schmitt Trigger | 26.0 | 77.9 | 19.27% | 19.30% |
| Rad-Hard | 21.9 | 65.7 | 0.46% | 0.61% |

Source: The author.

## 6.2 COMBINING PROCESS VARIABILITY AND SET EFFECTS

Process variability was then incorporated through Monte Carlo simulations in Quasar using nominal WFF levels of 1%, 3%, and 5%. Table 9 reports the mean ($\mu$), standard deviation ($\sigma$), and coefficient of variation ($\sigma/\mu$) of the LET threshold for every inverter topology under all variability conditions and for both fin counts. The results indicate a gradual reduction in the mean LET as the variability level increases. This trend reflects the fact that variability tends to weaken the effective drive strength of the transistors, thereby increasing their sensitivity to charge disturbances. Even with the reduction in the mean LET, the relative ranking of the inverter topologies remains the same. The Schmitt Trigger continues to be the most resilient under all variability levels, followed by the Strengthening inverter, while the Standard and Rad Hard configurations remain practically equivalent.

Table 9 – Process Variability impact on the LET threshold ($LET_{th}$ ) for different levels of process variability and considering minimum sizing and devices sized with 3 fins. $LET_{th}$ values in MeV.cm$^2$/mg.

| Inverter | Fin | 1% | | | 3% | | | 5% | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $\mu$ | $\sigma$ | $\sigma/\mu$ | $\mu$ | $\sigma$ | $\sigma/\mu$ | $\mu$ | $\sigma$ | $\sigma/\mu$ |
| Standard | 1 | 21.77 | 0.83 | 3.84% | 21.67 | 2.50 | 11.55% | 21.30 | 4.12 | 19.35% |
| | 3 | 65.34 | 2.50 | 3.84% | 65.02 | 7.51 | 11.55% | 63.92 | 12.36 | 19.34% |
| Strengthening | 1 | 23.83 | 1.19 | 5.02% | 23.34 | 3.41 | 14.63% | 22.07 | 5.40 | 24.49% |
| | 3 | 71.53 | 3.60 | 5.04% | 70.13 | 10.29 | 14.68% | 66.28 | 16.25 | 24.52% |
| Schmitt Trigger | 1 | 26.01 | 1.14 | 4.41% | 25.69 | 3.11 | 12.12% | 24.73 | 4.99 | 20.20% |
| | 3 | 78.12 | 3.45 | 4.42% | 77.12 | 9.33 | 12.10% | 74.23 | 14.97 | 20.17% |
| Rad-Hard | 1 | 21.89 | 0.83 | 3.80% | 21.73 | 2.49 | 11.49% | 21.34 | 4.11 | 19.26% |
| | 3 | 65.68 | 2.49 | 3.80% | 65.20 | 7.48 | 11.48% | 64.04 | 12.33 | 19.26% |

Source: The author.

Although each hardening strategy reacts differently to the presence of variability, the normalized dispersion of the LET values remains comparable among all designs. In [Dias & Meinhardt 2024], the Schmitt Trigger inverter demonstrated the strongest robustness when evaluated across different WFF conditions, maintaining favorable delay and energy characteristics in every scenario. The results obtained here follow the same pattern. All inverter types present a lower mean LET as variability increases, yet the Schmitt Trigger consistently retains the highest average threshold, showing that it remains the least vulnerable to process variability.

The coefficient of variation serves as a normalized indicator of how strongly variability spreads the LET distribution. The $\sigma/\mu$ values present an almost identical evolution for every topology and for both fin configurations. All inverters show a coefficient of around 3 to 5% for 1% variability, around 11 to 14% for 3% variability, and around 19 to 24% for 5% variability. These values reveal that variability shifts the average LET of each design, but it does not significantly modify the overall width of the LET distribution. Since all inverter topologies exhibit nearly the same coefficient of variation under each variability condition, the influence of variability on the spread of the results is essentially uniform across the entire set of circuits. Within this scenario, the Schmitt Trigger continues to provide the most favorable combination of radiation robustness and tolerance to variability, sustaining higher LET thresholds without presenting a broader distribution than the other inverter topologies.

## 6.3 DETAILED EVALUATION OF WFF IMPACT

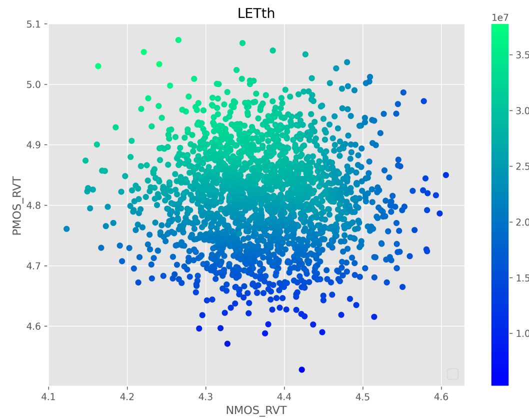
After identifying the Schmitt Trigger as the most effective inverter based hardening technique in terms of SET sensitivity and robustness to process variability, a more detailed analysis was carried out to understand how WFF influence its robustness. This evaluation focused on the LET threshold dependence of the device variability and how the WFF modifies the expected behavior of the Schmitt Trigger inverter. Figure 20 presents the dispersion of LET threshold values for the work-function derived from the Gaussian distribution with 5% of deviation, for devices implemented with 1 fin (a) and 3 fins (b).

The results indicate that the LET threshold decreases as the PMOS metal-gate work-function decreases from the nominal value, independent of the NMOS deviation. The most critical cases of SET faults are observed for metal-gate work-functions below 4.7eV. In addition, higher NMOS metal-gate work-function values, particularly above 4.5 eV, influence the expected robustness of the Schmitt Trigger, with the effect becoming more pronounced in the region where the PMOS devices haver low metal-gate work-function values. This behavior appears in both device sizes evaluated, although the absolute LET thresholds are significantly higher when device sizing is applied.

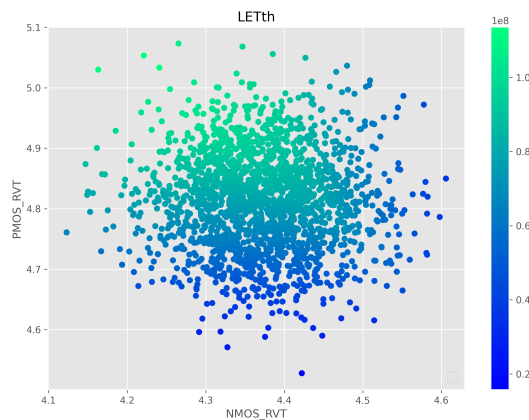
One of the most significant effects of process variability on the Schmitt Trigger cell is node-sensitive inversion. In all simulations performed without variability, the output node consistently appears as the most critical node, as expected for this topology. However, when variability is introduced, even the ST configuration with three fins can exhibit a different behavior, with the input node becoming the most critical in certain cases. This behavior occurs in the three inverter-based hardening techniques evaluated, however is more prominent in the Schmitt Trigger. These cases are shown in Figure 21 for three process-variability scenarios. In the conservative process-variability scenario, this effect can be seen only in Schmitt Trigger and occurs only in a few cases where the metal-gate work-function is higher for both PMOS and NMOS devices. This effect becomes much more pronounced at aggressive variability levels, as seen in (c), (f) and (i), where a significant number of cases show the input node becoming

Figure 20 – LET threshold dependence of the PMOS and NMOS metal-gate work-function fluctuation for the minimum size (fin=1) and for the devices sized as fin=3, considering 5% of deviation on the process variability distribution.

(a) Minimum sizing (each device with 1 fin.)




(b) Devices sized with 3 fins.

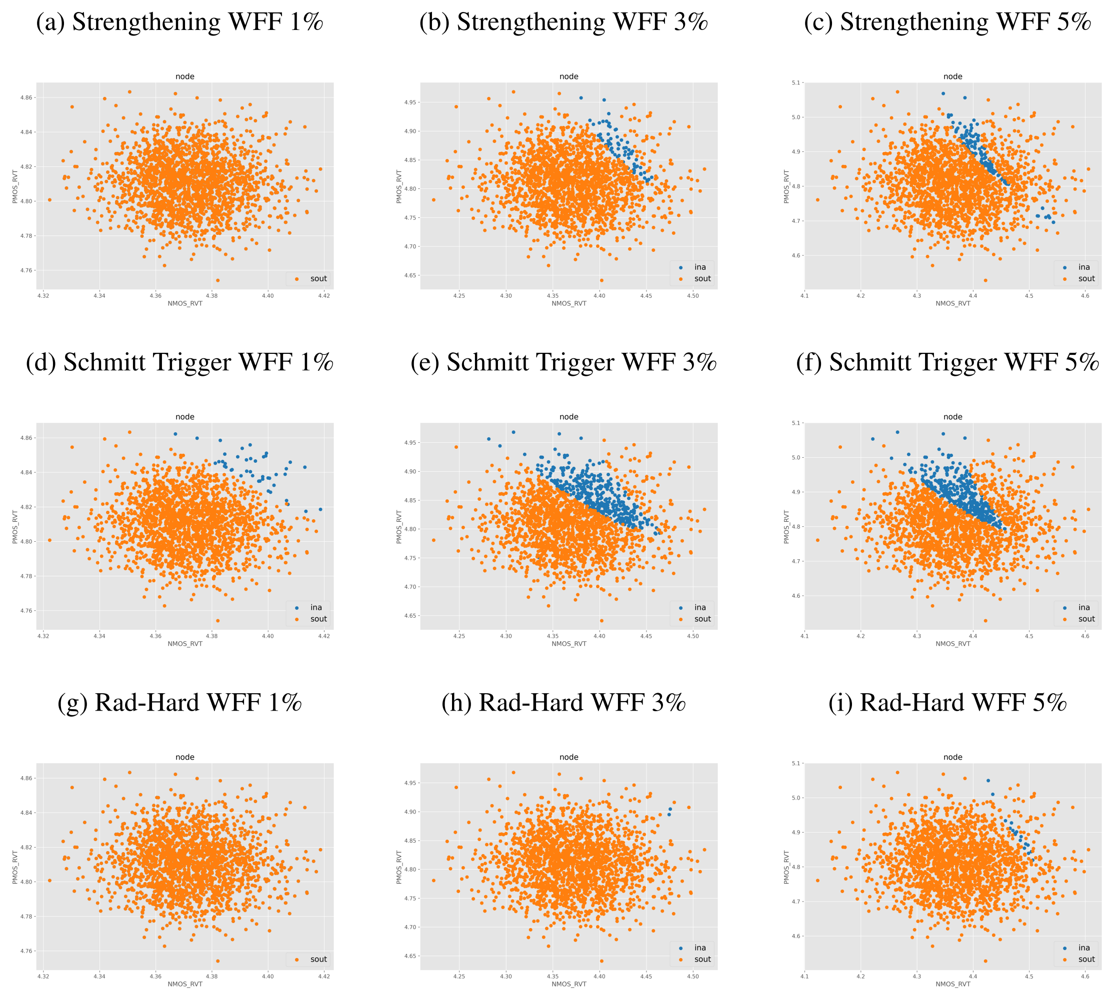



Source: The author.

critical, especially for medium NMOS deviation combined with high PMOS work-function deviation. These findings highlight the importance of including process variability in robustness evaluations, as it exposes atypical behaviors and conditions that must be accounted for, thereby improving robust design and fault-tolerant applications.

The complete analysis presented in this chapter forms the basis for subsequent architectural-level evaluations and supports the selection of candidate circuits for integration into the arithmetic units discussed in the next chapter.

Figure 21 – Evaluation of the sensitive node considering metal-gate work-function fluctuation for NMOS and PMOS devices of three inverter-based hardening techniques with each device with 3 fins and different levels of process variability.




Source: The author.

# 7 IMPACT EVALUATION ON A RISC-V DESIGN

This chapter presents a case study on integrating radiation-hardening inverter topologies into a RISC-V processor design. FinFET-based technologies are highly susceptible to process variability and transient faults, especially under near-threshold operation. Although circuit-level hardening techniques have shown promise in isolated cell-level evaluations, it is essential to understand their implications when applied to real, large-scale designs. Thus, the main objective is to evaluate the impact of selective hardening on system-level metrics such as area, delay, and power consumption. In particular, the Arithmetic Logic Unit (ALU) and internal adder modules are targeted for modification, as they are among the most critical blocks in the processor pipeline in terms of both performance and vulnerability to transient effects.

This experiment is designed as part of the requirements of the final design for the CI Inovador Program - track digital, a complementary activity developed in the last year of this Master course. The content presented in this chapter builds upon the results reported from the synthesis of a complete processor in two technology nodes, and were also previously published in [Dias et al. 2025]. The original report forms the foundation for the analyses discussed here, which are extended to provide additional detail and integration with the overall objectives of this dissertation and the evaluation considering SET and process variability effects.

By introducing hardening inverters only in specific datapath locations, more specifically in the final stages of full adder circuits, this third evaluation aims to assess whether fault tolerance can be improved with negligible physical overhead. The approach supports the broader goal of this work, which is to combine robustness against radiation and variability without compromising the overall efficiency of digital systems.

To assess the potential area overhead associated with radiation-tolerant inverters, we selected the RS5 processor [Nunes et al. 2024], a RISC-V-based design. The RS5 core stands out for its modular structure, which allows designers to enable or disable architectural extensions such as M (integer multiplication and division) and Xosvm (memory management). This flexibility makes it possible to tailor the processor to different application requirements. In addition, RS5 provides optional performance counters for real-time monitoring of both application behavior and core activity, as well as support for multitasking through an operating system that incorporates a dedicated memory management mechanism. So, RS5 implements the RISC-V 32-bit Integer Module processor core and a complete digital flow was performed on it. As depicted in Figure 22, this processor includes an Execute stage with an Arithmetic Logic Unit (ALU), making it ideal for analyzing full adder cells within a realistic pipeline context [Nunes et al. 2024].

Figure 22 – Four-stage pipeline of the RS5 processor [Nunes et al. 2024]

Source: [Nunes et al. 2024]

## 7.1 METHODOLOGY

To a more comprehensive discussion, this analysis was carried out using two distinct technology nodes, allowing the investigation of robustness techniques across a range of technologies. In addition to the 7 nm FinFET ASAP7 PDK [Clark et al. 2016], the processor circuit was synthesized in a 45 nm CMOS standard-cell library.

To enable a quantitative analysis of the area and power overhead of integrating hardening inverters, full adder cells were examined both within the ALU and throughout the processor architecture. For timing closure, target clock cycles were set to 3 ns for the 45 nm design and 2 ns for the 7 nm implementation, corresponding to operating frequencies of 333 MHz and 500 MHz, respectively. The synthesis flow and the adopted Cadence tools are presented in Fig. 23, and the details of the transistor-level design and simulation, as well as the logic and physical synthesis, are described in the next subsections.

Figure 23 – Synthesis Flow

Source: The author.

### 7.1.1 Transistor-Level Design and Simulation

The four inverter topologies considered for this experiment are the Standard, Strengthening, Schmitt Trigger, and Rad-Hard. These designs were previously evaluated in Chapter 5 in terms of propagation delay, energy consumption, and process variability, and in Chapter 6 in terms of process variability and radiation effects.

In this experiment, we adopted the extracted circuit from the layout view for three topologies, implemented and simulated at the transistor level using Cadence Virtuoso and Spectre, due to the availability of the Cadence tools in the context of the CI Inovador program and the limited access to the HPICE Synopsys tool. For the 45 nm technology, the planar CMOS devices have the distinct behavior for PMOS and NMOS transistors, with different dopants and mobilities that demand a careful transistor size. In this case, transistor sizing was performed using the Logical Effort method to ensure consistent performance comparisons across topologies. Simulations were conducted under both nominal supply voltages (1.0 V for 45 nm and 0.7 V for 7 nm).

The hardening inverters were then incorporated into mirror adder architectures, utilizing the ADDFX2 standard cell in the 45 nm PDK and the FAX1 cell in the 7 nm PDK. In both cases, the radiation-hardened inverters were used to replace the final logic stage driving the carry-out (Co) and sum (Sum) outputs. To replicate realistic input behavior, each test circuit was driven by a chain of inverters designed to emulate practical signal slopes. The load at the output was modeled using a fan-out-of-four (FO4) inverter to ensure consistency across simulations. Propagation delay was recorded as the maximum delay observed among all output transitions. For dynamic energy measurements, the current drawn during switching was integrated over the interval corresponding to the worst-case delay.

### 7.1.2 Logic and Physical Synthesis

Before assessing how the incorporation of radiation-tolerant inverters affects the area, power, and timing of the processor, the RS5 design must first undergo complete functional verification and synthesis in both technology nodes. This step ensures that the baseline implementation is correct and that all subsequent comparisons reflect only the impact of the hardening strategies rather than inconsistencies in the design flow. For this reason, the RS5 processor was fully verified, synthesized, and physically implemented in both the 45 nm CMOS library and the 7 nm FinFET ASAP7 library, following an identical methodology across technologies.

The processor underwent functional verification prior to synthesis. The verification was performed in the Xcelium simulator, where a dedicated testbench executed a Fibonacci workload included in the RS5 distribution. This step confirmed that the baseline RTL behaved correctly before proceeding with implementation in the two technology nodes.

Logic synthesis was then conducted using Cadence Genus. The RS5 core was synthesized separately for the 45 nm CMOS standard cell library and for the 7 nm FinFET library available in the ASAP7 PDK [Clark et al. 2016]. The timing constraints reflected the intended operating frequency of each technology: a 3 ns clock period for the 45 nm process (333 MHz) and a 2 ns period for the 7 nm process (500 MHz).

For both technology nodes, the synthesis results were examined to identify the number of full adder instances present in different parts of the design, including the ALU, isolated adder blocks, and the full processor. Examples include the ADDFX2 cell in 45 nm and FAx1 cell in 7 nm. From these blocks, metrics such as total cell count, cell area, net area, and overall area were collected, normalized according to the unit conventions of each PDK (2000 microns for 45 nm and 1000 microns for 7 nm). Power estimations comprised leakage, internal, switching, and total power.

Physical implementation was performed in Cadence Innovus. The physical design sequence followed the standard digital backend flow, which included RTL loading from Verilog, floorplanning, placement of standard cells, clock tree synthesis, routing, insertion of filler cells, and the execution of design rule, connectivity, and geometric checks.

In the 45 nm implementation, the layout relied on five metal layers, and the power ring was routed using Metal4 and Metal5. The die boundaries extended from (0, 0) to (554400, 554400) in the PDK's 2000 micron unit grid. For the 7 nm FinFET version, six metal layers were used. The die limits were defined from (0, 0) to (68634, 68094), with unit scaling of 1000 micron units.

## 7.2 RISC-V ELECTRICAL AND STATISTICAL ANALYSIS

The electrical characterization begins with the circuit-level analysis since the radiation hardening strategies are introduced at this stage of the design flow. The comparative evaluation of the inverter topologies is essential for understanding how the full adder architectures and consequently the RISC V modules are affected once the hardening inverters are integrated into the datapath. Data for propagation delay and dynamic energy consumption in both 45 nm and 7 nm technologies were extracted from both logic and physical synthesis flow, allowing a consistent interpretation of the behavior of the hardening techniques under different device characteristics.

Table 10 presents the propagation delay and energy values for the five inverter designs when implemented in the 45 nm technology. As observed in the table, the Schmitt Trigger inverter produces the highest delay and energy consumption due to its hysteresis based switching behavior, while the Rad Hard inverter maintains a modest increase relative to the standard cell. In contrast, the Strengthening and Pseudo-Strengthening designs produce intermediate behavior, presenting delay values much higher than the standard inverter and energy values slightly higher. These results reinforce the tradeoffs inherent to circuit level hardening techniques and highlight the Rad Hard design as the most balanced one for this node.

Table 10 – Propagation delay and energy consumption for inverter designs - 45 nm

| **Inverter** | **Delay (ps)** | **Energy (fJ)** |
|---|---|---|
| Standard | 7.37 | 0.23 |
| Strengthening | 9.32 | 0.70 |
| Pseudo-Strengthening | 10.00 | 0.79 |
| Schmitt Trigger | 17.40 | 0.90 |
| Rad-Hard | 8.78 | 0.57 |

Source: The author.

A second set of simulations performed in 7 nm FinFET technology is summarized in Table 11. The absolute delay values decrease substantially due to the intrinsic speed of the FinFET devices, while the energy values increase because of the higher parasitic capacitances and leakage currents typical of advanced nodes. Nevertheless, the relative tendencies between the topologies remain consistent. In this technology node, when compared to the Standard inverter, the Rad-Hard inverter ranks third in both delay and energy consumption, meanwhile Schmitt Trigger ranks second in delay and first in energy, presenting opposite behaviour from the 45 nm node. It is interesting to compare these results with the previously presented in Table 3. The similarity indicates that the adoption of SPECTRE or HSPICE is not affecting the observed values.

Table 11 – Propagation delay and energy consumption for inverter designs – 7 nm

| **Inverter** | **Delay (ps)** | **Energy (fJ)** |
|---|---|---|
| Standard | 2.73 | 1.55 |
| Strengthening | 3.06 | 2.45 |
| Pseudo-Strengthening | 4.23 | 2.66 |
| Schmitt Trigger | 3.71 | 1.92 |
| Rad-Hard | 3.81 | 2.53 |

Source: The author.

To assess the practical impact of these inverters in a realistic context, this experiment integrates each hardening inverter into a full adder cell. Table 12 shows the propagation delay and dynamic energy results for the full adder designs in the 45 nm technology.

Table 12 – Propagation delay and energy consumption for full-adder designs - 45 nm

| **Full Adder** | **Delay (ps)** | **Energy (fJ)** |
|---|---|---|
| Standard | 137.38 | 15.86 |
| Strengthening | 126.52 | 14.69 |
| Pseudo-Strengthening | 122.11 | 15.06 |
| Schmitt Trigger | 156.57 | 17.51 |
| Rad-Hard | 121.76 | 14.13 |

Source: The author.

The observation of the results found from the insertion of the inverters on a full adder and raised from the second evaluation, considering the inverters-based approaches to mitigate SET and process variability effects, motivates this work to consider two different scenarios of design requirements on the following evaluations:

In the first scenario, the area impact is the main requirement. Observing the results from Table 12, the Rad-Hard-based full adder achieves the smallest delay and the lowest energy among all variants. Interestingly, even the standard full adder does not outperform the radiation-hardened version in delay, confirming that replacing the final-stage inverters does not degrade timing. On the contrary, improvements in drive reinforcement in some robust topologies compensate for the increase in device count. However,the results in Chapter 6 show that the Rad-Hard topology provides almost no improvement in robustness relative to the Standard inverter, even under different variability levels, because the physical mechanisms exploited by this method are largely suppressed in advanced metal-gate technologies.

In the second scenario, the mitigation of SET and process variability is considered. From the discussion in Chapter 5, the most robust cell was the Schmitt trigger. Among the circuits, the Schmitt Trigger inverter consistently demonstrates the highest LET threshold, followed by the Strengthening topology. In addition to its radiation robustness, prior work shows that the Schmitt Trigger enables favorable energy robustness trade-offs when properly tuned for ultra-low-power operation [Moraes et al. 2019] [Moraes et al. 2020]. It has also been shown that ST topologies can significantly reduce energy consumption under variability-aware voltage scaling while preserving robustness, particularly at advanced FinFET nodes. Although such low-power optimization is beyond the scope of this work, it further motivates the inclusion of the Schmitt Trigger among the evaluated designs and reinforces the strong performance observed in Table 3. In contrast, the Rad-Hard inverter exhibits LET threshold values nearly identical to those of the Standard inverter, suggesting that the applied hardening approach does not significantly improve robustness in the 7 nm FinFET technology. In [Rathod, Saxena & Dasgupta 2009], the radiation evaluation of the Rad-Hard inverter is performed by exploring oxide thickness variations and threshold voltage shifts, an effect that is largely suppressed in metal-gate FinFETs. As a result, hardening techniques that exploit these mechanisms fail to provide the expected radiation-hardening benefits at scaled nodes, even though they maintain the advantage of reduced area [Dias et al. 2025].

## 7.3 AREA ANALYSIS OF THE RS5 PROCESSOR IN 45 NM TECHNOLOGY

The evaluation of area impact begins with a transistor level interpretation, since the custom hardening full adder cells do not have physical layouts available. The standard full adder cell employed in the 45 nm library contains twenty eight transistors including the two output inverters. When these inverters are replaced by the Strengthening, Pseudo Strengthening or Schmitt Trigger variants the total transistor count increases to thirty six which corresponds to an area increase of approximately twenty eight percent. In contrast, the Rad Hard topology requires only two additional transistors resulting in a total of thirty two and an area increase of roughly fourteen percent. These values are summarized in Table 13.

Table 13 – Transistor count and estimated area increase for full adder cell implementations - 45 nm

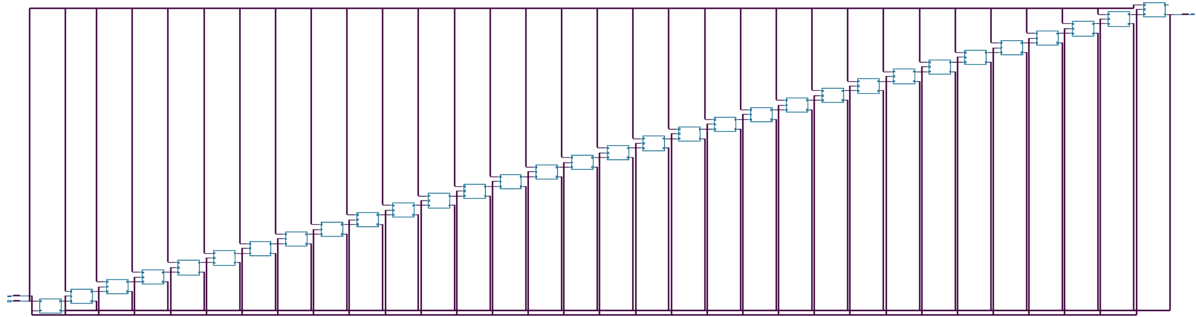
| Full Adder Implementation | Transistor Count | Area Increase (%) |
|---|---|---|
| Standard | 28 | Baseline |
| Strengthening | 36 | 28.6% |
| Pseudo-Strengthening | 36 | 28.6% |
| Schmitt Trigger | 36 | 28.6% |
| Rad-Hard | 32 | 14.3% |

Source: The author.

Although these figures provide a conservative estimation, they indicate that the Rad Hard inverter delivers radiation tolerance with a minimal area penalty. Furthermore, layout optimization strategies that reuse diffusion regions and adjust transistor placement can reduce the actual area overhead even further. Therefore, based on area, the Rad Hard topology was a candidate for selective integration.

The next step is to examine how many full adder instances exist inside the RS5 processor. It was identified that each 32-bit adder in the ALU consists of one ADDHX1 half adder followed by thirty one ADDFX2 full adders. Considering two adders in the ALU and additional arithmetic logic present elsewhere in the RS5 core the total number of ADDFX2 cells in the processor is 63. This configuration corresponds to a Ripple Carry Adder (RCA) architecture, as seen in Figure 24, where each full adder propagates the carry to the next stage sequentially. Given that the area impact applies only to the ADDFX2 cells and that the proposed hardening would modify only the output stage of each adder the corresponding silicon area overhead remains extremely small at the processor level.

Figure 24 – Architecture of 45 nm 32-bit adders



Source: The author.

According to data from the 45 nm PDK, the ADDHX1 cell occupies approximately 47.82% of the area of an ADDFX2 cell. For simplification, we approximate this to 50% in the analysis below.

$$\text{Adder Area}_{\text{standard}} = 31 \cdot A + \frac{A}{2} = 31.5A$$

$$\text{Adder Area}_{\text{Rad-Hard}} = 31 \cdot (1.143A) + \frac{A}{2} = 35.933A$$

$$\text{Adder Area}_{\text{Schmitt Trigger}} = 31 \cdot (1.1286A) + \frac{A}{2} = 40.366A$$

Table 14 summarizes the area metrics of the RS5 processor, the ALU, and its internal adders. These values have been corrected to reflect actual micrometer-scale units based on the design configuration.

Table 14 – Synthesized Area Metrics for RS5 Processor Modules - 45nm

| **Module** | **Cell Count** | **Cell Area** (μm$^2$) | **Net Area** (μm$^2$) | **Total Area** (μm$^2$) |
|---|---|---|---|---|
| Adder | 32 | 0.12 | 0.01 | 0.13 |
| ALU | 1071 | 1.26 | 0.52 | 1.78 |
| RS5 | 15392 | 24.89 | 10.99 | 35.89 |

Source: The author.

To quantify the effect of integrating Rad Hard full (Scenario 1) or Schmitt Trigger (Scenario 2) adder cells in a realistic design context, the evaluation considered the total area of each module, combining both standard cell area and routing overhead. This approach offers a more representative indication of how robustness-oriented modifications influence the final physical implementation. As summarized in Table 15, substituting the conventional adder with its Rad Hard counterpart results in an area growth of roughly 14.1% for the 32 bit adder, 1.07% for the ALU, and only 0.053% for the complete RS5 processor. These results show that the overhead rapidly diminishes as the scope increases, indicating that selective hardening of critical regions can be applied with virtually no system-level penalty.

When Scenario 2 is considered, the use of Schmitt Trigger based adders introduces a larger penalty, consistent with their higher transistor count. Integrating Schmitt Trigger cells increases the area of a 32-bit adder by roughly 19.2%, which represents a significantly higher overhead than the Rad-Hard alternative. However, once propagated to the block level, this difference becomes less pronounced, with the ALU area growing by approximately 2.95% and the total RS5 area increasing by only 0.13%.

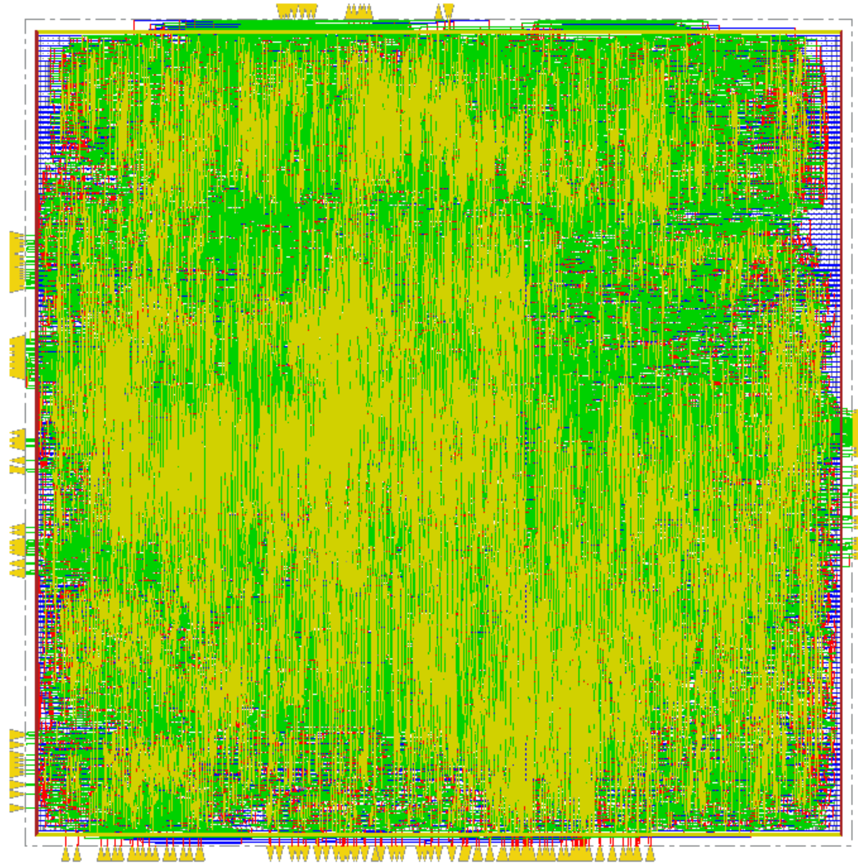
Table 15 – Estimated Area Impact of Using Rad-Hard Adder Cells (Scenario 1) or Schmitt Trigger Cells (Scenario 2) - 45nm

| **Module** | **Current Area** ($\mu m^2$) | Scenario 1 | | Scenario 2 | |
|---|---|---|---|---|---|
| | | **Estimated Increase** (%) | **New Area** ($\mu m^2$) | **Estimated Increase** (%) | **New Area** ($\mu m^2$) |
| Adder | 0.135 | 14.1 | 0.154 | 28.15 | 0.173 |
| ALU | 1.779 | 1.07 | 1.798 | 4.27 | 1.854 |
| RS5 | 35.890 | 0.053 | 35.909 | 0.21 | 35.965 |

Source: The author.

Finally, Figure 25 illustrates the post-synthesis layout obtained after completing the place and route flow for the RS5 processor in the 45 nm technology. The image offers an overall view of the area occupied by the full design and reinforces the conclusion that selective hardening produces only a marginal effect on the final layout. The compact arrangement of cells and interconnects reflects the high integration density achievable in advanced technologies, which allows the processor to remain area efficient even when additional hardened cells are introduced.

Figure 25 – Physical Layout of the 45nm Technology Synthesis



Source: The author.

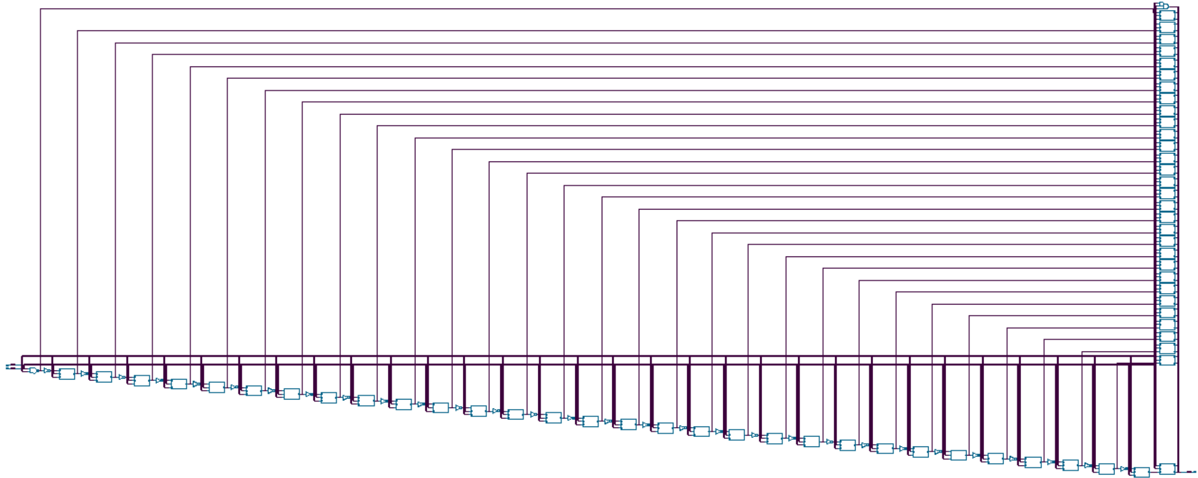
## 7.4 AREA ANALYSIS OF THE RS5 PROCESSOR IN 7 NM TECHNOLOGY

To extend the evaluation performed beyond the 45 nm implementation, this section examines the RS5 processor synthesized using the 7 nm FinFET technology. Inspection of the synthesized netlist identified a total of 260 FAx1 full adder instances throughout the processor. Of those, 62 appear within the ALU, specifically, 31 in each of the two 32 bit adder blocks, while the remaining 198 are distributed among other functional units. Even though most FAx1 cells lie outside the ALU, the adders inside the ALU belong to the processor's critical timing path, where timing margins are tighter and violations are more likely to impact execution.

In the ALU, the processor utilizes a parallel prefix adder (PPA) architecture, as shown in Figure 26, in its 32-bit adders, instantiated twice within the ALU. Each PPA is composed of the following cells:

- 31 FAx1 full adders, each with 24 transistors, including two inverters (one per output).
- 31 MAJIxp5 logic cells, each occupying half the area of FAx1.
- 1 NAND2xp5, 1 INVx1, 29 INVxp67, and 1 OA211x2.

Figure 26 – Architecture of 7 nm 32-bit adders



Source: The author.

The full adder structure used in this technology allows for the evaluation of the potential impact of adopting radiation-hardening versions of the `FAx1` cells. Table 16 shows the transistor count and estimated area increase for each full adder cell implementation on the 7 nm technology.

Table 16 – Transistor count and estimated area increase for full adder cell implementations - 7 nm

| Full Adder Implementation | Transistor Count | Area Increase (%) |
|---|---|---|
| Standard | 24 | Baseline |
| Strengthening | 32 | 33.3% |
| Pseudo-Strengthening | 32 | 33.3% |
| Schmitt Trigger | 32 | 33.3% |
| Rad-Hard | 32 | 16.7% |

Source: The author.

Although both technologies exhibit similar trends regarding the relative impact of the hardened full adders, the analysis in this chapter considers two distinct scenarios for the 7 nm implementation. Scenario 1 evaluates the adoption of the Rad Hard full adder, and Scenario 2 evaluates the integration of the Schmitt Trigger based full adder. The choice to include the Schmitt Trigger in Scenario 2, despite its larger area footprint, follows directly from the conclusions of Chapter 5, where the Schmitt Trigger demonstrated significantly higher robustness to the combined influence of process variability and radiation effects. Tab. 17 summarizes the area metrics of the entire RS5 processor synthesis, for the ALU individually, and for ALU internal adders.

Table 17 – Synthesized Area Metrics for RS5 Processor Modules - 7 nm

| Module | Cell Count | Cell Area (μm$^2$) | Net Area (μm$^2$) | Total Area (μm$^2$) |
|---|---|---|---|---|
| Adder | 93 | 0.01 | 0.002 | 0.01 |
| ALU | 1060 | 0.10 | 0.042 | 0.14 |
| RS5 | 16483 | 2.38 | 0.97 | 3.35 |

Source: The author.

Table 18 demonstrates the estimated area impact of using Rad-Hard Adder Cells (Scenario 1) or Schmitt Trigger Cells (Scenario 2). Scenario 1 results in a 9.58% increase in the 32 bit adder area when the Rad Hard version replaces the standard `FAx1`. This modification leads to a 0.73% increase in the ALU area and a 0.031% increase in the total RS5 processor area. In Scenario 2, assuming the adoption of a Schmitt Trigger version of the FAx1 cell, which introduces four additional transistors per output (33.3% increase in transistor count), and considering the PPA design structure, it is estimated a 19.19% increase in the 32-bit adder area. The ALU experiences a modest increase of less than three percent, while the expected increase in the total processor area is approximately 0.126%, which is negligible in practical terms. While the percentages differ between the two scenarios, both scenarios result in processor level impacts below one percent, allowing a direct comparison between an area focused alternative (Scenario 1) and a robustness oriented alternative (Scenario 2).

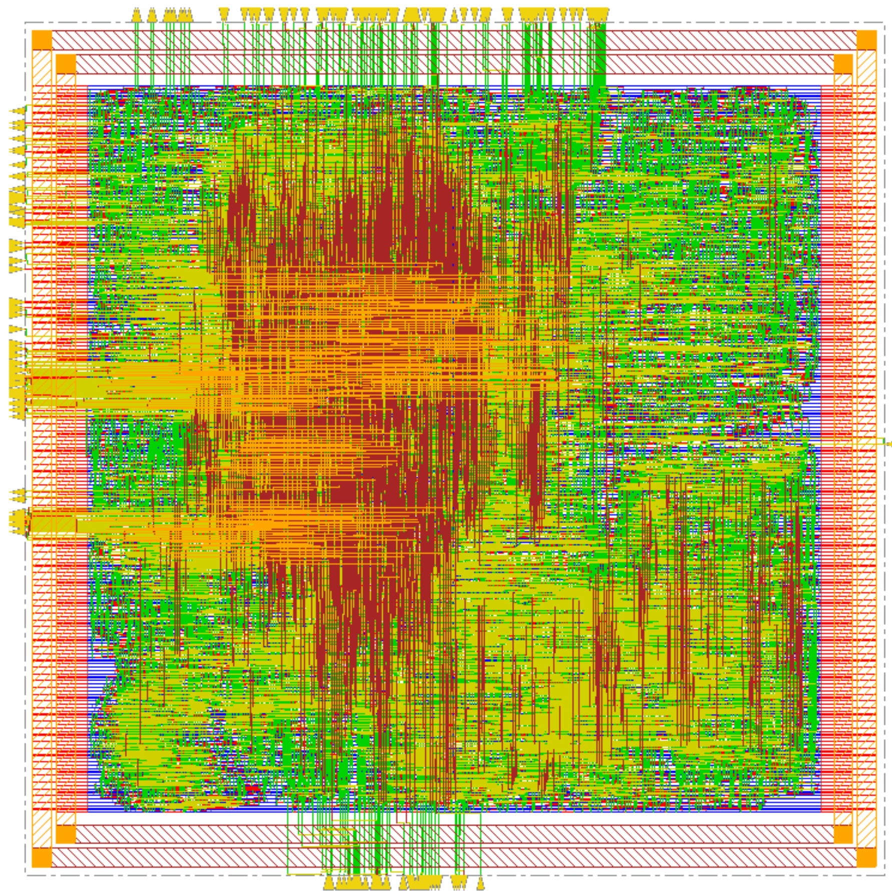
Table 18 – Estimated Area Impact of Using Rad-Hard Adder Cells (Scenario 1) or Schmitt Trigger Cells (Scenario 2) - 7 nm

| Module | Current Area (μm$^2$) | Scenario 1 | | Scenario 2 | |
|---|---|---|---|---|---|
| | | Estimated Increase (%) | New Area (μm$^2$) | Estimated Increase (%) | New Area (μm$^2$) |
| Adder | 0.010 | 9.58 | 0.0109 | 19.19 | 0.013 |
| ALU | 0.143 | 0.73 | 0.144 | 2.93 | 0.147 |
| RS5 | 3.353 | 0.031 | 3.363 | 0.13 | 3.357 |

Source: The author.

Figure 27 shows the physical layout obtained after place and route when the RS5 processor is implemented with the 7 nm FinFET standard cell library. The compact arrangement of cells and interconnects illustrates the high integration density characteristic of FinFET technologies, which allows designs to remain highly condensed even as the number of logic elements increases. Examining the final layout offers a global perspective on circuit organization and routing complexity at scaled technology nodes. This view also highlights that introducing additional logic elements, such as hardening full adder cells, can be accommodated with minimal area impact, particularly when these modifications are restricted to critical regions of the processor.

Figure 27 – Physical Layout of the RS5 in 7 nm Technology



Source: The author.

# 8 CONCLUSION

This work investigated the combined impact of process variability on circuit-level hardening techniques, with emphasis on inverter-based topologies implemented in 7 nm FinFET technology. The study was motivated by the increasing susceptibility of deeply scaled devices to process variability, mainly in regards of work-function fluctuation and soft errors. Within this context, four hardening approaches were evaluated under nominal operating conditions, under work-function fluctuations, and under single-event transient disturbances. Their implications were further analyzed in arithmetic circuits and at the processor-level through integration into a RISC-V architecture.

The first analysis focused solely on the electrical impact of process variability. Results demonstrated that increasing levels of WFF introduce significant deviations in propagation delay and energy consumption, especially at near-threshold voltage. Among the evaluated techniques, the Schmitt Trigger consistently exhibited the smallest delay and energy under variability, in relation to the Standard inverter. Strengthening circuits achieved the best delay under regular behavior but were more strongly affected by WFF, presenting higher deviation values in both delay and energy. Pseudo-Strengthening, which showed the worst delay, energy, and variability results, was therefore removed from the subsequent SET analysis. The comparison with previous bulk CMOS works confirmed that FinFET technologies modify the relative behavior of these techniques, largely due to superior driven capability and higher signal stability.

The second set of experiments evaluated the SET robustness of three circuits, first without variability and then combining SET analysis with WFF effects. Using Quasar to characterize the LET threshold for each topology, the results showed that the ST inverter again achieved the highest robustness, maintaining a larger LETth even when variability was introduced. Process variability not only reduced the LET threshold in all circuits but also increased the spread of the robustness distribution, sometimes altering the most sensitive node within a given topology. These observations confirm that SET and process variability interact, and that evaluating them separately can mask important reliability concerns in nanometer technologies.

The third part of the work extended the analysis to the system level by integrating hardening inverters into full-adder cells and synthesizing the RS5 RISC-V processor in both 45 nm CMOS and 7 nm FinFET nodes. The results demonstrated that, although the use of hardening techniques increases the transistor count of the full-adder cells (for instance, a 33.3% increase in 7 nm when adopting ST-based adders), the corresponding area impact at the module and processor levels is minimal. In the 7 nm flow, the increase was limited to 2.93% in the ALU area and only 0.13% in the total RS5 area, confirming that selective insertion of circuit-level techniques is feasible even in advanced nodes with area constraints.

Overall, the general evaluation demonstrated that inverter-based circuit-level mitigation techniques remain effective for improving reliability in modern FinFET technologies, especially when process variability and SET effects are considered jointly. The Schmitt Trigger emerged as the topology offering the best overall compromise among delay, energy, variability tolerance, and radiation robustness, whereas the Strengthening technique remains attractive for delay optimization under regular behavior but is more sensitive to variability. The results reinforce the importance of adopting variability-aware and radiation-aware design methodologies in advanced nodes, where traditional assumptions of deterministic behavior no longer hold.

Future work may extend the methodology adopted in this dissertation in several directions. The next set of evaluations may focus on replicating the full set of experiments using Decoupling Cells (DCELL) allowing a comparison between inverter-based hardening structures and capacitance-based mitigation strategies. Additional investigations may also include other structures commonly adopted in robust design, such as the C-element, to assess how different classes of combinational filters respond to WFF deviations and to variations in LET sensitivity. Another important extension is the investigation of near-threshold operation in the parts of the study conducted only under nominal conditions which would clarify how low voltage operation modifies the interaction between process variability and SET robustness. Finally, making the layout of the full adder cells with the hardened inverters at their outputs and characterizing the extracted cells would allow a more realistic area analysis and show their behavior when integrated into more complete systems.

## 8.1 PUBLICATIONS

The partial results derived from the development of this work, started in March 2024, had been submitted to three conferences. At this moment, the results have been accepted to oral presentation in two events of international impact. The third submission is still under review at this moment. The first case-study of the impact of process variability on 7 nm FinFET radiation hardening inverters presented here, have been published in the 31st IEEE International Conference on Electronics Circuits and Systems, 2024.

It is important to note that, as a complementary activity, participation in the CI Inovador Program provided additional knowledge in digital design that contributed to the evaluation of the applicability of hardening techniques to a RISC V design, particularly for the area optimization scenario presented here. These results were published at SBCCI 2025. In addition, as part of the CI Inovador Program, a two month professional experience was carried out at FrontGrade Gaisler in Sweden, centered on digital circuit design tasks and workflows, complementing the academic development achieved in this work.

1. **M. Dias**, C. Meinhardt, "Process Variability Impact on 7 nm FinFET Radiation Hardening Inverters" in *31st IEEE International Conference on Electronics Circuits and Systems (ICECS)*, Nancy, France, 2024.

2. **M. Dias**, P. Butzen, R. Reis, C. Meinhardt. Impact of Circuit-Level Radiation-Hardening Techniques in Adders on a RISC-V Design in *2025 38th SBC/SBMicro/IEEE Symposium on Integrated Circuits and Systems Design (SBCCI)*, Manaus, Brazil, 2025.
3. **M. Dias**, B. Sandoval, P. Butzen, R. Reis, C. Meinhardt. "Mitigation of sets under process variability effects: Circuit-level strategies for reliable design" in *27th Latin American Test Symposium (LATS)*, Florianópolis, Brazil, 2026.

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